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HIPSR: A Digital Signal Processor for the Parkes 21-cm Multibeam Receiver

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HIPSR (HI-Pulsar) is a digital signal processing system for the Parkes 21-cm Multibeam Receiver that provides larger instantaneous bandwidth, increased dynamic range, and more signal processing power than the previous systems in use at Parkes. The additional computational capacity enables finer spectral resolution in wideband HI observations and real-time detection of Fast Radio Bursts during pulsar surveys. HIPSR uses a heterogeneous architecture, consisting of FPGA-based signal processing boards connected via high-speed Ethernet to high performance compute nodes. Low-level signal processing is conducted on the FPGA-based boards, and more complex signal processing routines are conducted on the GPU-based compute nodes. The development of HIPSR was driven by two main science goals: to provide large bandwidth, high-resolution spectra suitable for 21-cm stacking and intensity mapping experiments; and to upgrade the Berkeley-Parkes-Swinburne Recorder (BPSR), the signal processing system used for the High Time Resolution Universe (HTRU) Survey and the Survey for Pulsars and Extragalactic Radio Bursts (SUPERB).

Keywords: instrumentation: spectrographs — instrumentation: polarimeters — methods: observational — telescopes

1. Introduction

The CSIRO Parkes 64-m radio telescope is equipped with a multibeam receiver that covers a frequency range of 1.23-1.53 GHz. This receiver consists of 13 cryogenically cooled dual-polarization feeds in a hexagonal array (Staveley-Smith *et al.*, 1996). The receiver was designed primarily for redshifted 21-cm hydrogen line (HI) observations over $0 \leq z < 0.2$ and was installed in 1997, along with the MBCORR digital signal processing (DSP) system. Until its decommissioning in 2016, MBCORR remained the primary signal processing system for 21-cm line emission studies with the multibeam receiver.

An additional DSP backend was installed at Parkes in 2008, designed for high time-resolution spectroscopy with the multibeam receiver (McMahon, 2008; Keith *et al.*, 2010). This backend was known as the Berkeley-Parkes-Swinburne Recorder (BPSR) and it replaced an analog filterbank that was designed and used for the Parkes Multibeam Pulsar Survey (PMPS; Stairs *et al.*, 1999). BPSR originally consisted of 26 Xilinx Virtex-2 Pro FPGA-based spectrometers connected by 10 gigabit Ethernet to a cluster of 13 servers, which further processed and reduced the signal before writing the spectra to disk for offline processing. BPSR processes the entire usable bandwidth of the receiver at high time resolution and has enabled a remarkable series of discoveries of radio pulsars and fast radio bursts (e.g. Keith *et al.*, 2010; Levin *et al.*, 2010; Bates *et al.*, 2011; Bailes *et al.*, 2011; Burke-Spolaor *et al.*, 2011; Keith *et al.*, 2012;

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Burke-Spolaor *et al.*, 2012; Bates *et al.*, 2012; Thornton *et al.*, 2013; Burgay *et al.*, 2013; Levin *et al.*, 2013; Tiburzi *et al.*, 2013; Ng *et al.*, 2014; Bates *et al.*, 2015). However, the spectra produced by BPSR are too coarsely channelized ($\Delta\nu \sim 390$ kHz) for neutral hydrogen observations.

In this article, we report on the HI-Pulsar (HIPSR) system, an upgrade to BPSR providing new high spectral resolution modes for HI observations. The HIPSR system, installed at Parkes in 2011, digitizes the entire usable bandwidth of the multibeam receiver, has increased resilience to radio frequency interference, and provides a significant increase in overall computational power in comparison to MBCORR and BPSR.

2. System Design

The HIPSR system uses an heterogeneous architecture consisting of an interconnected network of general purpose graphics processing units (GP-GPUs) and field programmable gate arrays (FPGAs). This architecture allows processing tasks to be divided between DSP ‘nodes’, with wide-bandwidth DSP conducted on FPGAs, and moderate to low-bandwidth DSP tasks performed on the GPUs.

This division of DSP is motivated by the relative advantages and weaknesses of the two DSP platforms. In recent years, GPUs have emerged as an attractive platform for parallelizable radio astronomy algorithms. For example, pulsar dedispersion pipelines (Barsdell *et al.*, 2010; Magro *et al.*, 2011), and low to moderate-bandwidth, large-N correlators (Clark *et al.*, 2013; Kocz *et al.*, 2014), have been shown to be well suited to GPU implementations.

For wide-bandwidth DSP, FPGAs are ubiquitous. FPGAs are well suited to wide-bandwidth applications as their I/O bandwidth is limited only by the number and speed of I/O pins upon the chip, whereas the I/O bandwidth of CPUs and GPUs are limited by the speed of the host’s data busses. On the other hand, algorithms which require large amounts of data to be stored in memory are poorly suited to FPGA-based implementations, as there is a limited amount of logic and memory available within each FPGA chip.

Many of the algorithms used in radio astronomy are well suited to FPGA implementations. For example, the CASPER collaboration provides a library of efficient FPGA gateway for radio astronomy, such as digital downconverters, vector accumulators, and polyphase filterbank (PFB) structures (Parsons *et al.*, 2009; Hickish *et al.*, *this issue*). Pulsar dedispersion pipelines have also been demonstrated on FPGAs (Clark *et al.*, 2014). The decision between GPUs and FPGAs (or any other DSP architecture for that matter) is dependent mainly upon the ease of deployment for the set of algorithms one wishes to run. For multi-purpose DSP systems — such as HIPSR — a heterogeneous architecture allows the advantages of both platforms to be leveraged.

2.1. HIPSR Packetized Architecture

The HIPSR system may be described as a multi-node DSP ‘frontend’ connected to a multi-node DSP ‘backend’ by a 10Gb Ethernet (10GbE) switch. The FPGA-based DSP frontend conducts signal processing tasks such as signal filtering and channelization; the GPU-based DSP backend performs higher-level, moderate- to low-bandwidth DSP such as running pulsar processing pipelines. A diagram of the system architecture is shown in Fig. 1.

Packetized DSP systems are becoming increasingly common within radio astronomy, see for example the Precision Array for Probing the Epoch of Reionization (PAPER) correlator (Parsons *et al.*, 2010), the Large-Aperture Experiment for detecting the Dark Ages (LEDA) correlator (Kocz *et al.*, 2015), and VEGAS, the Versatile Greenbank Astronomical Spectrometer (Roshi *et al.*, 2011; Chennamangalam *et al.*, 2014). The inclusion of a switch greatly increases the flexibility of the system as data can be dynamically routed between nodes. It does, however, require all data to be packetized along with metadata that describes the packet’s data payload. Nevertheless, using a switched 10GbE-based packetized architecture instead of defining and commissioning a bespoke backplane has drastically decreased development time: all interconnect is off-the-shelf, industry standard, commodity hardware.

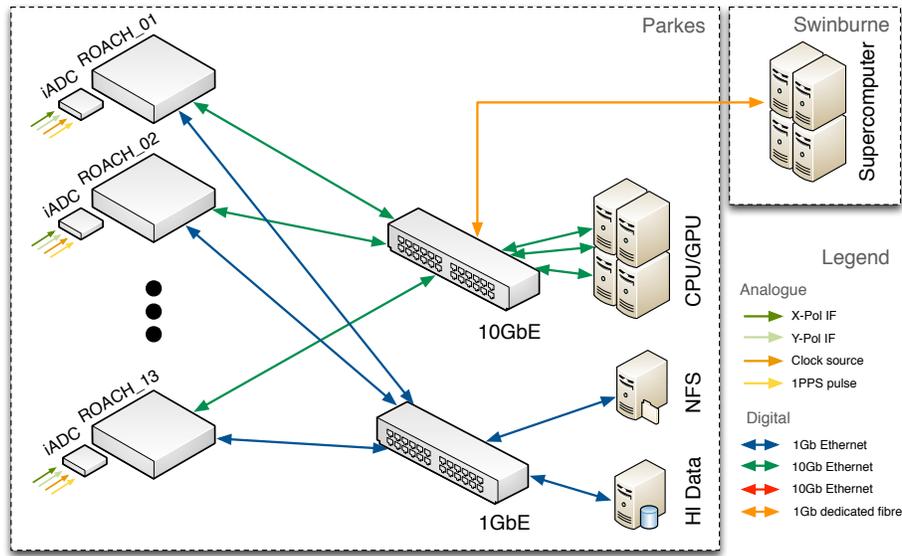


Fig. 1. HIPSR network diagram. The ROACH-based DSP frontend is pictured on the left; these are connected via a 10 Gb Ethernet switch to the GPU-based DSP backend. 1 Gb Ethernet is used for monitor and control, and for low-bandwidth data transport from the FPGA frontend.

2.2. Hardware Overview

The DSP frontend consists of 13 Reconfigurable Open Architecture Computing Hardware (ROACH) signal processing boards, each of which has an FPGA as its centerpiece. Each ROACH has a 2-input, 1 Gsample/s digitizer mezzanine card installed, which allows for a total of 26 inputs to be digitized (i.e. every IF of the multibeam receiver). The DSP backend consists of 8 server nodes, each of which is equipped with dual Nvidia C2070 GPUs. This hardware is discussed in further detail below.

2.2.1. The CASPER ROACH Board

The ROACH is a Xilinx SX95T Virtex-5 FPGA-based signal processing board designed for radio astronomy applications. ROACH is open-source hardware provided by the Collaboration for Astronomical Signal Processing and Electronic Research (CASPER)¹.

The ROACH board has four CX4-type Ethernet connectors that allow up to 40 Gb/s of bandwidth for data transfer over 10 GbE or XAUI protocols. Daughter boards, such as analog-to-digital converters, may be connected via the two Z-DOK interfaces, each with 40 differential pairs connecting to the FPGA I/O pins. General Purpose Input/Output (GPIO) pins are also provided for control of miscellaneous sensors and external devices. For temporary storage of large vectors, the FPGA is connected to quad data rate random access memory (QDRII+ RAM) and double data rate memory (DDR2).

The Virtex-5 FPGA on the ROACH is connected to a PowerPC chip by an On-Chip Peripheral Bus (OPB) controller. The PowerPC runs a customized Linux kernel and provides monitor and control for the board. It has its own dedicated DDR2 and Flash memory, 1 Gb Ethernet port, USB port, and SD memory card socket. The OPB interface allows the PowerPC to reprogram the FPGA and to access registers and memory resources on the FPGA fabric. This simplifies data readout and provides a convenient way to reconfigure the firmware running on the FPGA.

¹<http://casper.berkeley.edu>

Table 1. Atmel AT84AD001B performance characteristics ([Atmel, 2009](#)).

ADC specification	
Sampling rate	1GS/s (2GS/s interleaved)
Number of bits	8
Effective number of bits	6.8
Full scale input	500mVpp
Spurious free dynamic range	-54 dBc
Differential non-linearity	0.25 LSB
Integral non-linearity	0.5 LSB
Bit error rate	10^{-13} at 1GS/s

2.2.2. *iADC Digitizer Card*

The digitizer used in HIPSR, known as the iADC or ADC2x1000-8, is an 8-bit, 2-input analog-to-digital converter (ADC) card designed by CASPER. The iADC is a Eurocard-sized daughter board that connects to the ROACH via the Z-DOK connector. It is powered by an Atmel/e2V AT84AD001B digitizer chip, which runs at speeds of up to 1024 Msample/sec. Inputs are connected to the iADC’s SMA jacks; a Mini Circuits ADTL2-18 balun (30 MHz to 1.8 GHz bandwidth) converts the signals from single-ended to differential.

When in operation, an external frequency reference tone must be presented as a clock signal. A pulse per second (1PPS) may also be connected; this signal is passed through to the FPGA so multiple ROACH boards may be synchronized to within a FPGA clock cycle. Using the iADC, two signals with bandwidths of up to 512 MHz may be digitized. Alternatively, the AT84AD001B offers an interleave mode which sacrifices one input but is then able to digitize 1024 MHz from a single input. In HIPSR, the former is used exclusively.

Two important characteristics for digitizers are crosstalk levels between signal inputs, and the linearity of the digitizer response. Crosstalk of the iADC has been measured by to be under -28 dB ([Parsons *et al.*, 2010](#)), and was found to stable enough such that it can be removed to levels ~ 60 dB. Differential and integral non-linearity has been tested experimentally and found to be in accordance with the manufacturer’s quoted specification (differential 0.25 LSB, integral 0.5 LSB). Further specifics of the iADC are listed in Tab. 1.

2.2.3. *GP-GPU Server Nodes*

The GP-GPU server nodes are bespoke systems, built to specification by Silicon Graphics Pty. Ltd. Each of the 8 server nodes comprise dual 2.66 GHz Intel Xeon six-core CPUs, 48 GB DDR3 memory, and dual Nvidia Tesla C2070 GP-GPUs. While a majority of DSP is conducted on the GPUs, the Intel Xeon CPUs may also be used, if required.

As each server has a single CX4-type 10 GbE network interface card (NIC), the input data rate for each server is limited to 10 Gb/s. Given that there are 26 IFs which must be processed by 8 server nodes, the DSP frontend must decrease the data rate² from each IF from 6.4 Gb/s to about 3.0 Gb/s.

2.2.4. *Data Server*

In addition to the GPU server nodes, there is a server that provides monitor and control for the DSP frontend, and provides data storage. This server has a 2.4 GHz Intel Xeon four-core CPU, and 24 GB DDR3 memory. As it is not used for DSP, it does not have a GPU. This server runs a DHCP daemon and provides a network file system (NFS) to the ROACH boards.

²digitized data rate is $2 \times 400\text{MHz} \times 8\text{bit} = 6.4\text{Gb/s}$

2.2.5. Node Interconnect

As shown in Fig. 1, the DSP frontend and backend nodes are connected via a 10 Gb Ethernet switch. This Cisco 4900M switch is configured with 24 CX4-type ports, 13 of which are connected to the DSP frontend ROACH boards, and 8 of which are connected to the server nodes. The switch allows bi-directional data flow between nodes. The 10 GbE switch also has a dedicated 1 GbE fiber link to the Green II supercomputer³ at Swinburne University of Technology in Melbourne, Australia.

All nodes are also connected by 1 GbE through a Cisco 3750 switch. For low data bandwidth applications, where all of the necessary DSP to reduce data rates is conducted on the FPGA, all data may be read off the 1 GbE ports of the ROACH boards.

2.3. Installation and Cabling

In March 2012, the HIPSR hardware was installed into radio frequency interference (RFI) shielded racks (Fig. 2), located on the second floor of the Parkes 64-m telescope building (this room lies underneath the telescope dish). A set of BNC-terminated cables were laid under the floor from the existing multibeam IF distribution panel to feedthroughs installed on the racks; another internal set of cables connect the bulkhead to the SMA input of the iADC cards. The 1PPS input of the iADC cards are connect to a PPS distribution unit, and similarly a synthesized reference clock signal is distributed to each iADC board. A single ‘master’ ROACH board is connected to the Parkes Calibration Control Unit (CCU), by a coaxial cable between the CCU and a GPIO output on the master ROACH.

Each server node and ROACH board is connected to a 1 GbE switch by an Ethernet cable (CAT-5E STP). Similarly, each server node and ROACH is connected to a 10 GbE switch via CX4-type cables.

3. Modes of Operation

HIPSR can be operated in either high-time resolution or 21-cm spectral line modes. While commensal modes are possible in principle, spectral line work requires the cycling of a reference noise diode at 128 Hz, which is problematic for high-time resolution studies. As such, commensal observations are not supported.

3.1. High Time Resolution Modes

The total data rate as digitized for the 26 inputs to the ROACH iADC cards is 166.4 Gb/s. As there are a total of 8x 10 GbE connections to the GPU servers, bandwidth over the 10 GbE network is a bottleneck. Therefore, the data rate is typically decreased by time integration on the FPGA boards, lowering bit depth, extracting a subset of frequency channels, or dropping the number of IF signals sent to the GPU servers.

Data are captured on the GPU servers using PSRDADA⁴, which provides the ‘pipeline’ infrastructure on which several modes of operation are based. That is, PSRDADA writes the data to ring buffers in shared memory and manages the routing, monitoring and processing of the high-throughput data stream. The various pulsar observing modes are detailed in Sarkissian *et al.* (2011); we give a brief overview of these modes here, focusing on the modifications and improvements afforded by HIPSR.

3.1.1. Berkeley-Parkes-Swinburne Recorder (BPSR)

The aforementioned Berkeley-Parkes-Swinburne Recorder (BPSR) is a high time-resolution digital filterbank data acquisition and processing system, designed for pulsar and transient detection. When originally installed, BPSR consisted of 13 CASPER iBOB boards, each connected to a Dell 1950 server-class machine. The functionality of the original BPSR system is completely reproduced and BPSR is now a mode of operation of the HIPSR system. This required a recompilation of the iBOB FPGA code for the ROACH platform, during which some important improvements to the polyphase filterbank were made; first, the

³<http://astronomy.swin.edu.au/supercomputing/green2/>

⁴<http://psrdada.sourceforge.net/>

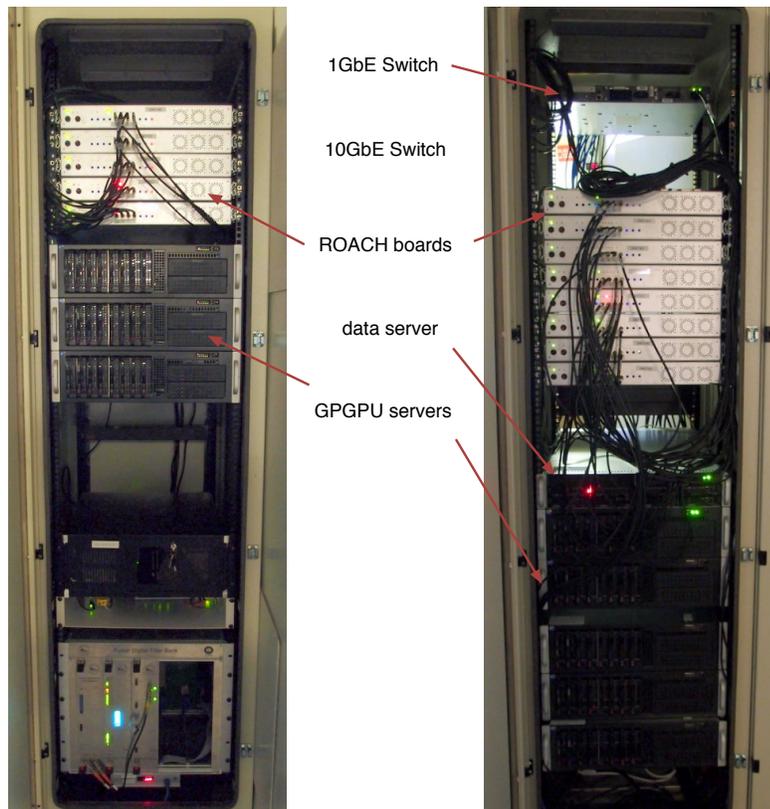


Fig. 2. HIPSr hardware installed into Parkes 64-m telescope RFI shielded racks.

ROACH enabled improved bit-precision within the FFT and the addition of extra filterbank taps; more importantly, the spectrometer was upgraded to produce all four Stokes parameters, which enabled the first detection of the polarization of a Fast Radio Burst (FRB; Petroff *et al.*, 2015).

For BPSR, the ROACH boards apply a 1024-channel, 4-tap Hamming-windowed polyphase filterbank to the 400 MHz bandwidth inputs. The signals are then detected, integrated for 64 μ s, decimated to 8 bits, then packetized and sent via 10 GbE to the GPU compute nodes. The GPU compute nodes then sum, normalize, and decimate to 2 bits per sample, before writing to disk in real-time using DSPSR⁵ (van Straten & Bailes, 2011).

On HIPSr, the BPSR system is capable of realtime searches for FRB events using the Heimdall⁶ processing software. Heimdall performs a search for single pulses across a range of specified dispersion measures, returning a list of candidate events that may then be saved to disk for further analysis. The Heimdall pipeline employs the dedisp⁷ library, which implements a GPU-accelerated algorithm for incoherent dedispersion (Barsdell *et al.*, 2012). This real-time ability was exploited in Petroff *et al.* (2015), where a FRB event was detected and used as a trigger for follow-up observations at different observatories.

The BPSR system is discussed in further detail in Keith *et al.* (2010) and McMahon (2008). Note that these papers detail the original iBOB-based hardware; however, apart from the additional features described above, these papers remain an accurate overview.

⁵<http://dspsr.sourceforge.net/>

⁶<http://heimdall-astro.sourceforge.net/>

⁷<http://dedisp.googlecode.com>

3.1.2. CASPER Parkes Swinburne Recorder

The CASPER Parkes Swinburne Recorder (CASPSR) is used to perform phase-coherent dispersion removal over the full bandwidth of a single dual-polarization beam. CASPSR consists of a single iBOB and iADC digitizer that digitizes and outputs the full 400 MHz of bandwidth at Nyquist rate (6.4 Gb/s) to the backend servers over 10 GbE. These data are then saved to disk, using PSRDADA for packet capture and DSPSR for disk write. While the iBOB firmware has been ported to ROACH, the original iBOB frontend is still primarily used.

3.2. 21-cm line spectral observing modes

3.2.1. Wide-bandwidth Spectroscopy

For the 21-cm modes of operation all DSP is performed on the ROACH boards. HISPEC_400_8192 is an 8192-channel, 400-MHz bandwidth PFB spectrometer, which computes all Stokes parameters. That is, each ROACH board processes the polarization pair from a single beam of the receiver and computes the auto-correlation and cross-correlation products for that pair. To use this spectrometer with the multibeam system, 13 copies of this spectrometer are run in parallel, each on a separate ROACH board. In comparison to the MBCORR autocorrelation spectrometer (ACS⁸), HISPEC_400_8192 offers a factor of 6 increase in bandwidth while still achieving higher spectral resolution, vastly improved inter-channel isolation, and increased dynamic range from 8-bit sampling. A direct comparison to MBCORR is shown in Tab. 2.

Due to its increased instantaneous bandwidth, HISPEC can yield significantly faster survey speeds (a factor of 2-3 times) than MBCORR for wide-bandwidth 21-cm line surveys (i.e. >64 MHz). This will decrease the required observing time for 21-cm intensity mapping experiments as proposed by Li *et al.* (2012), and for spectral stacking such as that by Delhaize *et al.* (2012). Supporting such science projects was a key motivation for the HIPSR system.

3.2.2. Mid-bandwidth Spectroscopy

A 16384-channel, 200-MHz bandwidth mode (HISPEC_200_16384) for 21-cm observations was also developed. This mode is similar in functionality to HISPEC_400_8192, but halves the bandwidth and doubles the number of channels; this trade-off is required as there are limited resources within the FPGA. HISPEC_200_16384 does not compute cross terms between polarizations, so Stokes parameters are not computed.

All HIPSR modes digitize at a Nyquist rate of 800 Msamples/s. In HISPEC_200_16384, a half-band digital filter and complex mixer perform digital downconversion to select out 200 MHz of bandwidth, after which the 16384-channel PFB is applied. A comparison of HISPEC modes is shown in Tab. 2.

3.2.3. Noise Adding Radiometer Calibration

HISPEC employs noise adding radiometer (NAR) techniques to accurately measure system temperature (Brunzie, 1988). NAR techniques allow for greater calibration accuracy to be achieved, at the expense of increasing system temperature (increasing T_{sys} by 5-10%). In a NAR, a calibrated noise source is turned on and off at ~ 100 Hz to inject a known signal on top of the sky signal. Calibration is then achieved by monitoring the power difference between on and off states; this differential measurement is less susceptible to bandpass gain variations than an absolute power measurement.

In the 21-cm multibeam receiver, a calibrated noise source is injected after the orthomode transducer (part of the antenna feed); this noise source is controlled through the CCU. In HISPEC, a master ROACH is connected to the CCU, and all other ROACHes are synchronized to within one clock cycle (5ns) of the master through the distributed 1PPS. The HISPEC firmware on each ROACH is then able to compute two values: P_{on} , the total power of the signal when the noise source is switched on; and P_{off} , the total power

⁸see Price (2016) for a comparison of ACS and PFB spectrometer implementations.

Table 2. Comparison of HIPSR 21-cm line observing modes with MBCORR 64-MHz mode.

Specification	HISPEC	HISPEC	MBCORR
	400_8192	200_16384	64_1024
Bandwidth (MHz)	400	200	64
Sampling (bits)	8	8	3
Number of channels	8192	16384	1024
Spectral res. (kHz)	48.8	12.2	62.5
Velocity res. (km/s)	10.3	2.5	13.4
Implementation	PFB	PFB	ACS
– Number of taps	4	4	-
– Window function	Hamming	Hamming	-
Interchannel isolation	~50 dB	~50 dB	~6.6dB
Spectral products	XX*YY* XY*YX*	XX*YY*	XX*YY*
Integration length (s)	2-5	2-5	2-5

of the signal when the noise source is off. The relationship between system temperature T_{sys} and the noise source’s temperature T_C is then given by

$$T_{\text{sys}} = \frac{T_C}{\frac{P_{\text{on}}}{P_{\text{off}}} - 1}. \quad (1)$$

The value of T_C may be measured as required by comparison to astronomical calibration sources such as 1934-638 and Hydra A, which have well characterized flux models.

4. Results

4.1. System bandwidth

Fig. 3 shows example power spectra for an observation of calibrator source 0407-638 on 30 May 2014 using the two HISPEC modes. These tests used the central beam of the receiver and its corresponding analog signal chain. The analog chain performs signal conditioning to amplify, downmix and filter the signals to provide a suitable baseband signal (IF) to the digitizer; the analog chain mixes the receiver signal (RF) with a local oscillator (LO) and a sideband is extracted using analog filters with a 60-400 MHz passband. For these data, the LO was set to extract the lower sideband and as such the IF is reversed in frequency.

Several features are apparent in Fig. 3(a). The filter response of the HIPSR_200_16384 half-band filter can be seen, and the sharp cutoff of the analog chain’s 60 MHz highpass filter can be seen at the upper end of the HIPSR_400_8192 spectrum (IF is frequency reversed). A periodic ripple is apparent in both spectra, caused by standing waves between the dish surface and the focus. Several sources of radio interference are visible as spikes across the band (e.g. 1227 MHz and 1450 MHz). Fig. 3(b) shows a zoom-in on the galactic 21-cm line profile for the 0407-638 observation. The HIPSR_200_16384 spectrum resolves a double-peak in the line profile that cannot be seen in the HIPSR_400_8192 profile.

4.2. Radio interference

Compared to MBCORR, HIPSR has far superior interchannel isolation (~ 50 dB vs. ~ 6.6 dB between neighbouring channels). As a result, spectra are less affected by Gibbs ringing. A comparison between HIPSR and MBCORR’s response (before smoothing) is shown in Fig. 4. The significantly improved interchannel isolation of HISPEC allows edge features to be more accurately discerned. By applying a smoothing kernel to the MBCORR data, Gibbs ringing can be suppressed; however, this decreases spectral resolution. The HISPEC modes of operation do not require a smoothing kernel to be applied.

In the presence of strong RFI, clipping may occur at the digitizer, which severely degrades the entire spectra. As HIPSR employs 8-bit sampling (256 levels), the dynamic range of the digitizer is far greater than that of the 3-level MBCORR. Combined with the improved interchannel isolation, HIPSR is capable of

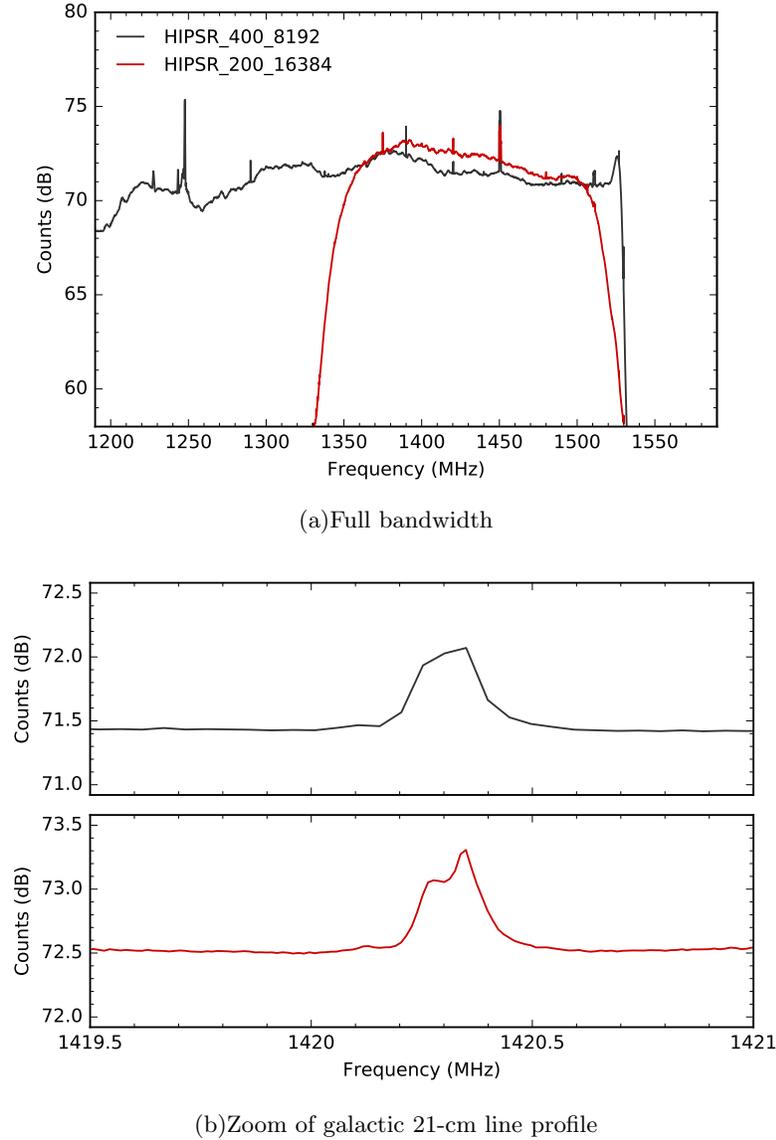


Fig. 3. Example spectra for 400 MHz (black) and 200 MHz (red) 21-cm operating modes. Data were taken sequentially during system testing on 30/05/2014, with the telescope pointed at the calibrator source 0407-638.

providing high-quality spectra in observing conditions with moderate amounts of RFI in which MBCORR cannot operate nominally.

4.3. Extragalactic HI

To illustrate the viability of the HIPSR system for HI surveys, this section presents an observation of a faint (~ 50 mJy) HI-massive galaxy, HIZOA J0836-43. This HI-massive disc galaxy lies in the Zone of Avoidance, at right ascension and declination ($8^h 36^m 51^s$, $-43^\circ 37' 41''$). It has a redshift $z = 0.036$ and correspondingly lies at a distance of 148 Mpc. It was first detected (unresolved) in the HI Zone of Avoidance (HIZOA) survey (Kraan-Korteweg *et al.*, 2005), and remains one of the most HI-massive galaxies detected to date (Donley *et al.*, 2006). The HIZOA survey was conducted using the Parkes multibeam receiver and MBCORR, and the original archival data is still readily available⁹. As such, it is a fitting source to test the HIPSR system.

⁹<http://www.atnf.csiro.au/research/multibeam/release/>

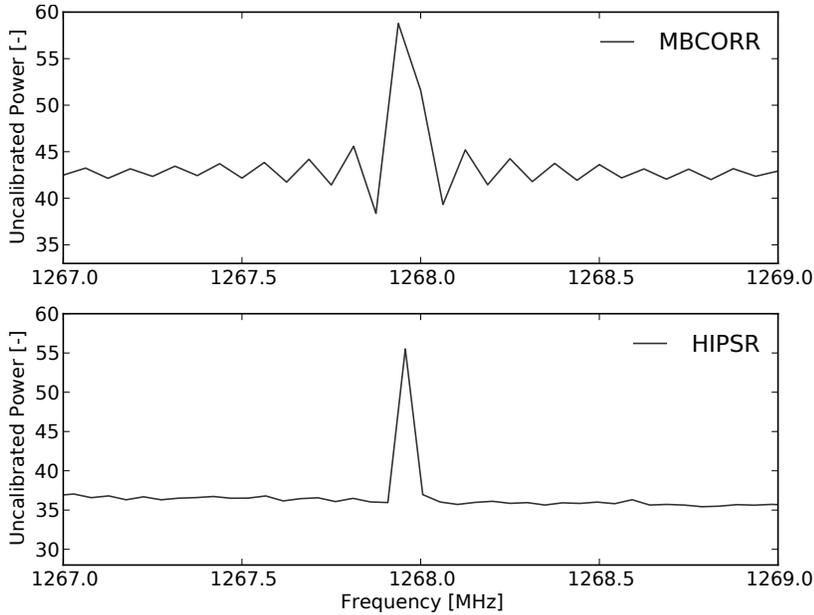


Fig. 4. Example of HIPSR and MBCORR response to narrowband RFI. The (unsmoothed) data output from MBCORR is visibly affected by Gibbs ringing.

The source was observed for 100 s in all 13 beams. The bandpass curve was removed by using position switching between on and off source pointings of each beam. Observations of Hydra A were used to further calibrate the data and to set the flux scale. The data from all 13 beams was then combined to form an overall spectrum.

In a final calibration step, the average power level of the featureless (flat) areas of the spectrum was computed and subtracted to bring the average to 0 Jy. The final calibrated HI profile of HIZOA J0836-43 is shown in Figure 5 and 6, along with archival data from the HIZOA catalogue. The peak flux of the HIPSR data is 55 mJy, while the HIZOA archival data has a peak flux of 47mJy. The noise level in HIPSR spectrum is 7.9 mJy, and the HIZOA spectrum exhibits a 7.85 mJy noise level. The coefficient of determination between the two lines is $R^2 = 0.74$, which indicates a high degree of correlation between the observations.

4.4. Pulsar Observations

As the high resolution spectrometer for both the High Time Resolution Universe (HTRU) survey and the ongoing Survey for Pulsars and Extragalactic Radio Bursts (SUPERB), the BPSR mode of HIPSR has been extensively tested in the field. BPSR data taken at Parkes after March 2012 uses the HIPSR-based system. Here we describe some of the initial commissioning observations that were performed to assess the performance of the backend system for pulsar survey experiments. For these tests, the channelized, detected spectra for both polarisations were de-dispersed and folded using DSPSR (van Straten & Bailes, 2011) to form pulse profiles presented here.

The first pulsar observation performed with the HIPSR backend was of the bright millisecond binary pulsar J0437–4715. This pulsar was observed with the primary beam of the multibeam receiver for a total of 770 seconds. Fig. 7 shows the pulse profile produced from this observation. BPSR was recording with a sampling interval of 64 μ s; therefore, the main peak of the pulsar, which has a full width at half maximum of around 140 μ s (Manchester *et al.*, 2013), is resolved with only a few time samples.

As a second test of HIPSR’s high time resolution spectrometer, the intermittent pulsar J0941–39 was observed. In Fig. 8, a single bright pulse is shown. The bottom panel shows the dispersed pulse which has been smeared over about 100 ms. The top panel shows the pulse after the effects of dispersion have been removed. The intrinsic width of the pulse is about 4 ms. Pulses from an intermittent pulsar, rotating radio transient (RRAT; McLaughlin *et al.*, 2006) or FRB are detected in real time using Heimdall. Fig. 9 shows

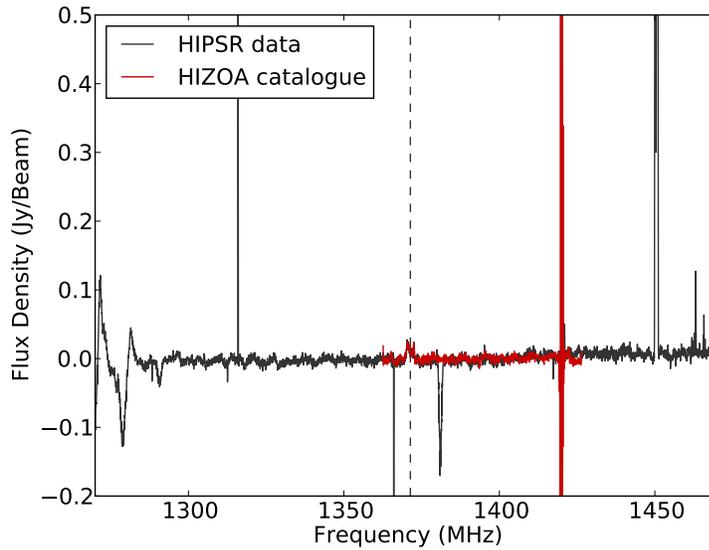


Fig. 5. Calibrated HIPSr data with HIZOA archival data overlaid.

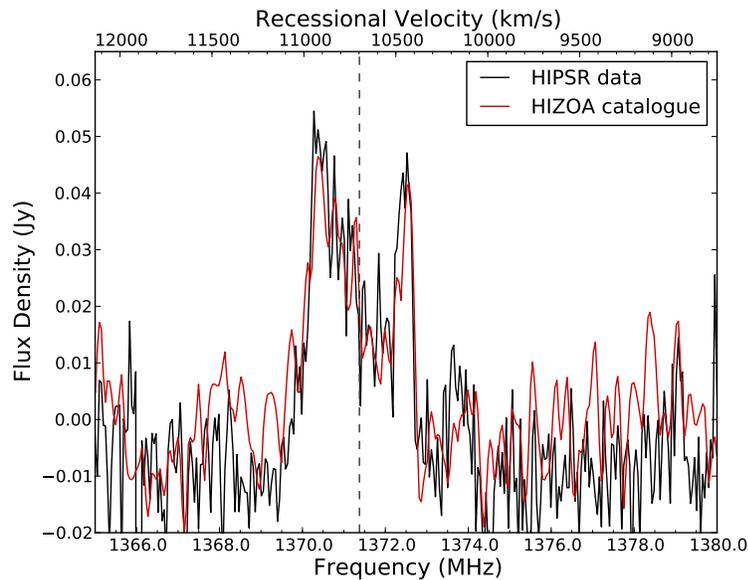


Fig. 6. HIPSr first light observations of HIZOA J0836-43, showing HI profile.

a rotating radio transient (RRAT; [McLaughlin et al., 2006](#)) detected in beam 01 of the multibeam receiver; plots like this are part of the real-time feedback presented to the observer.

5. Conclusions and future outlook

HIPSr is a multi-purpose digital signal processing system for the Parkes 64-m telescope's 21-cm multibeam receiver; it provides a unified, multi-purpose DSP backend. HIPSr was installed at Parkes over 2011-2012, and has been in use since. As of 2016, the MBCORR backend was decommissioned, leaving HIPSr as the only digital backend for the 21-cm multibeam receiver. In the last quarter of 2016, the GP-GPU servers of HIPSr will be removed, in preparation for a future upgrade; this will mean high-time resolution modes are inoperable until a replacement GP-GPU backend is installed. The FPGA frontend and Ethernet switches

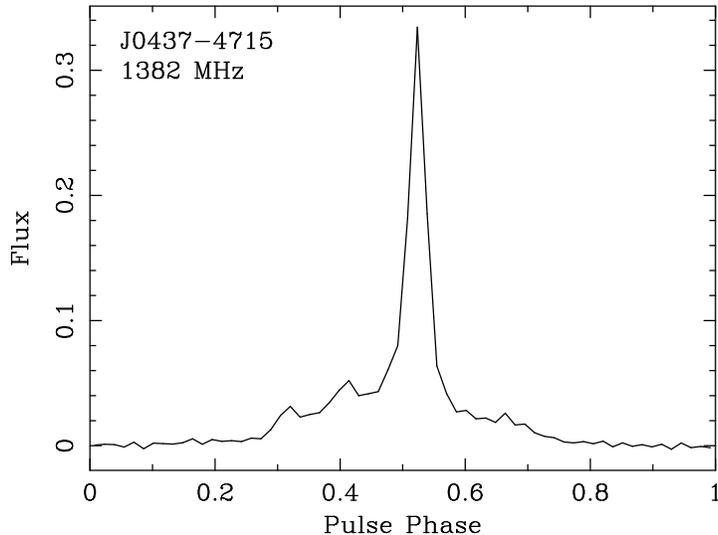


Fig. 7. Uncalibrated pulse profile of J0437-4715 integrated for 770 seconds, observed with HIPSr during commissioning.

will remain, and wideband 21-cm functionality will continue to be supported.

Nevertheless, there is motivation for a full replacement of HIPSr. Since installation, the CX4 10 GbE Ethernet standard has been superseded by SFP+, and 40 GbE over QSFP+ has become common. The newer CASPER ROACH2 and SNAP FPGA boards (Hickish *et al.*, [this issue](#)) use the SFP+ standard, and retains support for the iADC digitizer cards. The FPGA firmware could be ported to these platforms in a straightforward manner, so these FPGA boards are a potential avenue for future upgrades. Similarly, the GP-GPU server nodes could be replaced with current-generation equivalents. Many Ethernet switches support mixed 10 and 40 GbE, meaning fewer GP-GPU nodes could be used, or a larger fraction of bandwidth could be processed.

The most compelling motivation for an upgrade (or replacement) of HIPSr is to capture and process the entire 400 MHz bandwidth from all 26 voltage streams. Also compelling is the implementation of real-time RFI identification and excision algorithms — for example, those described by Nita *et al.* (2007) and Kocz *et al.* (2010) — decreasing the amount of data lost to interference.

An alternative approach to increasing Parkes’ L-band science capability is to install a new multi-pixel feed. Recent tests of the ASKAP Mark-II phased array feed (PAF) on Parkes (Chippendale *et al.*, 2016), have shown that PAFs are a viable technology for large single-dish telescope. An ultra-wideband receiver, spanning 0.7-4.0 GHz is currently under development for Parkes (Manchester, 2015), and will require a DSP backend. A unified digital backend — similar in architecture to HIPSr — is a potential solution for maximizing science capability at Parkes while minimizing engineering time and development costs.

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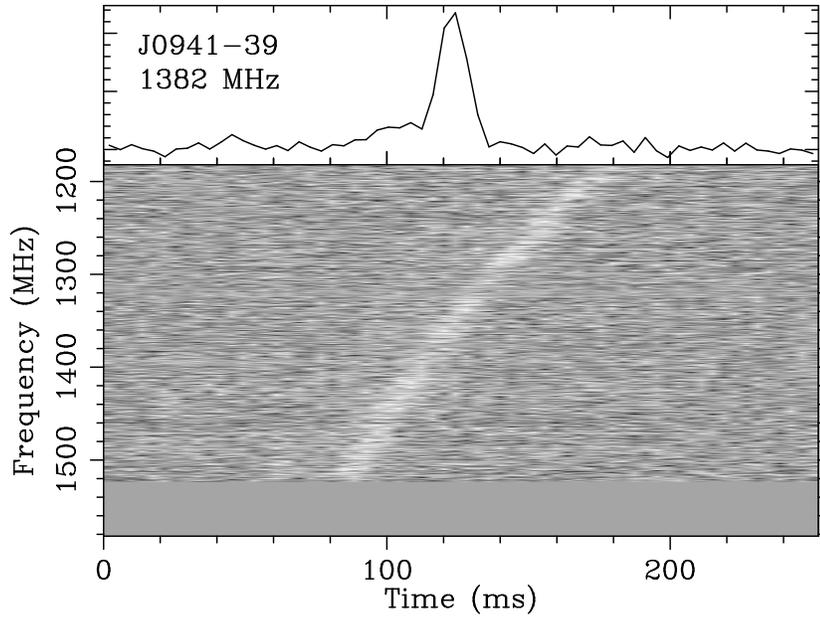


Fig. 8. Single pulse from J0941-39.

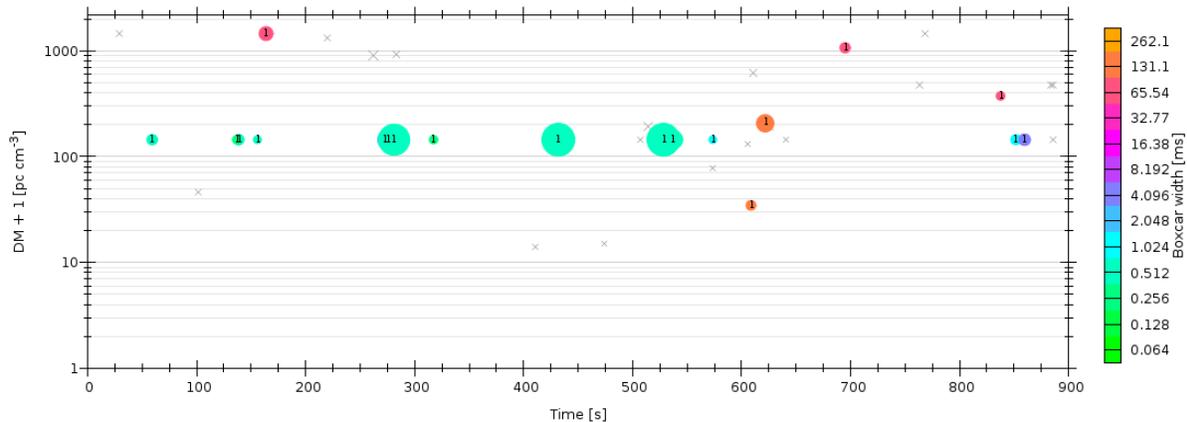


Fig. 9. Detection of single pulses from J0837-24, an RRAT with DM of 142.8 in a 900 second observation using HIPSr. The size of each dot is proportional to the Signal to Noise Ratio (SNR) of the pulse.

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