Design of Power Stage of INAF GAIA Board for biasing of AETHRA WP1 downconverter

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Abstract

The GAIA digital board developed by INAF was designed to bias up to ten stages of cryogenic low noise amplifiers (LNAs) and to deliver a maximum drain current $I_{dmax} \leq 50$ mA with a drain voltage $V_{dmax} \leq 5$ V for each of them. The GAIA board monitors and controls each of the stages independently. However, such board cannot be employed to monitor and control the AETHRA WP1 75-116 GHz downconverter module as the power amplifiers of the fully-integrated MMIC developed at IAF, integrated into the downconverter module, require current values of up to 300 mA each, that is six times greater than what GAIA can deliver. Therefore, a power stage of the GAIA board has to be developed to comply with the high-current bias requirements of the AETHRA WP1 downconverter. Here, we describe the design of the power stage of the GAIA board, named PSG (Power Stage Gaia). The PSG is a four-layer digital bias board, to be connected in series with GAIA, capable of delivering up to 10 × high-current stages. One GAIA board is used to monitor and control one PSG board. The latter is an extension of GAIA and cannot be used independently of it. Therefore, one GAIA board plus one PSG board must be used in conjunction to monitor and control up to 10 high-current stages of the AETHRA WP1 downconverter. The version 1.2 of the GAIA board, developed for biasing, monitoring and controlling of the LNAs, cannot be used in conjunction with the PSG but requires a small modification to allow data interchange between the two boards. A new GAIA board, version 1.5, must be used in conjunction with the PSG.

This document describes the main specifications of the GAIA bias board version 1.2, the requirements and design of the PSG as well as the upgraded GAIA version 1.5. In Section 1 we summarize the specifications of the GAIA board, version 1.2 (current version). The PSG is described in Section 2, while Section 3 reports on the upgrade of the GAIA board (version 1.5) for use with the PSG.

1. GAIA bias board

The GAIA board developed by INAF is a four-layer rack-mountable programmable digital bias board based on a microcontroller (Atmel ATMega2560) and on digital potentiometers (Analog Device AD5231) designed for remote monitor and control of the gate voltages V_g and of the drain voltages V_d of cryogenic Low Noise Amplifier (LNA) modules. One single Gaia board can control up to 10 × V_d and 10 × V_g and monitor 10 × V_d, 10 × V_g and 10 drain currents, 10 × I_d. The I_d of each LNA module amplification stage is imposed by the assigned V_d and V_g. One GAIA board can bias 10 independent cryogenic LNA modules (10 independent channels) in case each module requires one V_d and one V_g. The digital board is designed to provide high bias voltage stability and proved to generate very low RFI emission, as required for radio astronomy purposes. The

procedure for setting up the bias voltages to their goal values, when switching on the LNAs, is reached incrementally from the zero-volt condition and is coded in the microcontroller firmware. The inverse procedure is applied when switching off. The same board includes analogue to digital converters (LTC2495) for remotely monitoring V_d, V_g and I_d for each of the 10 channels. Table 1 shows the main electrical specifications of GAIA.

A photo of the GAIA board is shown in Figure 1. A monitor and control software for the GAIA board was developed to allow setting and monitoring the 10 different drain and gate channels. The GUI (Graphical User Interface) is shown in Figure 2. The GUI allows to set the values for all V_d and all V_g voltages. Furthermore, the GUI allows to calibrate out the resistances of the DC cables connecting the LNA to the GAIA board (in case the resistances are set to 0 Ω, there will be a small error in the measured voltages): R_{cable} indicates the "hot" terminal (either V_d or V_g), while R_{ground} is a single ground cable. "Drain" and "Gate" indicate the step potentiometer value, ranging from 1 to 1024, allowing to set the voltage as follows:

a) "Drain": 1 to 1024 are associated, respectively to the minimum and maximum values of the drain voltage (1 corresponding to 0 V, 1024 corresponding to +5 V);
b) "Gate": 1 to 1024 are associated, respectively to the minimum and maximum values of the gate voltage (1 corresponding to -6.5 V, 1024 corresponding to +5 V).

Item	Values
N. of amplification stages	10 (10 × V_d and 10 × V_g)
Drain voltage range	0 V ≤V_d≤ 5 V
Gate voltage range	-6.5 V ≤V_g≤ 5 V
Maximum drain current	I_{dmax}≤ 50 mA (per channel)
Current consumption +/-10V	≈327mA
Current consumption 5V_TTL	≈191mA
Max total power consumption	≈7.5 W (≈3.75 W for GAIA board + ≈3.75 W for LNA load)
ADC characteristics	16 bit with ≈15 Hz sampling rate
Voltage resolution setting	≈5 mV
Communication port	Auto-negotiated 100 Mb LAN with RJ45 connector
Board size (without front panel)	h=100 mm, depth=160 mm

Table 1:Main specification of the GAIA digital LNA bias board.

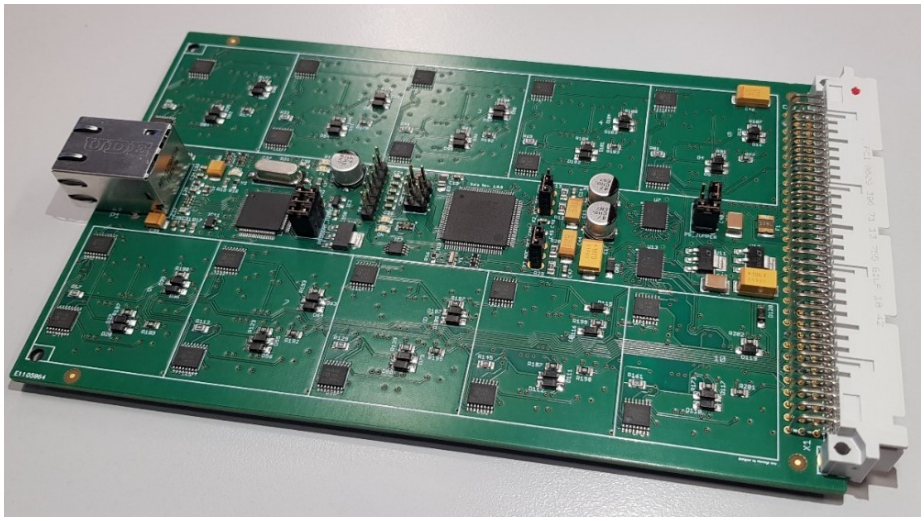

Figure 1: Photo of the GAIA bias board, version 1.2.

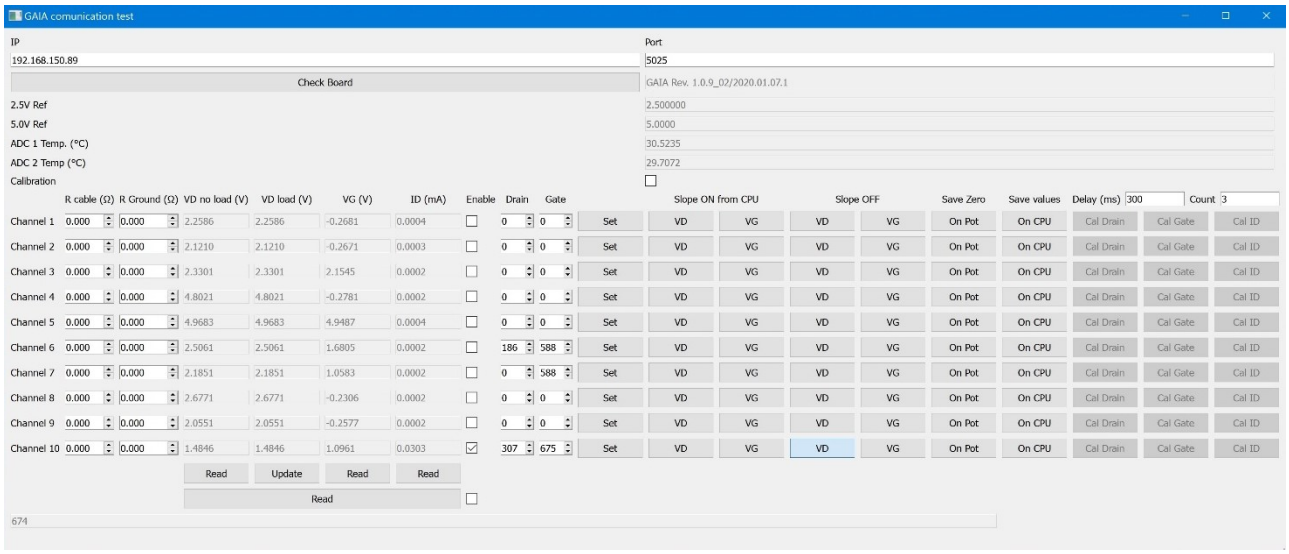

Figure 2: Graphical User Interface of the GAIA board showing the monitor and control of the 10 channels.

GAIA adopts a DIN 41612 male connector mounted on-board (Mouser code 649-8693967137E1LF). The pinout of the GAIA 1.2 version is provided in Table 2.

PIN	Function	PIN	Function
A1	+10 VDC	**C1**	+10 VDC
A2	N.C.	**C2**	N.C
A3	+10 VDC	**C3**	+10 VDC
A4	N.C.	**C4**	N.C.
A5	-10 VDC	**C5**	-10 VDC
A6	N.C.	**C6**	N.C.
A7	-10 VDC	**C7**	-10 VDC
A8	N.C.	**C8**	N.C.
A9	+5V TTL	**C9**	+5V TTL
A10	N.C.	**C10**	N.C.
A11	GND	**C11**	GND
A12	N.C.	**C12**	N.C.
A13	N.C.	**C13**	N.C.
A15	N.C.	**C15**	N.C.
A15	N.C.	**C15**	N.C.
A16	N.C.	**C16**	N.C.
A17	GND	**C17**	N.C.
A18	VD_1	**C18**	VG_1
A19	VD_2	**C19**	VG_2
A20	VD_3	**C20**	VG_3
A21	VD_4	**C21**	VG_4
A22	VD_5	**C22**	VG_5
A23	N.C.	**C23**	GND
A24	GND	**C24**	N.C.
A25	VD_6	**C25**	VG_6
A26	VD_7	**C26**	VG_7
A27	VD_8	**C27**	VG_8
A28	VD_9	**C28**	VG_9
A29	VD_10	**C29**	VG_10
A30	N.C.	**C30**	GND
A31	GND	**C31**	N.C.
A32	GND	**C32**	N.C.

Table 2: Pinout of DIN41612 connector of GAIA version 1.2.

A female DIN 41612 connector (Mouser code 649-869396814755V1LF) must be adopted to connect GAIA to a backplane. The bias voltages are a +5V for the digital logic and a +/-10 V for the analogue part of the bias circuitry. For low-noise radio astronomy purposes, it is strongly suggested that GAIA is biased by a linear power supply (not a switching power supply) to mitigate RFI emissions. Examples of recommended power supplies are the PSM212 and PSM205 from Schroff Pentair.

The GAIA bias board was successfully used for biasing the W-band cryogenic low noise amplifiers during AETHRA WP1 tests performed at IRAM Grenoble, in January 2020. A report on the tests performed at IRAM is in preparation.

The GAIA board version 1.2 requires a simple upgrade in order to be compatible with the Power Stage GAIA board (PSG) described in the following Section 2. The GAIA board performs the monitor and control of the PSG. Section 3 describes the upgrade GAIA board version 1.5, which is compatible for operation with the PSG.

2. Power Stage of the GAIA board (PSG)

The GAIA board can deliver a maximum drain current of I_d=50 mA, with a drain voltage V_d=5 V (see Table 1), resulting in a maximum power consumption of 250 mW for each of the 10 channels (max. 2.5 W for the ten-channel GAIA board). With these maximum drain current values, the board is suitable to set the I_d currents of most of cryogenic LNA modules at their optimum bias for which it was designed, as required for low noise operations. However, the downconverter module developed for AETHRA WP1 requires current values to be delivered to the circuitries beyond the limits that the GAIA can provide. A schematic diagram of the AETHRA WP1 downconverter, shown in Figure 3 and Figure 4, provides the estimated current requirements of the main components:

- power amplifier PA1: V_{d2}=1.2 V with I_{d2}=250 mA;
- power amplifier PA2: V_{d3}=1.4 V with I_{d3}=300 mA;

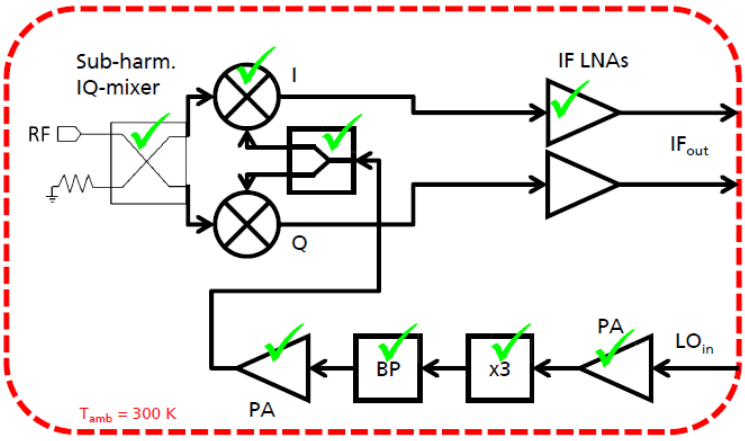

Figure 3: Schematic diagram of the fully integrated MMIC downconverter for AETHRA WP1 (75-116 GHz) designed at IAF showing the main sub-circuitries: RF hybrid, sub-harmonic mixers, IF LNAs, LO chain with power amplifiers and frequency multiplier.

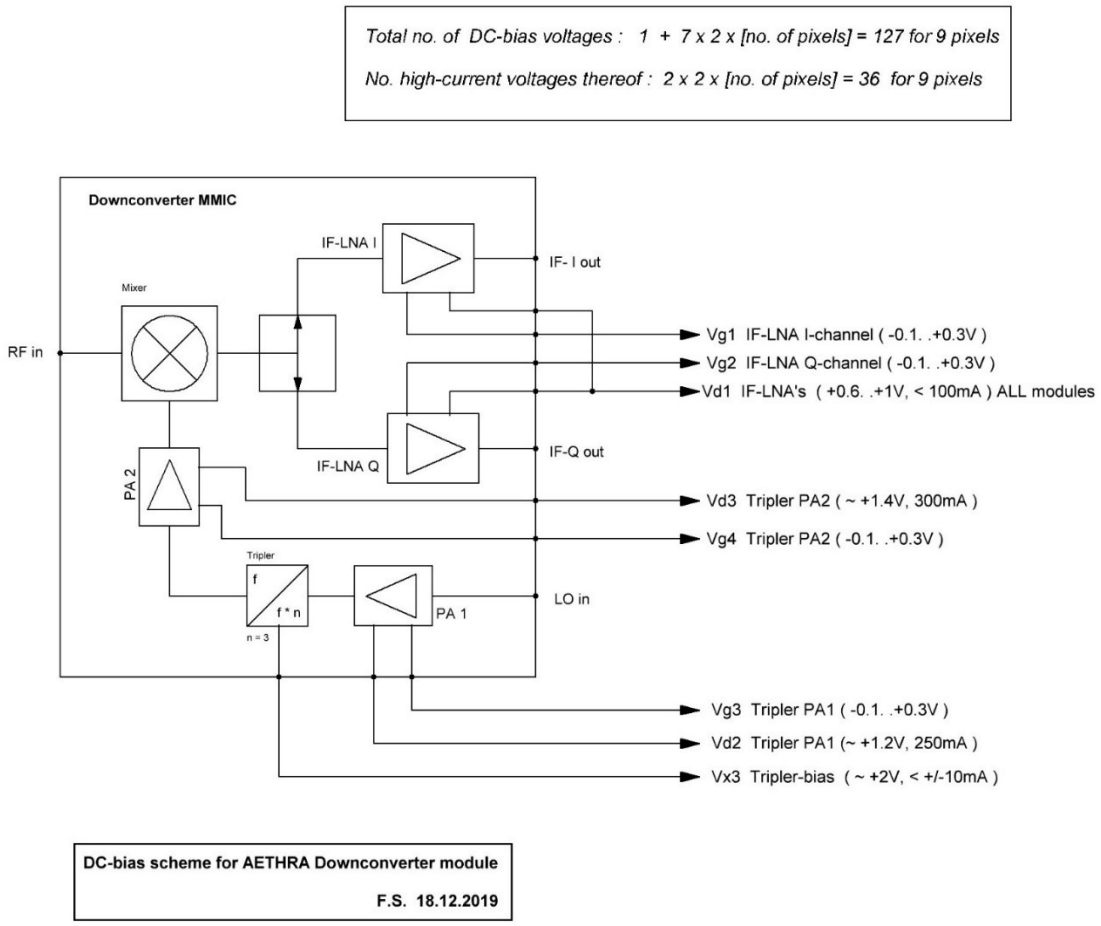

Figure 4: Schematic diagram of AETHRA WP1 downconverter.

Based on the above requirements, we decided to develop a power stage of the GAIA board capable of delivering a voltage of up to V_d=5 V with current I_d up to 500 mA for each of 10 possible channels, as listed in the specification Table 3. We assumed that the gate currents are negligible compared to the drain currents, therefore the I_g are not monitored (neither for GAIA nor for the PSG). The gate currents do not transit from the PSG, but are extracted directly from the GAIA board. A block diagram of the PSG, showing its possible interconnection to the GAIA board, is shown in Figure 5. Views of the PSG and GAIA boards are shown in Figure 6. The PSG main components are 10 power amplifiers (PAs), 10 current sensors, two Analog-to-Digital Converters (ADCs) and one driver, managed by I^2C bus. The components are mounted on a 100 mm ×160 mm Eurocard board with size identical to GAIA.

We note that the I_d drain currents from the GAIA board outputs to the power amplifier (PA) input of the PSG, being the PA an operational amplifier with very high input impedance, is close to zero (of order of µA). Referring to Figure 5, the V_{D1}, V_{D2} … V_{D10} of the PSG are monitored and controlled by the GAIA board. The currents at the output of the Power Amplifiers PA_1, PA_2 … PA_{10} (in buffer configuration) are monitored by current sensors based on INA225 from Texas Instruments. The INA225 is a voltage-output and current-sense amplifier. The device measures the differential voltage developed across a resistor when current flows through it. This resistor is commonly referred to as a current-sensing resistor or a current-shunt resistor. The output of this sensor is coupled back to the Analog to Digital Converter (LTC2495 from Linear Technology). The voltage feedback is extracted at the output of the current sensor to allow direct measurements of the

load voltage (in our case the AETHRA WP1 downconverter), thus minimizing the measurements error. The voltage feedback is obtained by coupling the output voltage back to the input of the ADC. Each of the Power Amplifiers of the PSG can be enabled or disabled by the driver TCA9555 (from Texas Instruments). The driver can pull up or down the pin voltage of each of the PAs. The main components of the PSG are listed in Table 4. Images of the PSG board design are shown in Figure 7. The four metallization layers of the PSG are shown in Figure 8.

Item	Values
N. of amplification stages	10 × V_d
Drain voltage range	0 V ≤V_d≤ 5 V
Maximum drain current	I_{dmax}≤ 500 mA (per channel)
Max total power consumption	≈50 W (≈25 W for PSG board + ≈25 W for downconverter load)
ADC characteristics	16 bit with ≈15 Hz sampling rate
Voltage resolution setting	≈5 mV
Communication port	Serial port I²C for communication with GAIA board
Board size (without front panel)	h=100 mm, depth=160 mm

Table 3: Main specifications of the PSG (power stage of GAIA board).

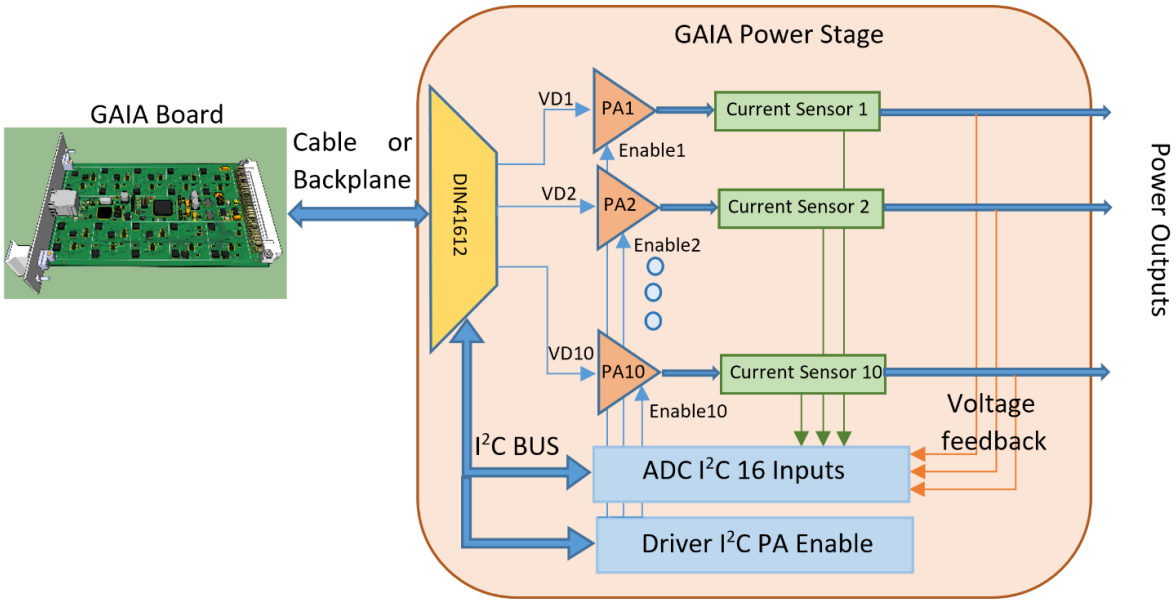

Figure 5: Block diagram of the PSG (GAIA Power Stage, shown on the right) and connection to the GAIA board (shown on the left) through a cable of backplane (to be located on a 19-inch rack).

Component	**Model and manufacturer**
Driver I²C PA Enable	TCA9555 from Texas Instruments
ADC I²C Inputs	LTC2495 from Linear Technology
Current Sensor	INA225 from Texas Instruments
Power Amplifier	LT1970 from Linear Technology

Table 4: List of main components of the PSG board.

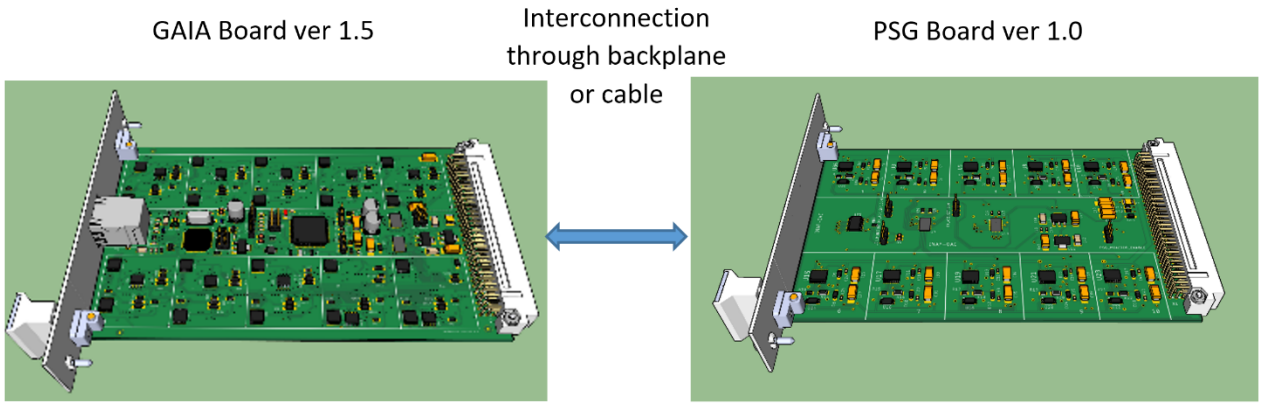

Figure 6: 3D views of the PSG board ver. 1.0 (shown on the right) and of the GAIA Board ver. 1.5 (shown on the left). The two boards can be connected through either a cable or a backplane board (to be located on a 19-inch rack).

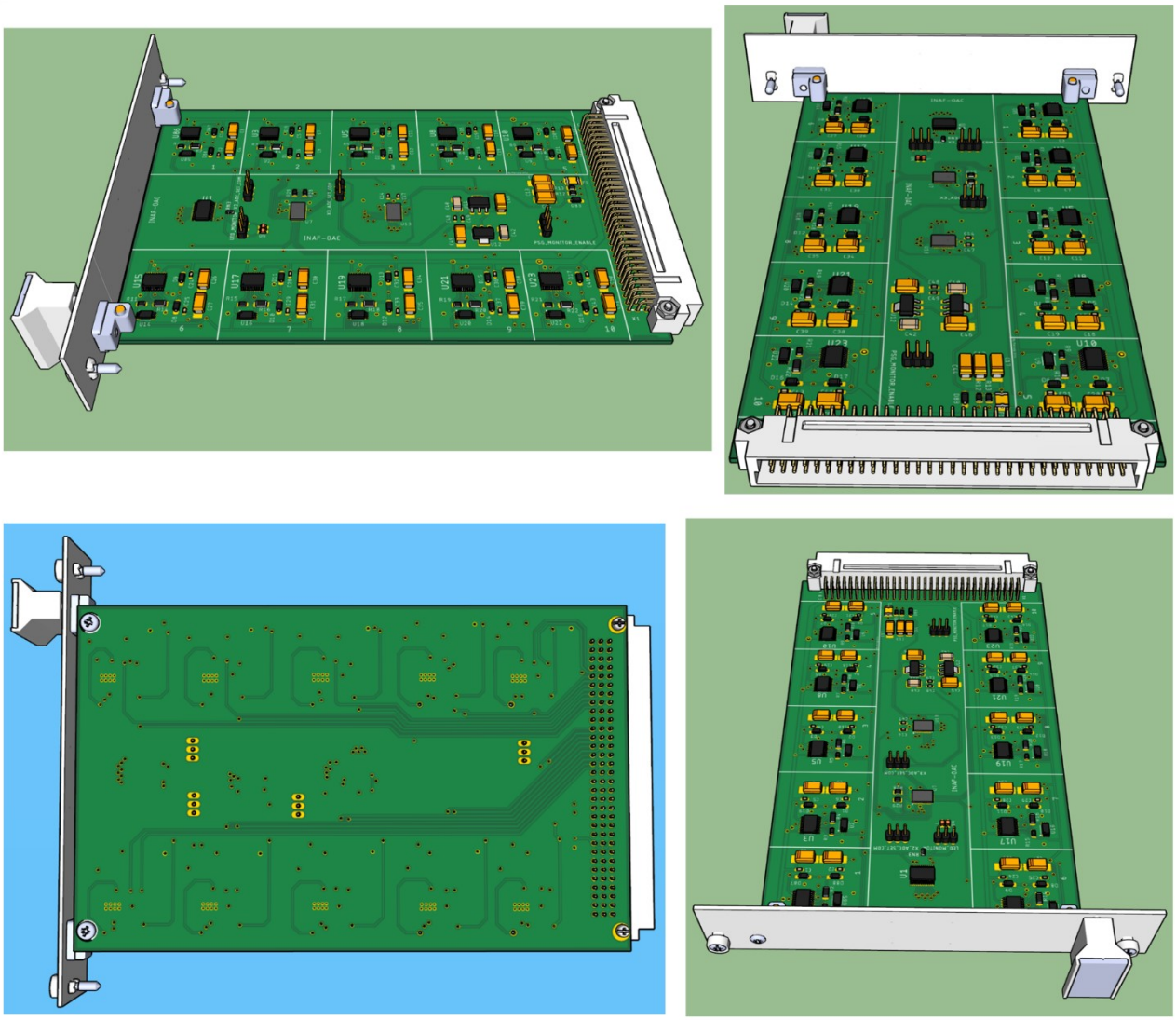

Figure 7: 3D drawings of the PSG board version 1.0 designed by INAF.

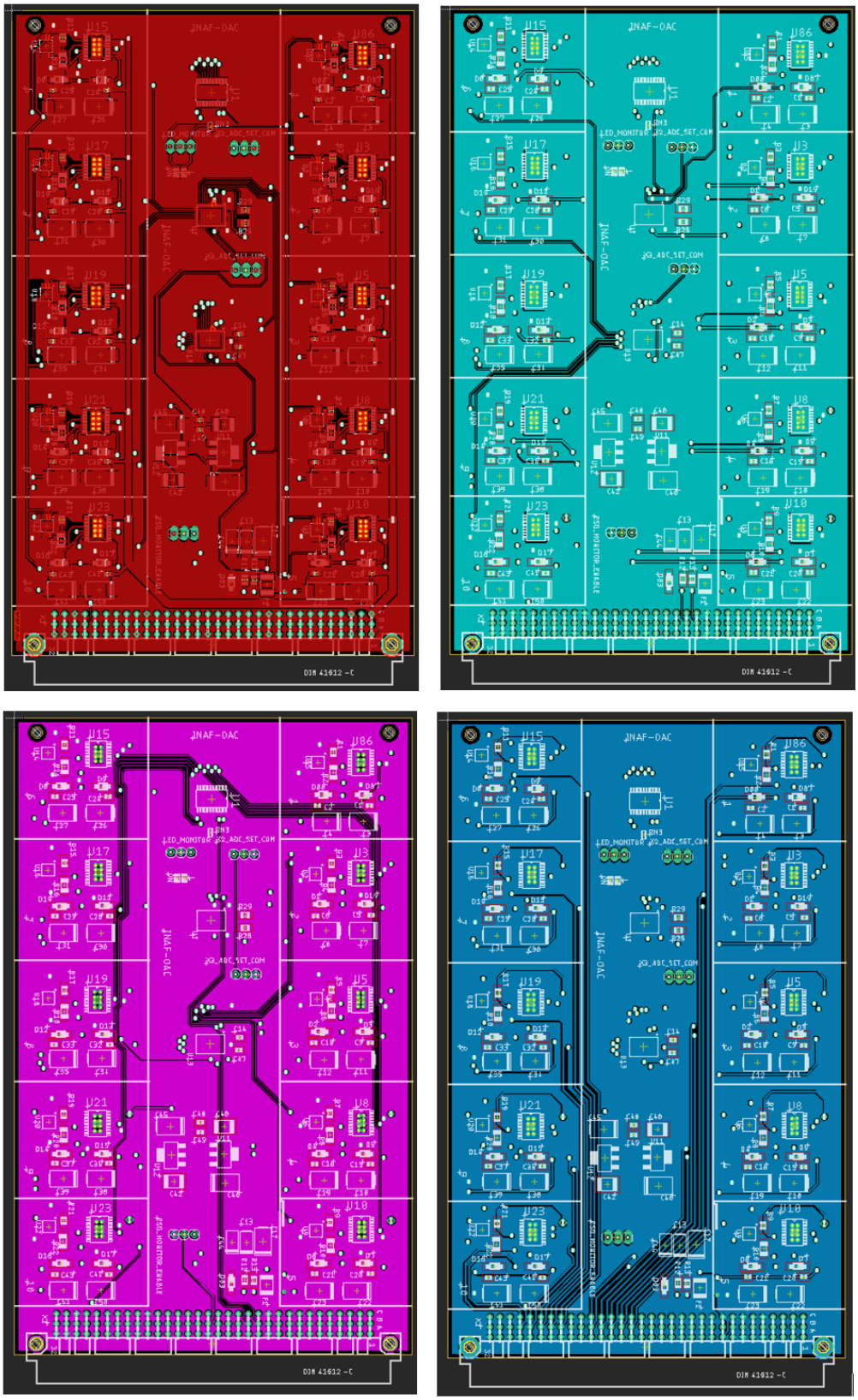

Figure 8: View of the four metallization layers of the PSG board. PSG top layer (red) shown in top left. PSG second layer (light blue) shown in top right. PSG third layer (purple) shown in bottom left. PSG bottom layer (dark blue) shown in bottom right.

The pinout of the DIN41612 connector of the PSG is listed in Table 5. The input of the drain voltages (VD_x) are in column C (PIN numbers C18-C22 and C25-C29). The output of the drain voltages (VDP_MON_x) are in columns A (PIN numbers A18-A22 and A25-A29).

PIN	Function	PIN	Function	PIN	Function
A1	+10 VDC	**B1**	N.C.	**C1**	+10 VDC
A2	N.C.	**B2**	N.C.	**C2**	N.C
A3	+10 VDC	**B3**	N.C.	**C3**	+10 VDC
A4	N.C.	**B4**	N.C.	**C4**	N.C.
A5	-10 VDC	**B5**	N.C.	**C5**	-10 VDC
A6	N.C.	**B6**	N.C.	**C6**	N.C.
A7	-10 VDC	**B7**	N.C.	**C7**	-10 VDC
A8	N.C.	**B8**	N.C.	**C8**	N.C.
A9	+5V TTL	**B9**	N.C.	**C9**	+5V TTL
A10	N.C.	**B10**	N.C.	**C10**	N.C.
A11	GND	**B11**	N.C.	**C11**	GND
A12	N.C.	**B12**	SDA	**C12**	N.C.
A13	N.C.	**B13**	SCL	**C13**	N.C.
A15	N.C.	**B14**	N.C.	**C15**	N.C.
A15	N.C.	**B15**	N.C.	**C15**	N.C.
A16	N.C.	**B16**	N.C.	**C16**	N.C.
A17	GND	**B17**	PSG_MONITOR	**C17**	N.C.
A18	VDP_MON_1	**B18**	N.C.	**C18**	VD_1
A19	VDP_MON_2	**B19**	N.C.	**C19**	VD_2
A20	VDP_MON_3	**B20**	N.C.	**C20**	VD_3
A21	VDP_MON_4	**B21**	N.C.	**C21**	VD_4
A22	VDP_MON_5	**B22**	N.C.	**C22**	VD_5
A23	N.C.	**B23**	N.C.	**C23**	GND
A24	GND	**B24**	N.C.	**C24**	N.C.
A25	VDP_MON_6	**B25**	N.C.	**C25**	VD_6
A26	VDP_MON_7	**B26**	N.C.	**C26**	VD_7
A27	VDP_MON_8	**B27**	N.C.	**C27**	VD_8
A28	VDP_MON_9	**B28**	N.C.	**C28**	VD_9
A29	VDP_MON_10	**B29**	N.C.	**C29**	VD_10
A30	N.C.	**B30**	N.C.	**C30**	GND
A31	GND	**B31**	N.C.	**C31**	N.C.
A32	GND	**B32**	N.C.	**C32**	N.C.

Table 5: Pinout of the PSG (Power Stage of Gaia bord).

3. Upgrade of GAIA for use with the PSG

The GAIA board version 1.2 cannot be employed with the PSG. A small modification of the GAIA board, an upgraded version 1.5, is necessary to allow communication with the PSG and monitoring of the currents and voltages delivered by the PSG current sensors and voltage feedbacks. These values are sampled by the ADC and sent back to GAIA through a I^2C digital communication protocol. The enabling and disabling of the PAs is also controlled by the digital driver using the same digital serial bus. The new GAIA board version 1.5 replaces in all specifications the older 1.2 version and can be used also for biasing the AETHRA WP1 cryogenic LNAs.

The pinout of the upgraded version 1.5 of GAIA is listed in Table 6. The red coloured values refer to the new functions. The PSG_MONITOR function is used to read if the PSG board is connected (in the backplane or through DC cables) with GAIA.

PIN	Function	PIN	Function	PIN	Function
A1	+10 VDC	**B1**	N.C.	**C1**	+10 VDC
A2	N.C.	**B2**	N.C.	**C2**	N.C
A3	+10 VDC	**B3**	N.C.	**C3**	+10 VDC
A4	N.C.	**B4**	N.C.	**C4**	N.C.
A5	-10 VDC	**B5**	N.C.	**C5**	-10 VDC
A6	N.C.	**B6**	N.C.	**C6**	N.C.
A7	-10 VDC	**B7**	N.C.	**C7**	-10 VDC
A8	N.C.	**B8**	N.C.	**C8**	N.C.
A9	+5V TTL	**B9**	N.C.	**C9**	+5V TTL
A10	N.C.	**B10**	N.C.	**C10**	N.C.
A11	GND	**B11**	N.C.	**C11**	GND
A12	N.C.	**B12**	SDA	**C12**	N.C.
A13	N.C.	**B13**	SCL	**C13**	N.C.
A15	N.C.	**B14**	N.C.	**C15**	N.C.
A15	N.C.	**B15**	N.C.	**C15**	N.C.
A16	N.C.	**B16**	N.C.	**C16**	N.C.
A17	GND	**B17**	PSG_MONITOR	**C17**	N.C.
A18	VD_1	**B18**	N.C.	**C18**	VG_1
A19	VD_2	**B19**	N.C.	**C19**	VG_2
A20	VD_3	**B20**	N.C.	**C20**	VG_3
A21	VD_4	**B21**	N.C.	**C21**	VG_4
A22	VD_5	**B22**	N.C.	**C22**	VG_5
A23	N.C.	**B23**	N.C.	**C23**	GND
A24	GND	**B24**	N.C.	**C24**	N.C.
A25	VD_6	**B25**	N.C.	**C25**	VG_6
A26	VD_7	**B26**	N.C.	**C26**	VG_7
A27	VD_8	**B27**	N.C.	**C27**	VG_8
A28	VD_9	**B28**	N.C.	**C28**	VG_9
A29	VD_10	**B29**	N.C.	**C29**	VG_10
A30	N.C.	**B30**	N.C.	**C30**	GND
A31	GND	**B31**	N.C.	**C31**	N.C.
A32	GND	**B32**	N.C.	**C32**	N.C.

Table 6: Pinout of DIN41612 connector of GAIA version 1.5.

Table 7 shows an example of the BOM of the PSG components. Further details, including the full BOM, Gerbers and Pick&Place files are provided separately for both the PSG version 1.0 and GAIA version 1.5 boards.

Qty	Value	Device	Package	Parts	Description	AVAILABILI	DESCRIPTI	DIGI-KEY_F	DIGI-KEY_F	MF	MOUSER
24	100n	C-EUC0603	C0603	C1, C2, C5,	CAPACITOR, European symbol						80-C0603X104K5R3316
21	100u tanta	CPOL-EUD,	D/7343-31	C3, C4, C7,	POLARIZED CAPACITOR, European symbol						80-T510X107K020ATA45
2	10u 25V	CPOL-EUC,	C/6032-28	C13, C44	POLARIZED CAPACITOR, European symbol						80-T491C106K25AT7280
1	10u 35V ta	CPOL-EUD,	D/7343-31	C45	POLARIZED CAPACITOR, European symbol						80-T495D106M35ATE260
1	1k	4R-N0402/	4X0402AR\	RN3	Array Chip Resistor						667-EXB-28V102JX
2	1uF	C-EUC1812	C1812	C40, C42	CAPACITOR, European symbol						80-C1812C105J1RACTU
4	2.7K	R-EU_M08	M0805	R12, R13, F	RESISTOR, European symbol						667-ERJ-PB6B2701V
10	200m 1%	R-EU_R08(	R0805	R1, R3, R5,	RESISTOR, European symbol						667-ERJ-6DSFR20V
1	22u 35V ta	CPOL-EUD,	D/7343-31	C46	POLARIZED CAPACITOR, European symbol						80-T495X226K35ATE300
10	800m 1%	R-EU_R12(	R1206	R2, R4, R6,	RESISTOR, European symbol						603-RL1206FR-070R8L
1	GREEN	LEDCHIP-LI	CHIP-LED0	ON	LED						645-599-0160-007F
4	HARWIN M	PT31X03	1X03	LED_MONI	PHOENIX CONNECTOR						855-M20-9990346
10	INA225	INA225	SOP65P49(	U2, U4, U6, U9, U14, U16, U18, U20, U22, U85							595-INA225AIDGKT
1	KDZTFTR5.	MBR0520L	SOD123	D83	SCHOTTKY BARRIER RECTIFIER						755-KDZTFTR5.6B
1	LT1117CST	LT1117CST	SOT223	U12							584-LT1117CST-5#PBF
1	LT1118CST	LT1118CST	SOT223	U11							584-LT1118CST-2.5PBF
10	LT1970CFE	LT1970CFE	SOP65P64(	U3, U5, U8	Op Amp		Op Amp Si	LT1970CFE	https://ww	Analog Dev	584-LT1970CFE#PBF
2	LTC2495QI	LTC2495QI	QFN50P50	U7, U13							584-LTC2495IUHF#PBF
1	MABC96LP	MABC96LP	MABC96LP	X1	CONNECTOR male, 96 pins, type C, rows ABC, grid 2.54 mm with m						649-8693967137E1LF
20	MBR0520L	MBR0520L	SOD123	D1, D2, D3	SCHOTTKY BARRIER RECTIFIER						863-MBR0520LT1G
1	MF-MSMF	L-EUL1812	L1812	F1	INDUCTOR, European symbol						652-MF-MSMF050-2
1	TCA9555PI	TCA9555PI	SOP65P64(	U1	I/O EXPAN	Good	1.65 to 5.5V 16-Bit I2C and SMBu			Texas Instr	595-TCA9555PWR
1	YELLOW	LEDCHIP-LI	CHIP-LED0	L	LED						645-599-0160-007F

Table 7: Example of Bill of Material (BOM) of the PSG.