Resistive Switching in Microscale Anodic Titanium Dioxide-Based Memristors

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Abstract

The potentiality of anodic TiO_2 as an oxide material for the realization of resistive switching memory cells has been explored in this paper. Cu/anodic-TiO_2/Ti memristors of different sizes, ranging from 1 × 1 μm^2 to 10 × 10 μm^2 have been fabricated and characterized. The oxide films were grown by anodizing Ti films, using three different process conditions. Measured I–V curves have shown similar asymmetric bipolar hysteresis behaviors in all the tested devices, with a gradual switching from the high resistance state to the low resistance state and vice versa, and a R_{OFF}/R_{ON} ratio of 80 for the thickest oxide film devices.

Keywords: Memristor, RRAM, Resistive switching, rectifying behavior, Anodizing, TiO_2.

1. Introduction

Memristors are metal/insulator/metal devices whose resistance can be varied by applying an electrical field between the two metal contacts. The fingerprint of this behavior is visible through a non linear current-voltage characteristic which is normally represented by an hysteresis loop [1–3]. This property allows memristors to be employed as non volatile memory devices as well as resistive random access memories (RRAMs) [4]. Moreover, the capability of memristors to sustain multiple resistive states can be also exploited for realizing multi-level memories, programmable analog circuits and neuromorphic logic elements [2], [5]. Because of their simple structure, prone to extreme down scaling, 3-D stacking potentiality, high speed, low power consumption and excellent compatibility with the complementary metal-oxide-semiconductor (CMOS) technology, memristors are rightly considered the elemental bricks for a next generation of high-density nonvolatile memories [3, 4].

Typical employed insulator layers are binary metal oxides such as TiO_2 [1], [6–8], ZnO [9, 10], VO_2 [9], NiO [4], HfO_2 [4], and Ta_2O_5 [4]. Metal oxides are typically rich in defects. When they are inserted in a memristive structure and undergo electrical stresses, they exhibit a change in the electrical resistivity which leads to the two typical resistance switching states of the memristor: the High Resistance State (HRS) or OFF state, and the Low Resistance State (LRS) or ON state. The switching behavior is dependent not only on the oxide material but also on the metal contact employed, which enables different mechanisms for the conduction within the oxide film. In particular, if the contact metals are both inert (e.g. Pt), the most probable

resistive switching mechanism is the formation of conductive filaments within the oxide film [3]. The filaments are formed by oxygen vacancies, already present inside the defective oxide and/or introduced in the layer during the forming step of the device [11], that under electrical stimuli start to migrate, forming conductive paths between the two metal contacts [12]. On the other hand, when non-inert metals (e.g. Cu, Ag) are used as electric contacts, another possible switching mechanism is the formation of metallic bridges [10]. In this case, applying a proper positive voltage to the non-inert metal contact, the metal atoms start to migrate through the oxide as cations and deposit in metallic state at the opposite electrode. When the forming metal bridge reaches the other contact, a conductive path allows the resistance switching of the device, from the HRS to the LRS [13].

Titanium dioxide is nowadays largely used for resistive memory applications because of its abundance in nature and the excellent reported results. The two most common techniques employed for the deposition of TiO_2 films are RF sputtering and atomic layer deposition (ALD): they are, however, both expensive in terms of equipment and power consumption [1, 6]. As an alternative, anodizing is a low cost and low power consuming process (it is carried out at room temperature) to grow oxides on valve metals (such as Ti) and valve metals alloys that can be used in electronic devices [14, 15]. Furthermore, anodizing is a viable tool to grow oxides whose composition, thickness and structures can be easily tuned by selecting the metallic substrate and the electrochemical conditions (i.e. formation voltage, growth bath) [16]. So far just a few papers have reported memristive behavior of anodic grown TiO_2-based memristors. In particular, Miller *et al*. [7] have grown the oxide film by applying a constant voltage for different time durations and have fabricated large area memristors by using silver paste as electrical contacts. Diamanti*et al*. [8] instead have used conductive atomic force microscopy (c-AFM) for studying the homogeneity at the nanoscale of the anodic oxide grown in galvanostatic mode (i.e. by applying a constant current) and have found out a memristive behavior in an AFM tip/Nanocrystal TiO_2/Ti system. Memristive effect has also been found with anodic TiO_2 grown in the form of nanotubes [17].

In this work we expand the previous studies by introducing the dependence of the memristive behavior of micrometric anodic TiO_2-based memristors on the device size as well as on the anodizing parameters.

2. Experimental details

2.1. Fabrication process

All devices have been fabricated following the process steps depicted in Fig. 1. They result in the Cu/anodic-TiO_2/Ti sandwich structure of Fig. 1 (h), with Cu top electrodes of different sizes and a common Ti bottom electrode. The fabrication of the memristors starts with the e-beam deposition of an 80 nm thick Ti film onto 2 × 2 cm^2 glass substrates, which have been previously cleaned in an ultrasonic bath with acetone, rinsed in isopropanol and blown dry with nitrogen. Titanium is then anodized in a 1 M H_3PO_4 aqueous

solution with a three-electrodes configuration, using a Pt net as counter-electrode and a saturated silver/silver chloride electrode (Ag/AgCl) as reference electrode. Anodizing is carried out potentiostatically (i.e. by applying a constant voltage during oxide growth) at different potentials: 5V and 10 V (Ag/AgCl). By varying the anodizing parameters (i.e. formation potential and growth time), three different samples, named S1, S2, and S3 were obtained. Anodizing conditions are summarized in Table 1. All parameters were chosen to grow oxides with imperfect stoichiometry, necessary to obtain a memristive effect. Formation potential is directly proportional to anodic oxide thickness, thus sample S2 oxide film is the thickest one. The oxide thicknesses are estimated from the total circulated charge during anodic film growth through Faraday's law assuming unitary efficiency **[**18]. Not oxidized Ti was used as a common bottom contact for all the fabricated devices. No annealing was performed on the anodized films due to the reported detrimental effect of annealing on the Ag/anodic-TiO_2/Ti structure [7]. The next step was the definition of the memristors size by direct laser-assisted lithography. First, a 600 nm thick photoresist film (Shipley S1805) was spin-coated for 1 min at 2800 rpm on the TiO_2 film, and then baked for 5 min at 90 °C (Figure 1 (b)). The photoresist layer was then selectively exposed with a blue laser (405 nm) in order to define an array of 391 squared vias of different sizes (1 × 1 μm^2, 2 × 2 μm^2, 5 × 5 μm^2, and 10 × 10 μm^2) for each sample. After the resist development (Shipley MF319 developer) the samples were hard baked for 30 min at 200 °C. This curing process converted the photoresist into a hard and insulating layer which can withstand the following fabrication steps without being removed (Fig. 1 (c)). The hard photoresist layer has also the important task to avoid device damage during the following electrical characterization step, where the employed hard metal tips may penetrate through the device, making a short circuit between the top and bottom contacts. The next step was the deposition of a Cu film by thermal evaporation on the hard-baked photoresist (Fig. 1 (d)). With this step the micro-vias previously opened through the photoresist were filled with Cu, defining the active area of the memristors. The final photolithographic and wet etching steps (Figs. 1(e) to 1(h)) allowed the creation of large Cu pads acting as top contacts for each device. These pads are directly connected with the oxide film through the vias and are fundamental for easily probing the smallest devices (i.e. 1 × 1 μm^2, and 2 × 2 μm^2), otherwise not directly accessible being smaller than the tip's size.

Sample Name	S1	S2	S3
Formation potential [V vs. Ag/AgCl]	5	10	5
Growth time	100 s	20 min	20 min
Thickness [nm]	8 ± 5%	29 ± 5%	11 ± 5%

Table 1. Anodizing conditions and anodic films thickness (estimated from circulated charge during anodizing) for the three samples used in this work.

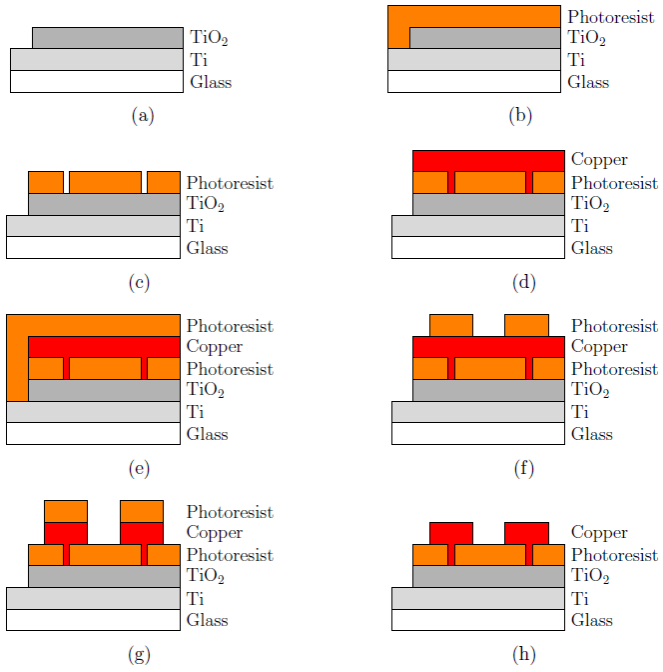

Fig. 1. Process steps for the memristors fabrication. (a) Anodic TiO_2 thin film grown on the metallic Ti film. A large area of Ti is preserved to be used as bottom contact during the electrical measurements. (b) Photoresist spin coating for the definition of the vias. (c) Laser-assisted lithography and vias definition after development. Hard baking of the photoresist. (d) Copper deposition. A metal mask is used to keep clear the Ti bottom electrode. (e) Photoresist spin coating for defining large Cu pads, using the same parameters as in the previous lithographic step. (f) Exposure and developing of the second mask. (g) Copper etching, using a 9 wt.% solution of ferric chloride in distilled water for 30 s, to obtain the Cu pads of 500 × 500 μm^2. (h) Completed devices.

2.2. Electrical characterization

All devices were electrically characterized at room temperature by performing two-probe I–V measurements. The bias voltage was swept from a negative to a positive potential while simultaneously measuring the current. To this purpose, a Versastat 3 (Princeton Applied Research) connected to a Karl Suss probe station was employed. The voltage was applied to the bottom electrode (Ti) while the top electrode (Cu) was grounded. The behavior of the devices was also double checked by using a simple setup made of a Philips PM5133 signal generator as a voltage source, a Tektronix TDS 1012 oscilloscope for data acquisition and a 1.2 MΩ resistor, connected in series with the device under test, for calculating the current values.

3. Results and discussion

In Fig. 2, are reported the current density vs. time curves recorded during the anodizing of Ti in 1 M H_3PO_4 solution. The measured current density decreases by increasing the polarization time, suggesting a decreasing electric field strength across the growing layer, according to the high field mechanism [19].

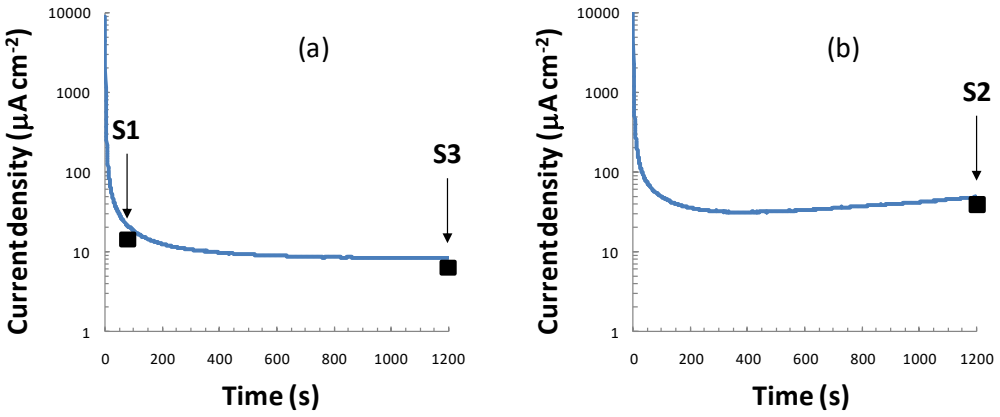

Fig. 2. Current density vs. time curves recorded during the potentiostatic growth of (a) S1, S3 samples and (b) S2 sample.

During potentiostatic polarization, the potential drop ΔV is distributed across the metal/oxide/electrolyte interface, according to the following relationship:

$$\Delta V = \Delta\Phi_{M/O} + \Delta\Phi_{oxide} + \Delta\Phi_{H} \quad (1)$$

where $\Delta\Phi_{M/O}$ is the potential drop at the Ti/TiO_2 interface, $\Delta\Phi_{oxide}$ (i.e. the product $E \times d_{oxide}$) is the potential drop across the growing oxide and $\Delta\Phi_H$ is the potential drop at the TiO_2/H_3PO_4 solution interface, due to the presence of the Helmholtz double layer. Since under band edge level pinning, $\Delta\Phi_H$ is constant [20], during potentiostatic growth, the transient current density and the electric field strength decay, due to the thickening

of the oxide. According to the Faraday's law and assuming unitary efficiency of the growth process, the oxide thickness can be expressed according to the following equation [16]:

$$d_{oxide} = \frac{M}{\rho z F}\left[\int j dt\right] \quad (2)$$

where j is the measured current density, M is the molecular weight of the growing oxide (79.9 g mol^{-1}), z = 4 is the number of electrons circulating per mole of formed oxide, F is the Faraday constant, and ρ is the oxide density (3.8 g cm^{-3}). As shown in Fig. 2 (a), the current density decreases all over the 5V potentiostatic transient, thus S3 sample is thicker than S1. In the case of 10 V anodic oxide growth (see Fig. 2 (b) for S2 sample), a slight increase of the current density during the oxide growth is recorded for long polarization time, probably due to the initial onset of crystallization process of the oxide and the consequent flowing of electronic current across the oxide. Estimated oxides thicknesses reported in Table 1 are in agreement with direct measurements of thickness from TEM inspections of anodic TiO_2 layers [21].

Fig. 3 shows the typical I–V curves for memristors of different size ranging from 1 × 1 μm^2 to 10 × 10 μm^2 taken from samples S1 (a) and S2 (b). The arrows indicate the switching direction. Memristive effect was observed for all tested devices in absence of a preliminary forming cycle. For sample S1, the voltage sweeps were performed following the sequence 0 V →–2.5 V → 2 V → 0 V at a sweep rate of 0.5 V/s for the 1 × 1 μm^2 devices, and 0 V →–2 V → 2 V → 0 V at 0.5 V/s for all other devices. This is due to the fact that smaller devices exhibit a smaller number of conductive filaments, then a larger voltage is necessary for the SET process (switching from HRS to LRS). Because of the thicker oxide film of sample S2 than sample S1, a larger voltage sweep (0 V →–3 V → 3 V → 0 V at 0.5 V/s) was necessary to achieve the resistive switching in sample S2.

All devices exhibited a bipolar hysteresis regardless of both size and oxide thickness. Because of the combination between metal contacts type and electrical connections arrangement employed, all the tested devices switched to the ON state only for negative applied voltages (V_{SET}~–2 V and~–1 V for the 10 × 10 μm^2 devices of S2,and S1, respectively), while switched to the OFF state only for positive applied voltages (V_{RESET}~ 2 V and ~1.75 V for the 10 × 10 μm^2 devices of S2, and S1, respectively). The switching to both ON and OFF states was gradual, typical of an analog device [22, 23]. Moreover, all the observed hysteresis had an asymmetric shape and a strong rectifying character. In particular, the current measured during the negative voltage sweep (from 0 V to –2 V or –3 V) is, depending on the specific device, one or even more than two order of magnitude larger than the current measured during the positive voltage sweep (from 0 V to 2 V or 3 V). This is visible in Fig. 3 which displays both positive and negative currents with the same scale. In order to see also the positive voltage sweep, a zoom of the I–V plot is needed down to the μA or nA scale,

respectively for S1 and S2 (see the insets of Fig. 3 (a) and (b)). Because of the thinner TiO_2 film, sample S1 exhibits larger positive current values than sample S2.

The structure of our devices ($Cu/TiO_2/Ti$) suggests that the conduction mechanism may be mainly ascribed to conductive copper bridges, alternatively formed and broken during the memristor operation [24 – 26]. The effect of the Ti contact may, in addition, play a role in supplying oxygen vacancies to the oxide, due to Ti oxidation and consequent formation of a non-stoichiometric oxide at the Ti/oxide interface [27 –29]. The latter modifies the small Ti/TO_2 barrier height (about 0.1 eV) [29, 30], [1], during devices operation. In particular, when a negative potential is applied to the Ti bottom contact, the Ti/TiO_2 barrier collapses giving rise to an ohmic contact [1], favouring then the switching to the LRS in tandem with the Cu filaments formation. During the positive voltage sweep, instead, the oxygen vacancies are repelled from the Ti contact and the depletion layer of the Ti/TiO_2 junction widens, leading, to a non ohmic contact. On the other hand, Cu filaments are broken due to the opposite electric field and the devices switch to the HRS. The dominant effect which limits strongly the current is however the Cu/TiO_2 Schottky diode (barrier height about 0.7 eV), which is responsible of the asymmetry shown by our devices. This kind of asymmetry has been reported not only with TiO_2-based memristors [29, 30], but also with HfO_2 [31, 32], ZnO [33, 34], and Al_2O_3 [35, 36]-based memristors, and has been ascribed normally to a diode-like behavior of one of the memristors contacts. The switching performance of our devices are strongly limited by the absence of a compliance in our setup. In average, a repeated cycling operation ends up with devices failure after about 20 cycles due to excessive Joule heating, leading in most of the cases to short circuits between the top and the bottom electrode.

I–V characterization of sample S3 (not shown here) was also performed in the same way as sample S1 and the hysteresis cycles obtained are similar to sample S1, except a slight decrease of the maximum currents which leads to higher resistances.

The asymmetry in the behavior of our devices has not been observed in [7], probably due to the larger size of their devices (~1 cm^2). The effect of different top metal contact should be excluded since the asymmetry is mostly due to the micrometric size of the structure [37]. In order to make a comparison, we prepared large area devices with a Cu top contact size of about 3 mm^2, deposited on sample S1 by thermal evaporation by means of a shadow mask. The electrical characterization, reported in Fig. 4, shows that the hysteresis cycle is symmetrical as reported in [7] and the order of magnitude of the current is the same for both positive and negative voltage sweeps. The R_{OFF}/R_{ON} ratio is however much lower (about 2) than that obtained for µm-scale devices. Transition from cm-scale devices reported in [7] to µm-scale devices presented in this work leads then to an asymmetric shape of the I-V curve and a larger R_{OFF}/R_{ON} ratio.

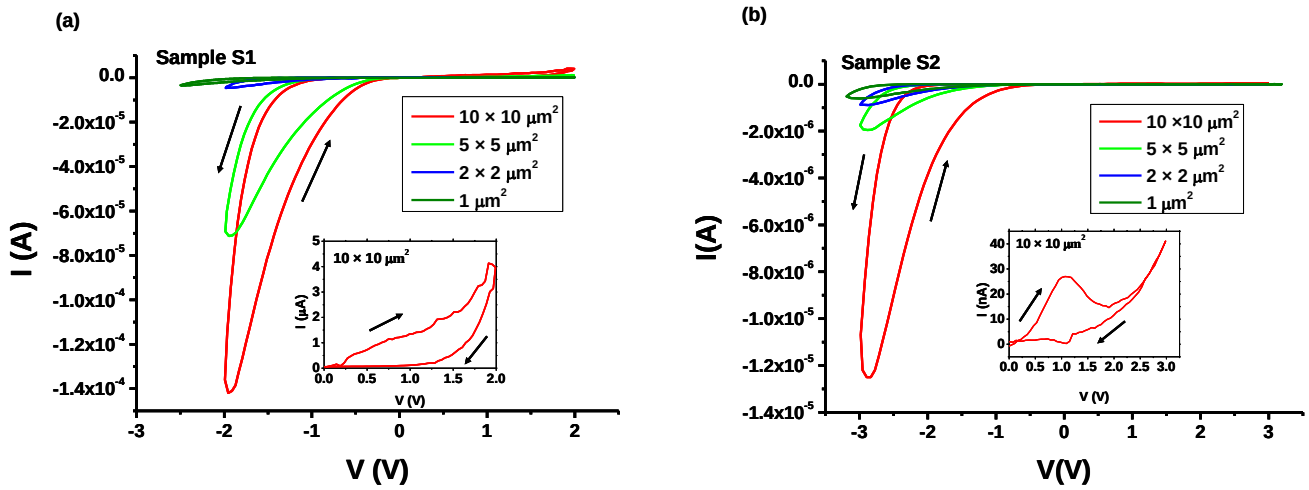

Fig. 3. Typical I–V hysteresis for each device size of sample S1 (a) and S2 (b). The insets zoom the positive voltage sweep for the 10 × 10 μm² devices.

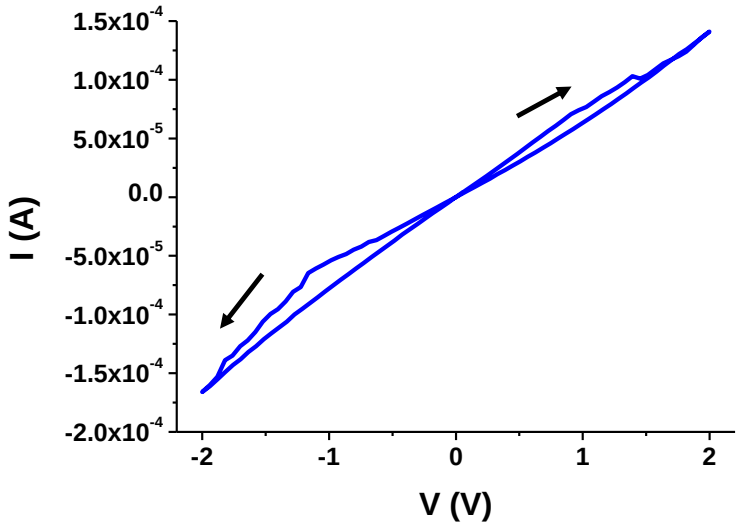

Fig. 4.Typical I–V curve taken from 2 mm diameter memristor with a 8.4 nm thick TiO_2 film. The arrows show the direction of the sweep.

In order to evaluate the quality of the resistance switching of the three samples, a comparative study in terms of R_{OFF} and R_{ON} against oxide thickness and device size is reported in Fig. 5. The resistance values were measured for each device at −1.3 V. By comparing the thinnest (S1) with the thickest (S2) oxide film sample, R_{OFF} increases for more than two order of magnitude (Fig. 4 (a), red triangles vs. green circles). This important change may be ascribed to the larger resistivity offered by sample S2, having a thicker oxide film and a reduced number of defects than sample S1 due to the longer anodizing process. R_{ON} (Fig. 4 (b)) shows a more limited but still significative increase. It is possible that the thicker oxide limits the number of

filaments obtainable for fixed applied voltage, making the conduction mechanism through filaments more difficult. This increase of resistances is much more limited by comparing sample S1 and sample S3, grown at the same voltage (5 V) but for different time (100 s and 20 min, respectively). In this case, the values of R_{OFF} and R_{ON} for devices of sample S3 are respectively increased by less than one order of magnitude if compared to the devices of sample S1. This can be ascribed to the slightly thicker oxide film of sample S3 with respect to sample S1 and to the larger resistivity of sample S3 oxide, because of the reduced number of defects expected after 20 min of anodizing. As consequence of these R_{OFF} and R_{ON} behaviors, the largest R_{OFF}/R_{ON} ratio is obtained for the thickest oxide sample, regardless the devices size.

By comparing the resistance states against devices area, it is possible to notice that R_{OFF} increases when devices size decreases. This is in good agreement with other results reported in the literature and indicates that in the HRS, the electrical conduction is homogeneous and the current passes through the whole interface between contacts and oxide (i.e. without conductive filaments, which in the HRS are all broken) [38].

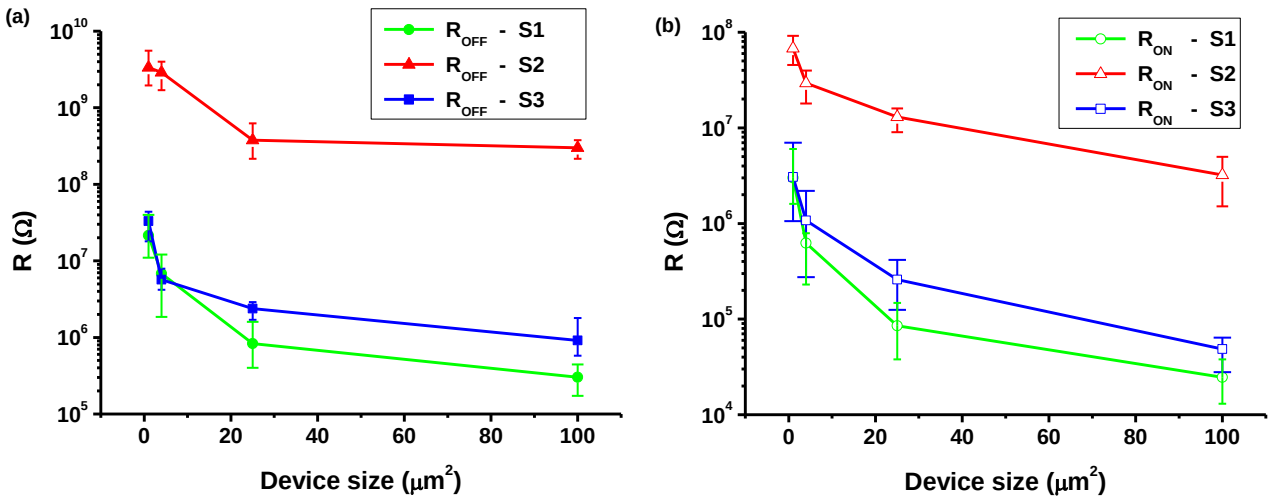

Fig. 5. R_{OFF}(a) and R_{ON}(b) against devices size for samples S1 (5 V, 100 s), S2 (10 V, 20 min), and S3 (5 V, 20 min).

R_{ON} increases as well when device size decreases. This behavior remarks the interface-switching mechanism of our devices, which is typical of analog memristors [22, 23]. Actually we noticed that, for all tested devices, after the first sweep the cycle becomes larger and larger with an evident increase of the maximum current. This behavior, shown by all devices, could be explained with a gradual switching of the device toward the ON state and a step by step formation of multiple filaments which leads to a gradual increase of the conductance shown by the device. In Fig. 6 we show 20 consecutive hysteresis cycles obtained with a voltage sweep between −2 V and 2 V applied to the 10 × 10 μm^2 device of S2. The inset shows instead the

plots of the current and the voltage against the elapsed time from the beginning of the applied voltage sweep. It is clear how the current increases with the number of cycles, showing the existence of a number of different resistance states until the full switching to the LRS.

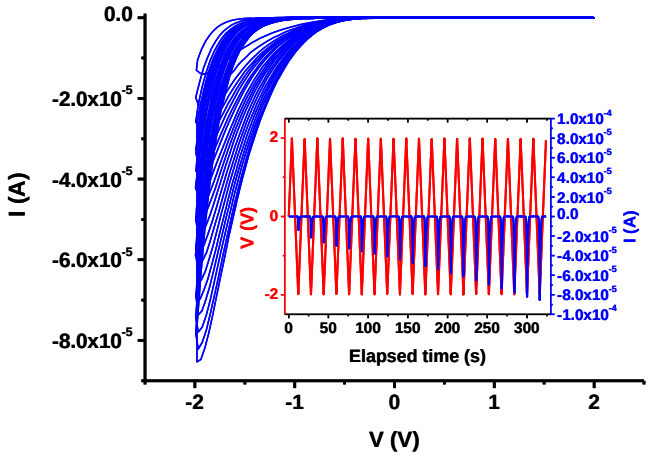

Fig. 6. Hysteresis cycles after 20 sweeps from –2 V to 2 V for the 10 × 10 μm^2 device of sample S2. The inset shows the temporal behavior of the applied voltage and the measured current.

The non constant behavior of R_{ON} against device size, limits the R_{OFF}/R_{ON} ratio of the smallest devices, and the best R_{OFF}/R_{ON} achieved in our study is about 80, for the 2 × 2 μm^2 devices of the thickest oxide sample (S2).

4. Conclusions

The memristive character of anodic titanium dioxide-based memristors, obtained at three different anodizing conditions and different size was investigated. The anodic TiO_2 film was grown on a Ti film in potentiostatic mode and the active area of the devices was defined through vias ranging from 1 × 1 μm^{2}to 10 × 10 μm^2. Millimeter-scale devices were also fabricated for comparison.

The I–V hysteresis obtained from all the μm-scale samples have the same asymmetric bipolar shape, with the negative loop much larger than the positive loop. Millimeter-scale devices show instead a symmetric shape and a smaller R_{OFF}/R_{ON} ratio.

By comparing devices with different oxide thickness, the thickest oxide film sample, grown at 10 V for 20 min, shows a higher R_{OFF}/R_{ON} ratio regardless of the devices size. The comparison between devices of different size shows an increase of R_{OFF} while decreasing the devices size regardless of the oxide film thickness. There is however also an increase of R_{ON} with device size decreasing, which limits the R_{OFF}/R_{ON}

ratio of the 1 × 1 μm^2 devices. The largest R_{OFF}/R_{ON} ratio is about 80 and is obtained for the 2 × 2 μm^2 devices of the thickest oxide sample (S2).

In conclusion, microscale low cost anodic-TiO_2-based memristors presented in this work, under specific fabrication conditions, have shown improved resistance contrast than previously published cm-scale devices. This result is encouraging for a further down scaling toward the nanometer scale for meeting the high density memory requirements for the next generation of RRAM.

Acknowledgments

The authors would like to thank the University of Palermo for financial support.

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