INAF Technical Report

SOXS: UV-VIS Detector System setting and test

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Change Record

Issue/ Rev.	Date	Section/Page affected	Reason/Remarks
1.0	25/09/2020		
1.1	23/10/2020	CCD test added	Test on Engineering CCD
2.0	26/2/2021	CCD test results added	Test on scientific CCD

Contents

1. Introduction

1.1 Scope

This document is intended to describe the CCD acquisition system for SOXS and the test on the electronics and on the detector.

At the beginning of this document, we will describe the E2V4482 CCD, the CCD settings and the phases for the different readout modes. We will describe the generated CCD waveforms, written with the waveform editor (BlueWave), we will show the waveforms generated by the controller and the theoretical waveforms provided by e2v.

Following we will illustrate the electronic tests on the bias, clock sequences and the test on the CCD detector.

1.2 Additional information

No additional information, at the moment.

1.3 Contact information

Feedback on this document is encouraged. Please email to cosentino@tng.iac.es

1.4 Reference documents

[RD01] **CCD44-82 NIMO Back illuminated High Performances CCD Sensor Datasheet**

[RD02] **NGC User Manual i1.0 (VLT-MAN-ESO-13660-4510)**

[RD03] **NGC Waveform Editor User Manual v1.1 (VLT-MAN-ESO-13660-3897)**

[RD04] **Optical DCS User Manual (VLT-MAN-ESO-13660-4086)**

[RD05] **Fiera Preamplifier rev_2b**

1.5 Acknowledgments

A special acknowledgement to the Dtec team of the FGG for the competent and useful contribution in the mechanic, optic and cryogenic support that made possible the realization of the laboratory tests, and to the technical office of FGG for the safety support.

2. The e2v 4482 CCD

In this paragraph are introduced some information about the e2v CCD 4482, that has been used for the programming/generation of the waveform sequences. More information and the characteristic of the e2v 4482 CCD can be found in [RD01].

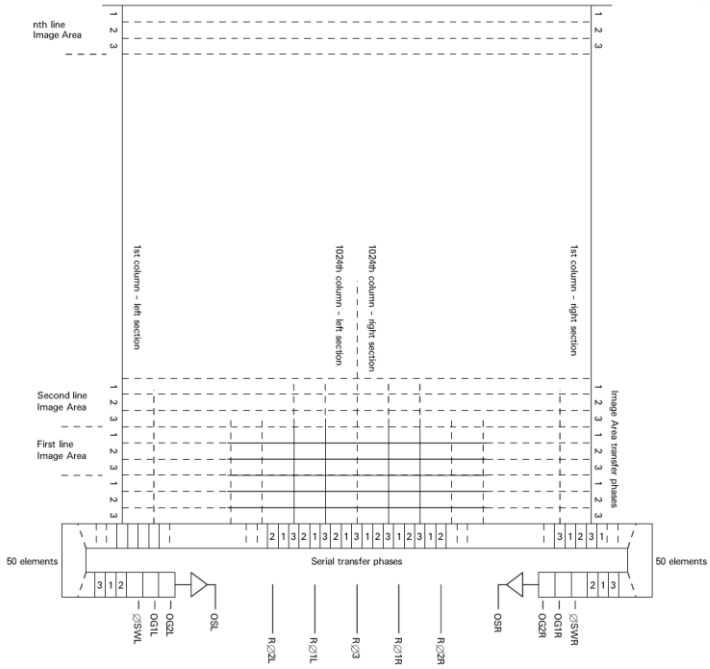


Figure 1 - Device Schematic

Table 1 - CCD Voltages

CONNECTIONS, TYPICAL VOLTAGES AND ABSOLUTE MAXIMUM RATINGS
40-pin PGA connector

PGA PIN	REF	DESCRIPTION	CLOCK AMPLITUDE OR DC LEVEL (V) (see note 7)			MAXIMUM RATINGS with respect to V_{SS}
			Min	Typical	Max	
A1, A8, C1, C8, F2, F7	V_{SS}	Substrate	-	9	-	-
D8	IØ1	Image area clock, phase 1	8	10	14	±20 V
E8	IØ2	Image area clock, phase 2	8	10	14	±20 V
F8	IØ3	Image area clock, phase 3	8	10	14	±20 V
D4	RØ1(L)	Register clock phase 1 (left)	9	11	15	±20 V
E4	RØ2(L)	Register clock phase 2 (left)	9	11	15	±20 V
D5	RØ1(R)	Register clock phase 1 (right)	9	11	15	±20 V
E5	RØ2(R)	Register clock phase 2 (right)	9	11	15	±20 V
F6	RØ3	Register clock phase 3	9	11	15	±20 V
E3	ØR(L)	Reset gate (left)	9	12	15	±20 V
E6	ØR(R)	Reset gate (right)	9	12	15	±20 V
E2	ØSW(L)	Summing well gate (left)	9	11	15	±20 V
E7	ØSW(R)	Summing well gate (right)	9	11	15	±20 V
F3	DG	Dump gate (see note 8)	−0.5	0	15	±20 V
D3	OG1(L)	Output gate 1 (left)	1	3	4	±20 V
D6	OG1(R)	Output gate 1 (right)	1	3	4	±20 V
B2	DD(L)	Dump drain (left)	22	24	26	−0.3 to +30 V
B7	DD(R)	Dump drain (right)	22	24	26	−0.3 to +30 V
D2	OG2(L)	Output gate 2 (left)		see note 9		±20 V
D7	OG2(R)	Output gate 2 (right)		see note 9		±20 V
B1	OD(L)	Output drain (left)	27	29	-	−0.3 to +35 V
B8	OD(R)	Output drain (right)	27	29	-	−0.3 to +35 V
A2	OS(L)	Output source (left)		see note 10		−0.3 to +25 V
A7	OS(R)	Output source (right)		see note 10		−0.3 to +25 V
C2	RD(L)	Reset drain (left)	15	17	-	−0.3 to +25 V
C7	RD(R)	Reset drain (right)	15	17	-	−0.3 to +25 V
Optional connections for 309 JFET						
A3	RL(L)	Load resistor (left)		A_{GND} (0 V)		
A6	RL(R)	Load resistor (right)		A_{GND} (0 V)		
B3	OP(L)	JFET source (left)		see note 11		
B6	OP(R)	JFET source (right)		see note 11		
C3	JD(L)	JFET drain (left)		OD(L) +2 V		
C6	JD(R)	JFET drain (right)		OD(L) +2 V		
Other connections						
D1, F1	Temp	Temperature sensor*		PT100		
E1	-	No connection				

If all voltages are set to the typical values, operation at or close to specification should be obtained. Some adjustment within the range specified may be required to optimize performance. Refer to the specific device test data if possible.

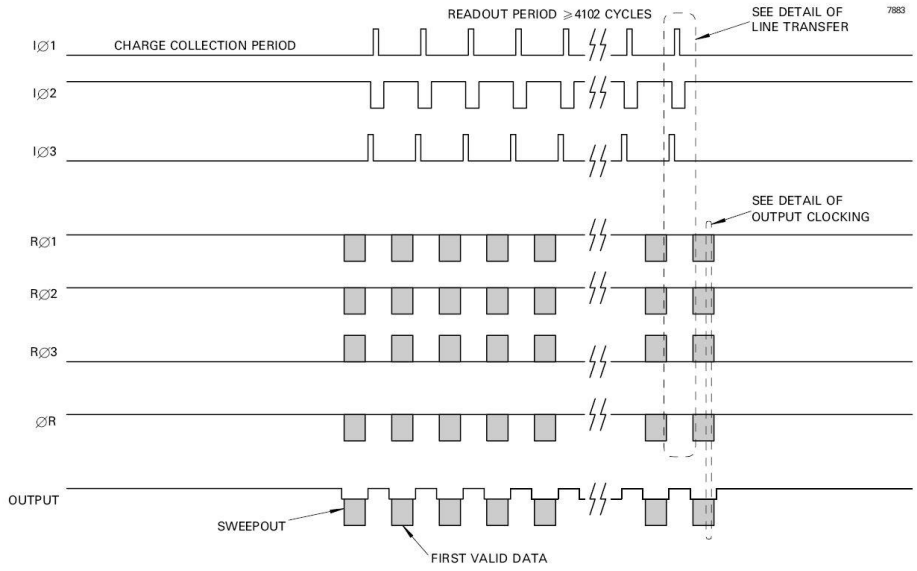
Maximum voltages between pairs of pins:

OS to OD +15 V.
Maximum current through any source or drain pin: 10 mA.
The CCD is not electrically connected to the metal package.

NOTES

7. Clock pulse low levels 0 + 0.5 V for image, reset and SW clocks; except R1 low = +1 V (register). For clock signals, the table indicates high levels for clocks.
   With the R1 connections shown, this device will operate through both outputs simultaneously (split serial mode). To operate from the left-hand output only, R11(R) and R12(R) should be reversed, i.e. pin D5 = R12(R) and E5 = R11(R).
8. Non-charge dumping level is shown. For charge dumping, DG should be pulsed to 12 + 2 V.
9. OG2=OG1 + 1 V; for operation in high responsivity, low noise mode, OG2 should be set to +4 V typical. For operation in low responsivity, increased charge handling mode, OG2 should be set to +20 V.
10. OS = 3 to 5 V below OD typically. Use a 3 – 5 mA current source or a 5 – 10 kΩ load.
11. The JFET is floating, with its gate connected to OS. A floating 10 kΩ load resistor is also connected to OS. The FET may be used to buffer the chip output (OS) if desired; in this case, connect the FET output to A_{GND} via a 5 mA load and RL directly to A_{GND}. (U309 data: V_{GD} and V_{GS} absolute maximum = -25 V). See detail below.

FRAME READOUT TIMING DIAGRAM



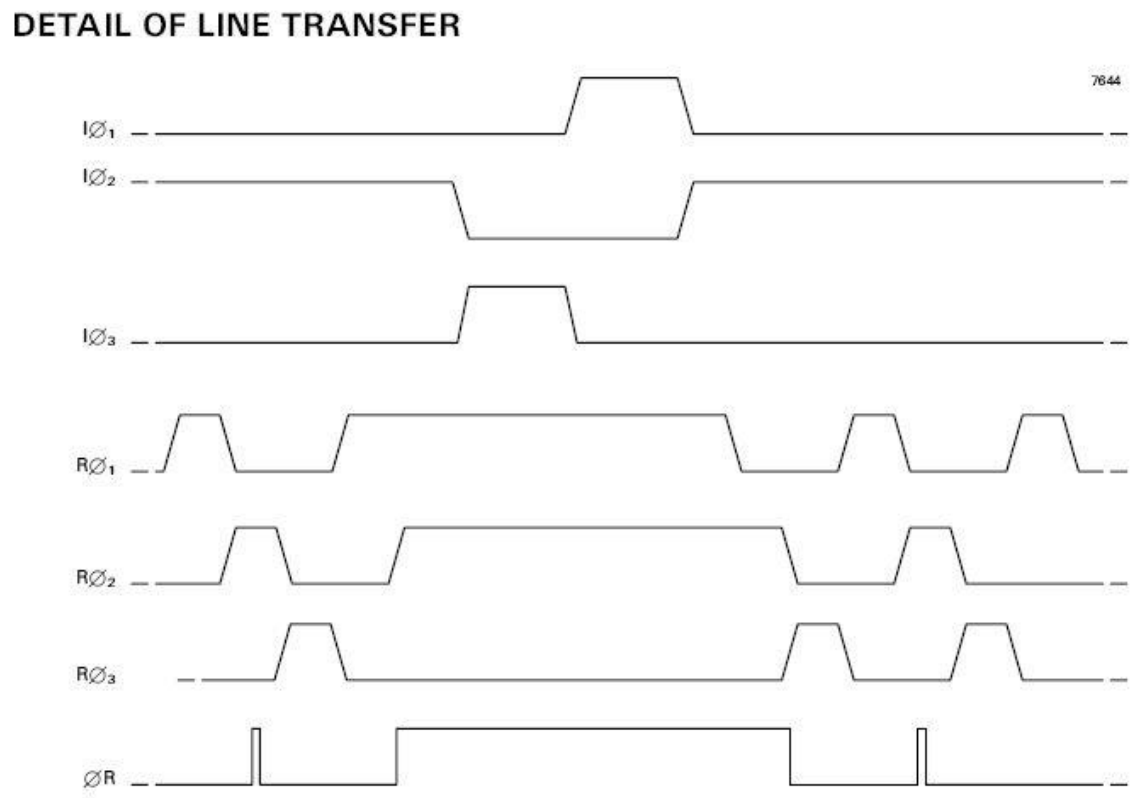


Figure 2 - Line Transfer

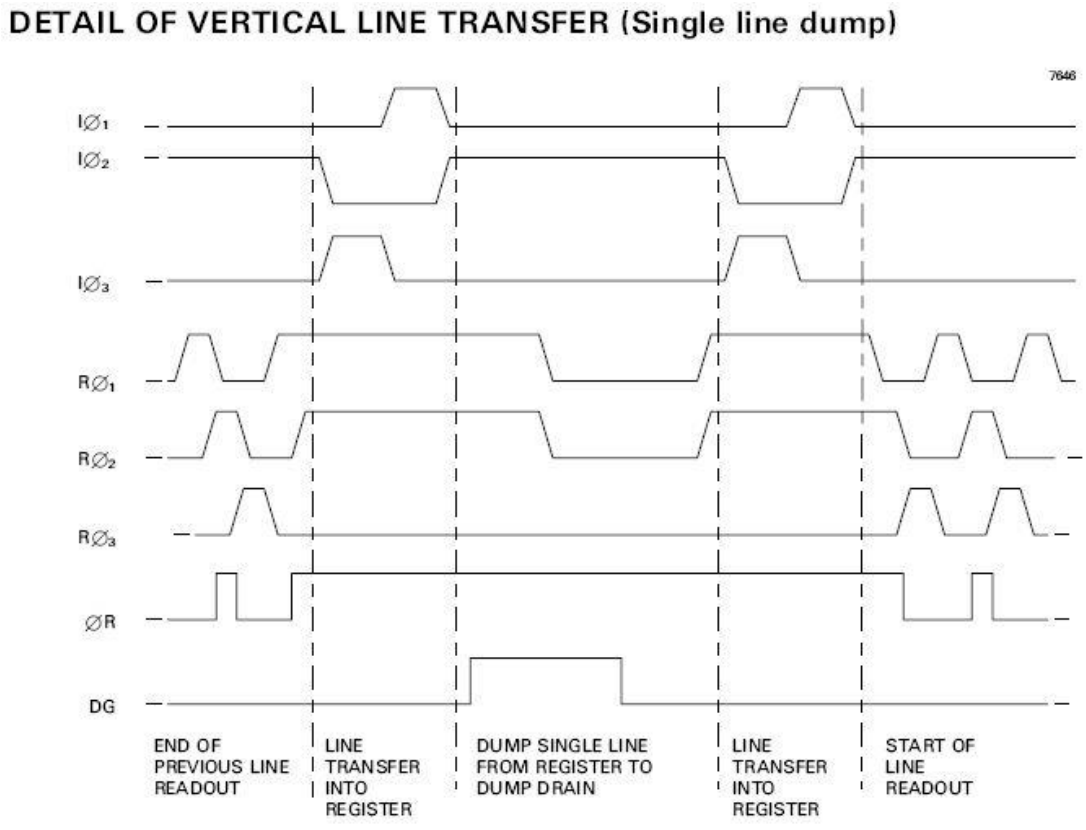


Figure 3 - Vertical Line Transfer (single line)

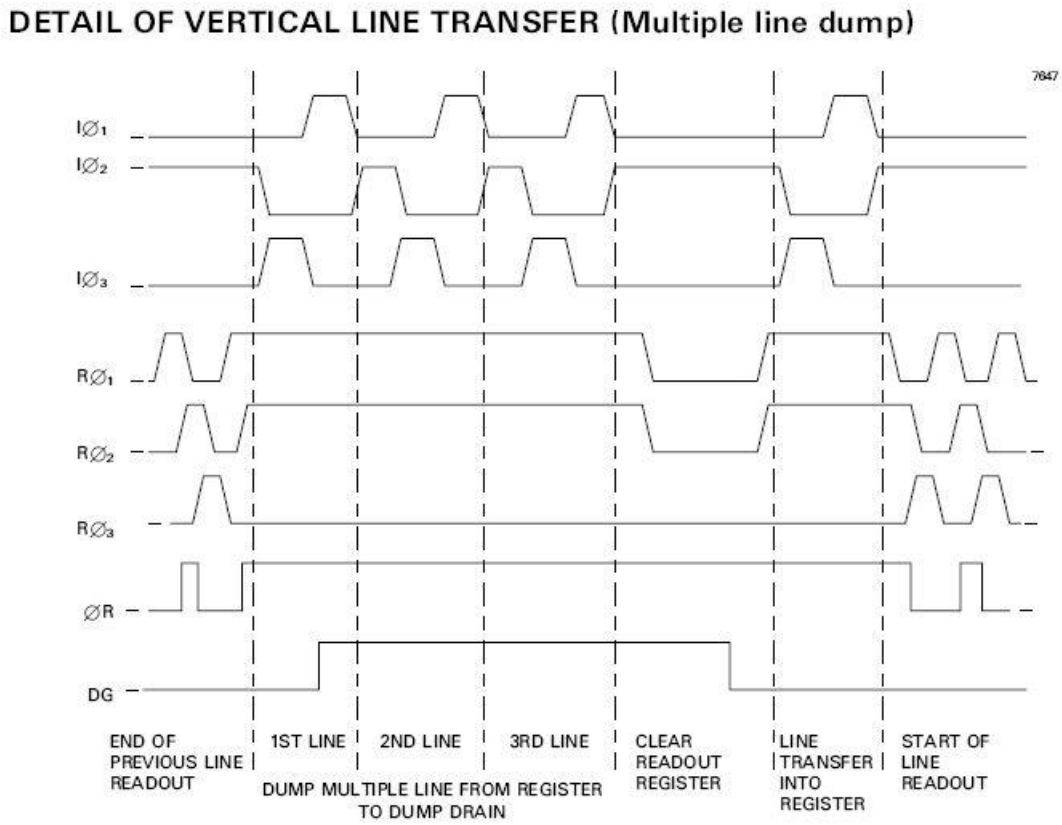


Figure 4 - Vertical Line Transfer (multiple line)

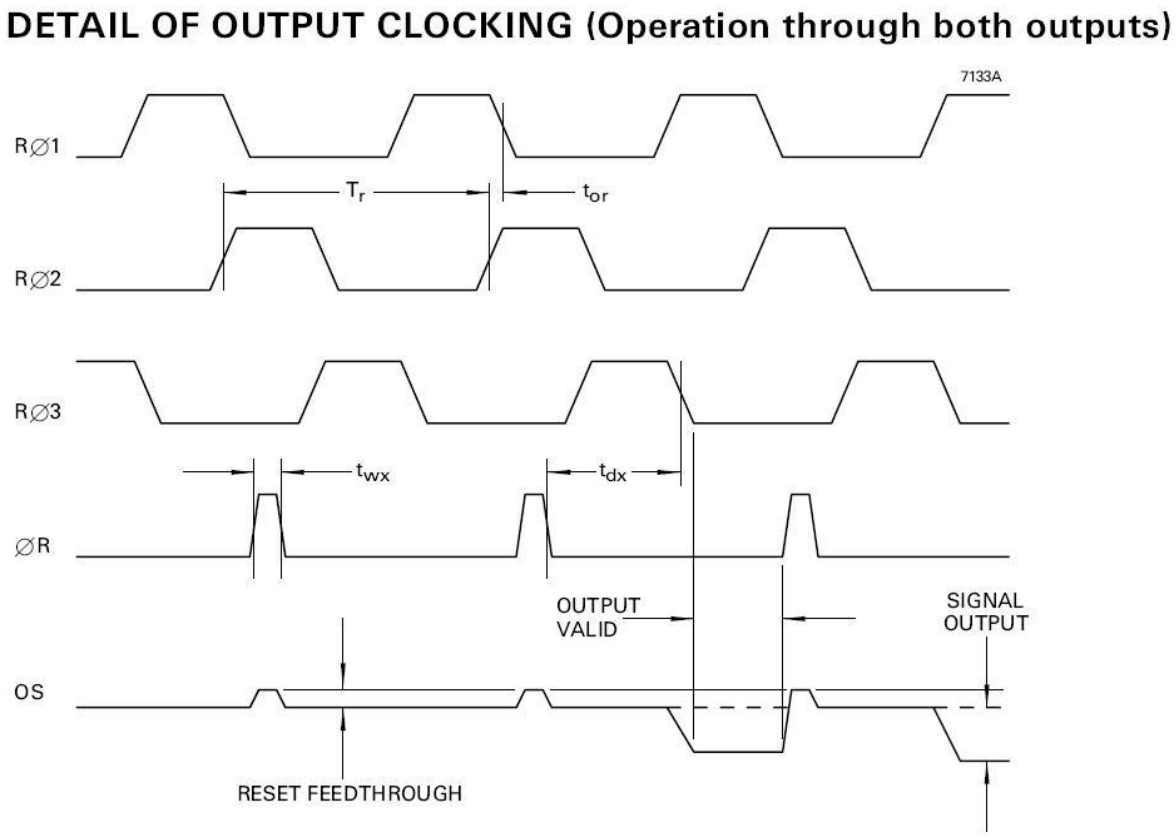


Figure 5 - Output Clocking (both output)

Table 2 - Clocking Timing

CLOCK TIMING REQUIREMENTS

Symbol	Description	Min	Typical	Max	
T_i	Image clock period	50	100	see note 12	µs
t_{wi}	Image clock pulse width	25	50	see note 12	µs
t_{ri}	Image clock pulse rise time (10 to 90%)	1	10	$0.5t_{oi}$	µs
t_{fi}	Image clock pulse fall time (10 to 90%)	t_{ri}	10	$0.5t_{oi}$	µs
t_{oi}	Image clock pulse overlap	5	10	$0.2T_i$	µs
t_{li}	Image clock pulse, two phase low	10	20	$0.2T_i$	µs
t_{dir}	Delay time, I∅ stop to R∅ start	10	20	see note 12	µs
t_{dri}	Delay time, R∅ stop to I∅ start	1	2	see note 12	µs
T_r	Output register clock cycle period	1	see note 13	see note 12	µs
t_{rr}	Clock pulse rise time (10 to 90%)	100	$0.1T_r$	$0.3T_r$	ns
t_{fr}	Clock pulse fall time (10 to 90%)	t_{rr}	$0.1T_r$	$0.3T_r$	ns
t_{or}	Clock pulse overlap	50	$0.5t_{rr}$	$0.1T_r$	ns
t_{wx}	Reset pulse width	50	$0.1T_r$	$0.2T_r$	ns
t_{rx}, t_{fx}	Reset pulse rise and fall times	20	$0.5t_{rr}$	$0.2T_r$	ns
t_{dx}	Delay time, ∅R low to R∅3 low	50	$0.5T_r$	$0.8T_r$	ns

OUTPUT CIRCUIT

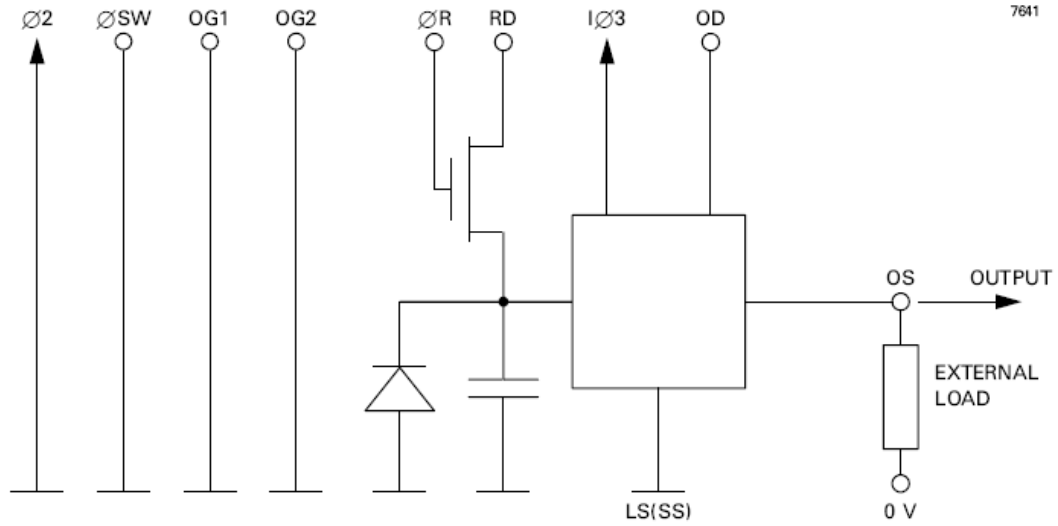


Figure 6 - Output Circuit

3. The bias programming

For the bias programming the SOXS UV-VIS acquisition system uses the file 'soxs.v' that contains the proper values for the e2v4482 CCD. In Table 3 are shown the theoretical values, the programmed and the voltages read in the CCD ZIF connector with the digital voltmeter (in green)

Table 3 - Bias values for the e2v 4482 CCD

Bias	Name	Value	Set	CCD	DATASHEET			Max to Vss	ESO
					Min	Typ	Max		
	Vss	0	0	A1,A8,C1,C8,F2,F7	0	3	10.00		0
dc[1]	RDR	11.57	11.5	C7	15	17	19.00	-0.3 to 25 V	11.5
dc[2]	JDR	24.88	25	C6	29	33			25
dc[3]	JDL	25.00	25	C3	29	33			25
dc[4]	DDLR	18.56	18.5	B2/B7	22	24	26.00	-0.3 to 30 V	18.5
dc[5]	RDL	11.59	11.5	C2	15	17	19.00	-0.3 to 25 V	11.5
dc[6]	ODL	23.08	23	B1	27	31	32.00	-0.3 to 35 V	23
dc[7]	ODR	23.07	23	B8	27	31	32.00	-0.3 to 35 V	23
dc[17]	0G2R	-2.50	-2.5	D7	2	4	5.00	± 20	-2.5
dc[18]	OG1R	-3.37	-3.5	D6	1	3	4.00	± 20	-3.5
dc[19]	0G2L	-2.50	-2.5	D2	2	4	5.00	± 20	-2.5
dc[20]	OG1L	-3.36	-3.5	D3	1	3	4.00	± 20	-3.5

Table 4 - voltages rating

Name	ESO TO Vss	EEV to Vss			Max to Vss
		Min	Typ	Max	
Vss	0	0	0		
RDR	11.5	12	14		-0.3 to 25 V
JDR	25	26	30		
JDL	25	26	30		
DDLR	18.5	19	21	23	-0.3 to 30 V
RDL	11.5	12	14		-0.3 to 25 V
ODL	23	24	28		-0.3 to 35 V
ODR	23	24	28		-0.3 to 35 V
0G2R	-2.5	-1	1	2	± 20
OG1R	-3.5	-2	0	1	± 20
0G2L	-2.5	-1	1	2	± 20
OG1L	-3.5	-2	0	1	± 20

4. The clocks programming

For the bias programming the SOXS VIS acquisition system uses the file ‘soxs.v’ that contains the proper values for the e2v4482 CCD. In Table 5 are shown the theoretical values, the programmed and the clock voltages read in the CCD ZIF connector with the digital voltmeter (in green)

Table 5 - Clocks values for the e2v 4482 CCD

Clock	Name	Low	Set	High	Set	CCD	DATASHEET			ESO		
							Min	Typ	Max	Low	Hi	Amp
clk[1]	SWL	-4.91	-5	5.05	5	E2	9	11	15	-5	5	10
clk[2]	SWR	-4.90	-5	5.06	5	E7	9	11	15	-5	5	10
clk[3]	RF3	-4.89	-5	5.05	5	F6	9	11	15	-5	5	10
cik[4]	RF2L	-4.92	-5	5.07	5	E4	9	11	15	-5	5	10
clk[5]	RF1L	-4.90	-5	5.04	5	D4	9	11	15	-5	5	10
clk[6]	RF2R	-4.91	-5	5.01	5	E5	9	11	15	-5	5	10
clk[7]	RF1R	-4.93	-5	5.05	5	D5	9	11	15	-5	5	10
clk[8)	DG	-5.90	-6	6.01	6	F3	-1	0	15	-6	6	12
clk[9]	IF1	-5.94	-6	4.08	4	D8	8	10	14	-8	2.5	10.5
clk[10]	IF2	-5.94	-6	4.03	4	E8	8	10	14	-8	2.5	10.5
elk([11]	IF3	-5.90	-6	4.05	4	F8	8	10	14	-8	2.5	10.5
clk([15]	FRL	-5.89	-6	6.02	6	E3	9	12	15	-6	6	12
clk([16]	FRR	-5.92	-6	6.06	6	E6	9	12	15	-6	6	12

5. Preamplifier test

The preamplifier was tested by using a signal generator (Figure 8) and the oscilloscope (Figure 9), with different gain and bandwidth. The tests was repeated for each channels of the preamplifier (selected in the engineering interface, see Figure 11).

Figure 8 - Signal generator

Figure 7 - Generator to preamplifier cable

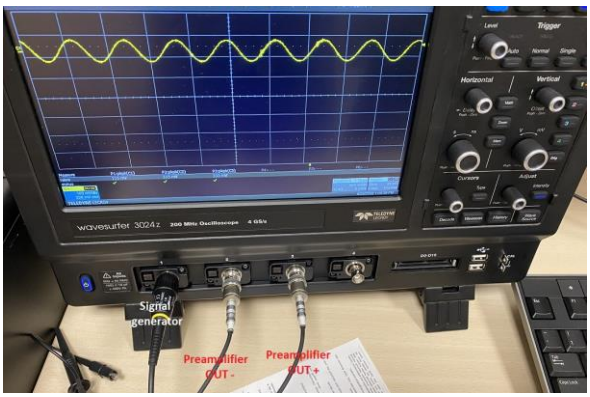


Figure 9 – Lecroy Oscilloscope

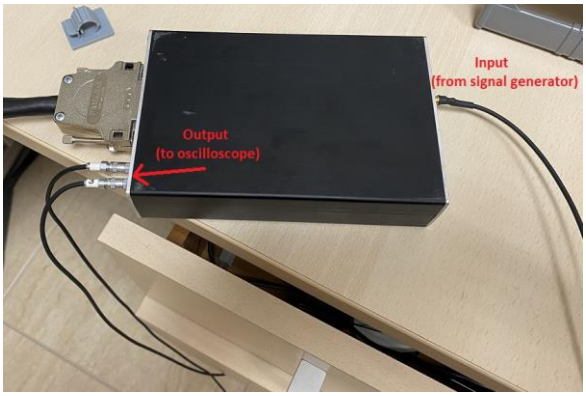


Figure 10 - NGC preamplifier

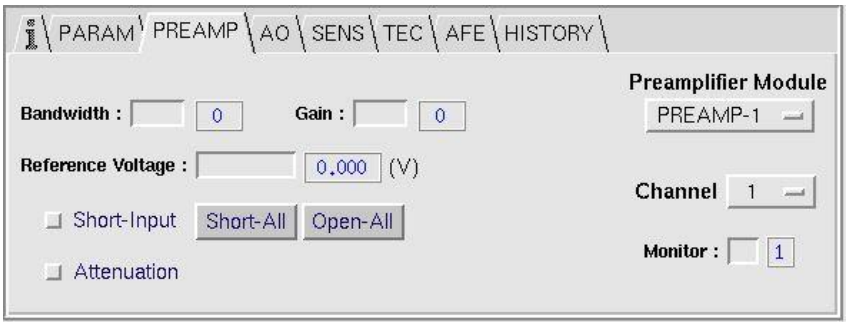


Figure 11 - Preamplifier settings

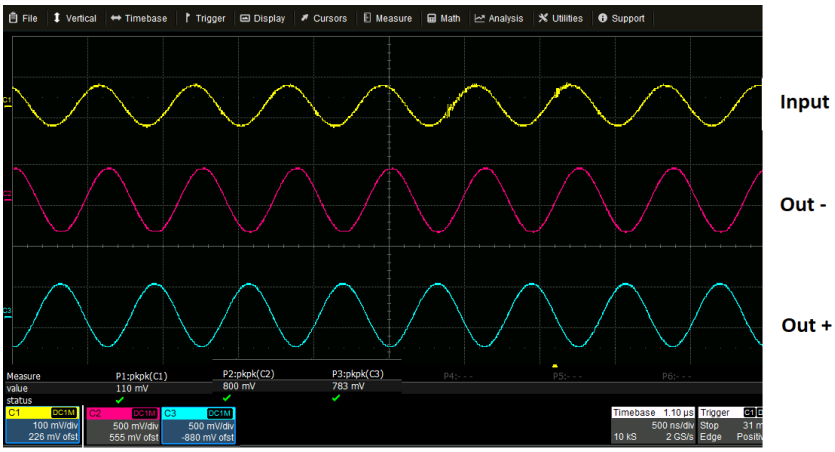


Figure 12 - Input signal vs output signals

In Table 6 are reported the preamplifier gains, calculated at TNG laboratory and provided by ESO.

Table 6 - Preamplifier gain

Gain selected	OUT +	OUT -	Calculated Gain	ESO Gain
0	1005	1007	19.53	24.62
1	1000	1000	19.42	23.2
2	967	967	18.78	22.2
3	933	933	18.12	20.72
4	867	867	16.83	20.22
5	817	817	15.86	18.82
6	783	783	15.20	17.76
7	717	733	14.08	16.36
8	483	483	9.38	10.56
9	417	417	8.10	9.18
10	367	367	7.13	8.12
11	333	317	6.31	6.72
12	283	283	5.50	6.16
13	217	217	4.21	4.76
14	187	187	3.63	3.72
15	120	120	2.33	2.32

Table 7 - preamplifier bandwidth

Bandwidth selected	Remarks	Bandwidth
0	Full bandwidth	5.49 MHz
1	400 kpx/sec	1.25 MHz
2		596 KHz
3	200 kpx/sec	433 KHz
4		320 KHz
5		266 KHz
6	100 kpx/sec	215 KHz
7		190 KHz
8		154 KHz
9		141 KHz
10		125 KHz
11		116 KHz
12	50 kpx/sec	106 KHz
13		99 KHz
14		91 KHz
15		86 KHz

6. The Programmed Waveforms

6.1 The Waveform of the NGC controller (Bluewave)

The waveform shown in this paragraph was be used in the implementation of NGC CCD controller for SOXS and was be programmed by using the Waveform Editor Program ('BlueWave').

Different patterns (Figure 13) are combined by a script (Table 8) to generate the clock sequences for the CCD readout.

Table 8 - Script for the CCD readout

```
JSR WIPE 1
JSR INTEGRATE 1
JSR READ 1
RETURN
WIPE:
LOOP 2
  EXEC line_dump 4144
  EXEC wipe_serial 4178
END
EXEC end_wipe 1
RETURN
INTEGRATE:
EXEC integrate 100
EXEC end_integrate 1
RETURN
READ:
# wipe serial register
LOOP 4
  EXEC wipe_serial 4178
END
# generate prescan lines
LOOP $PRSCY
  EXEC wipe_serial 18
  EXEC pre_read 1
  LOOP $PIXEL
    EXEC h_shift $DET.BINX
    EXEC post_read 1
  END
END
# read binned image $LINES x $PIXEL
LOOP $LINES
  EXEC line_shift $DET.BINY
  EXEC wipe_serial 18
  EXEC pre_read 1
  LOOP $PIXEL
    EXEC h_shift $DET.BINX
    EXEC post_read 1
  END
END

RETURN
```

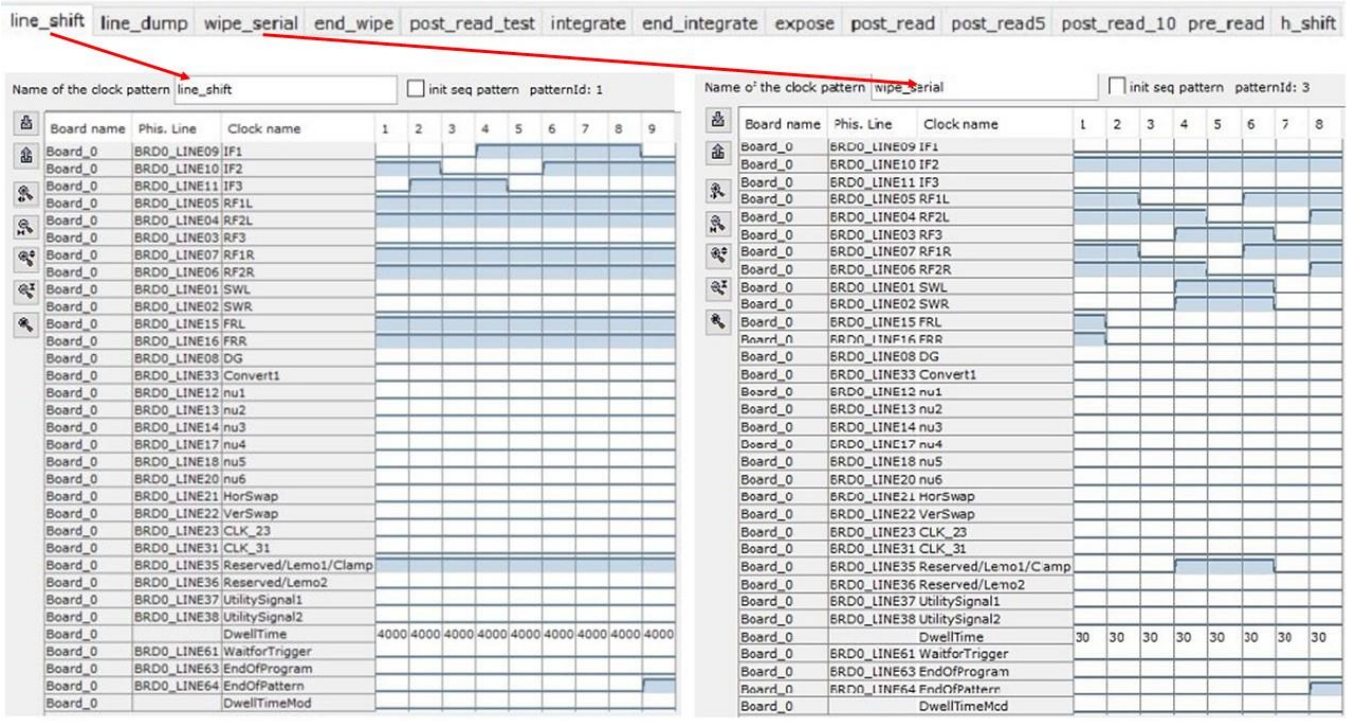


Figure 13 - Example of patterns

7. Test of the Waveform with the oscilloscope

To verify the bias voltages and the clocks waveform, the approach was the measurement of the signals in different point of the electronic chain (NGC, connectors and ZIF socket). In the following paragraph will be described the configurations used and the results obtained.

7.1 NGC controller with the test board

In this test the configuration is:

- CCD controller NGC
- SOXS cables
- Test board (without CCD)

Figure 14 - Test Equipment

In this test we used the test equipment of Figure 14 and the measures was done on the CCD ZIF socket.

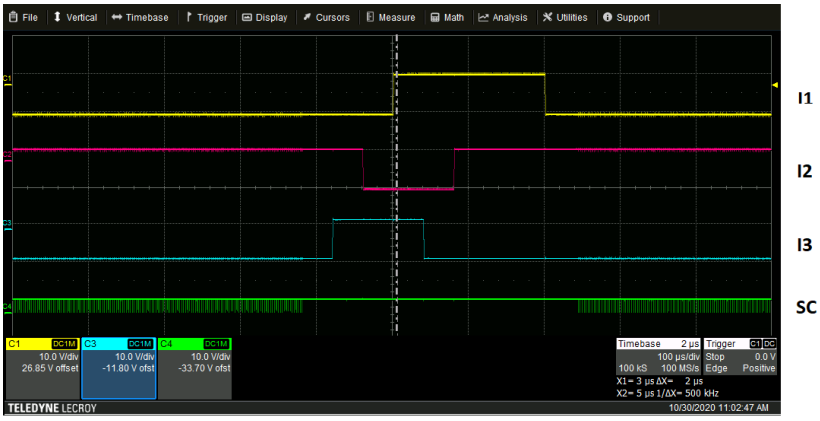


Figure 15 - Vertical waveforms without capacitor filter in the intermediate board

Figure 16 - Vertical waveforms with 0.1 µF capacitor filter in the intermediate board

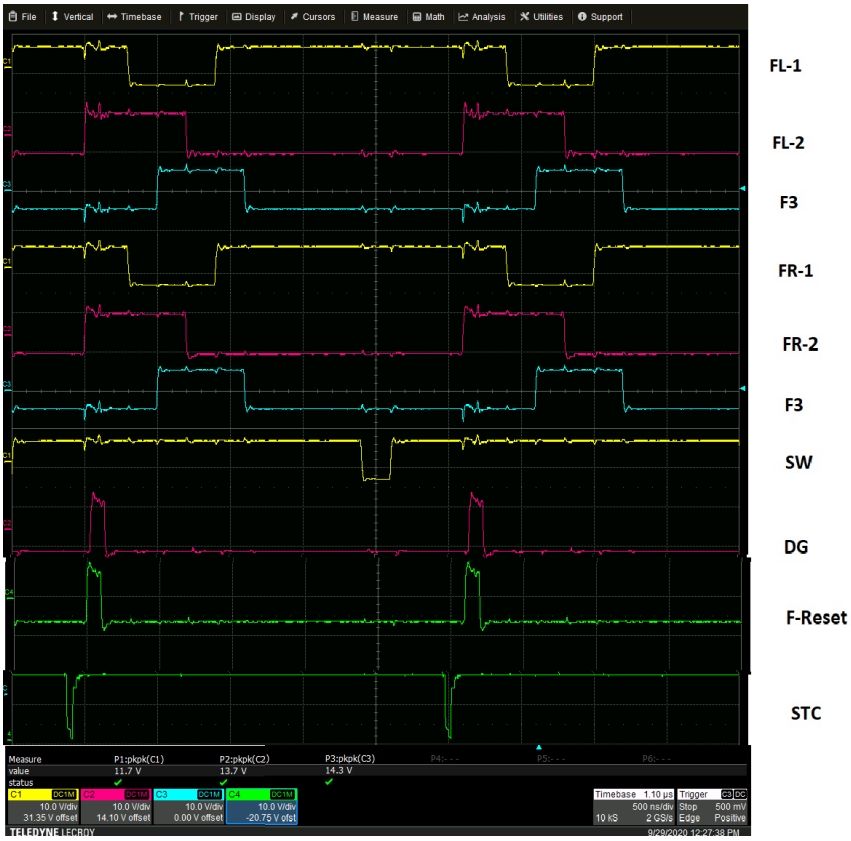


Figure 17 - Serial LR waveforms

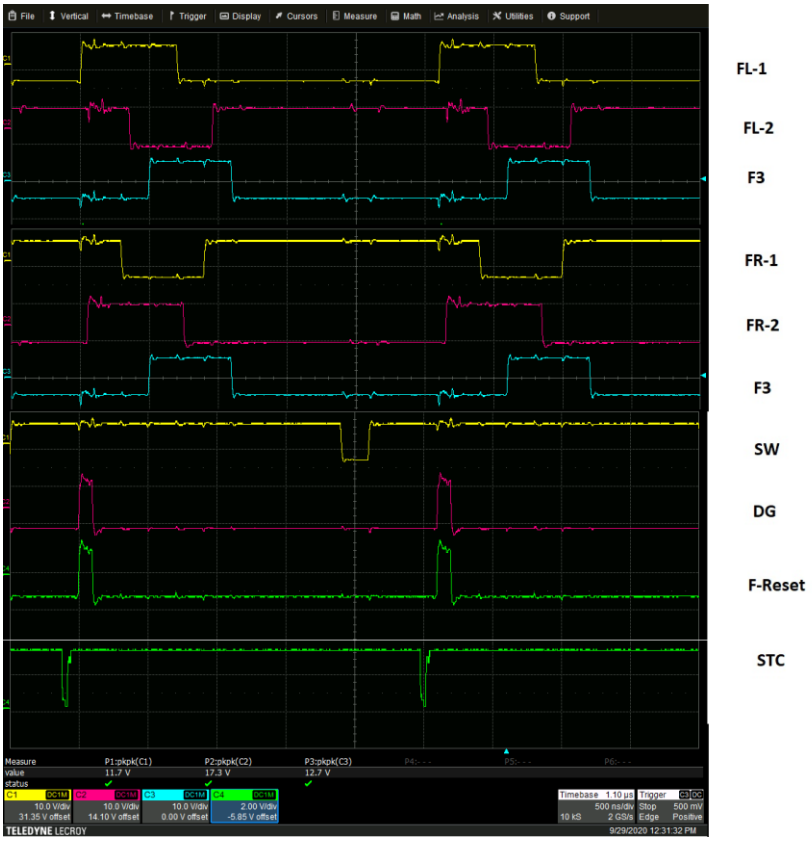


Figure 18 - Serial Left-readout waveforms

Figure 19 - Serial Right readout waveforms

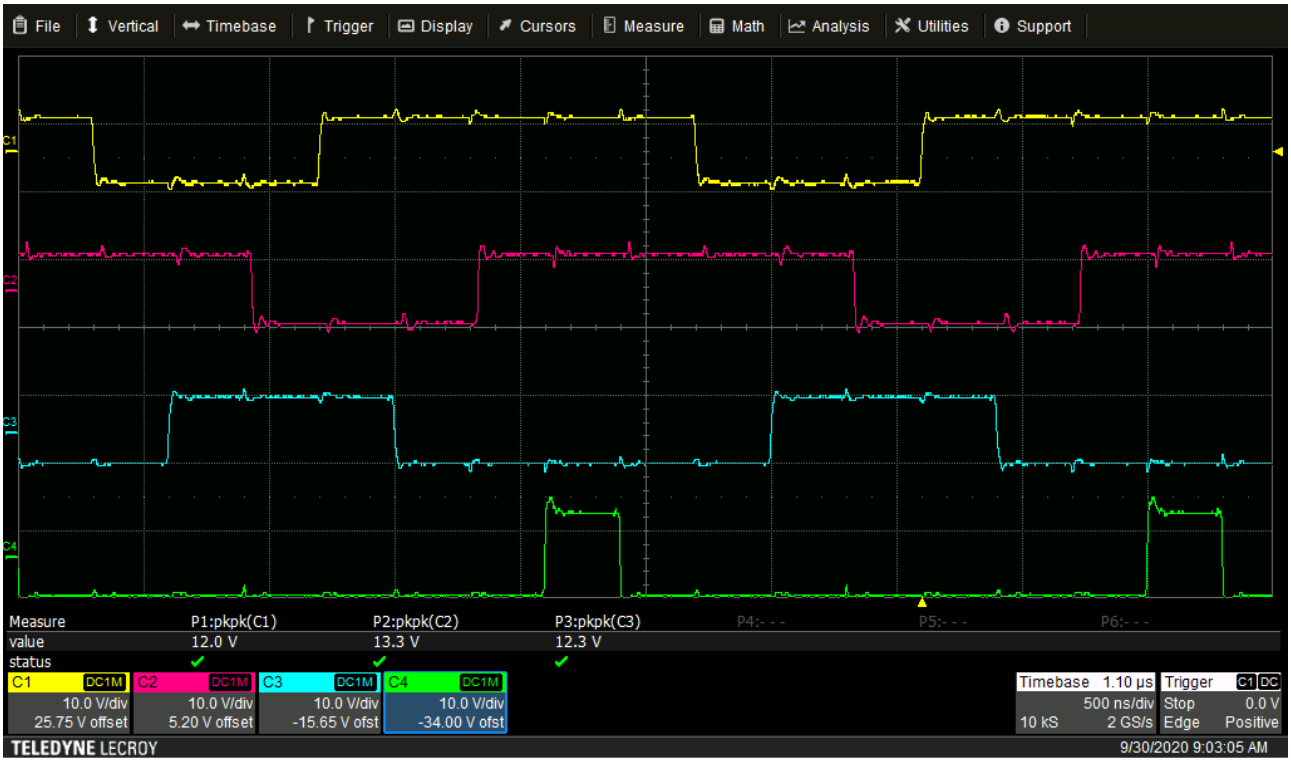


Figure 20 – Wipe Serial register (serial phases)

Figure 21 - Wipe vertical register (parallel phases)

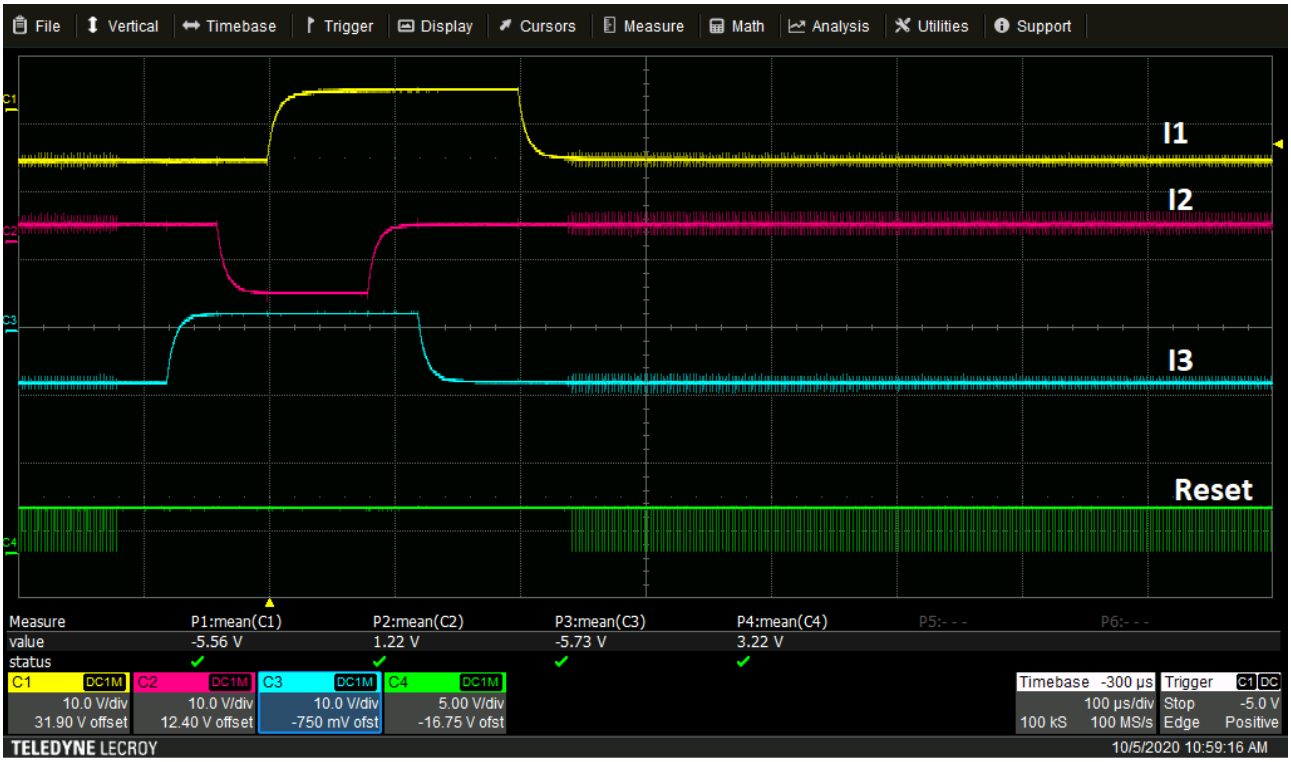


Figure 22 -CCD readout (Vertical details)

The serial RL waveforms has been analysed in different speed mode, to verify the degrading of the waveforms, depending on the speed. CCD acquisition.

8. CCD tests

The CCD e2v 4482 provides two different video signal configurations for each output channels, one direct from CCD output (OSL and OSR) and another buffered with an internal FET (OPL and OPR) [RD01].

To test the different video signals, we connected one configuration to the preamplifier channel #3 and the other to the preamplifier channel #4. In this way we can compare the two configurations and choose the best configuration for SOXS.

Configuration:

- CH#3 – Left CCD output – OSL connected to preamplifier (Figure 23)
- CH#4 – Right CCD output – OPR connected to preamplifier (Figure 24)

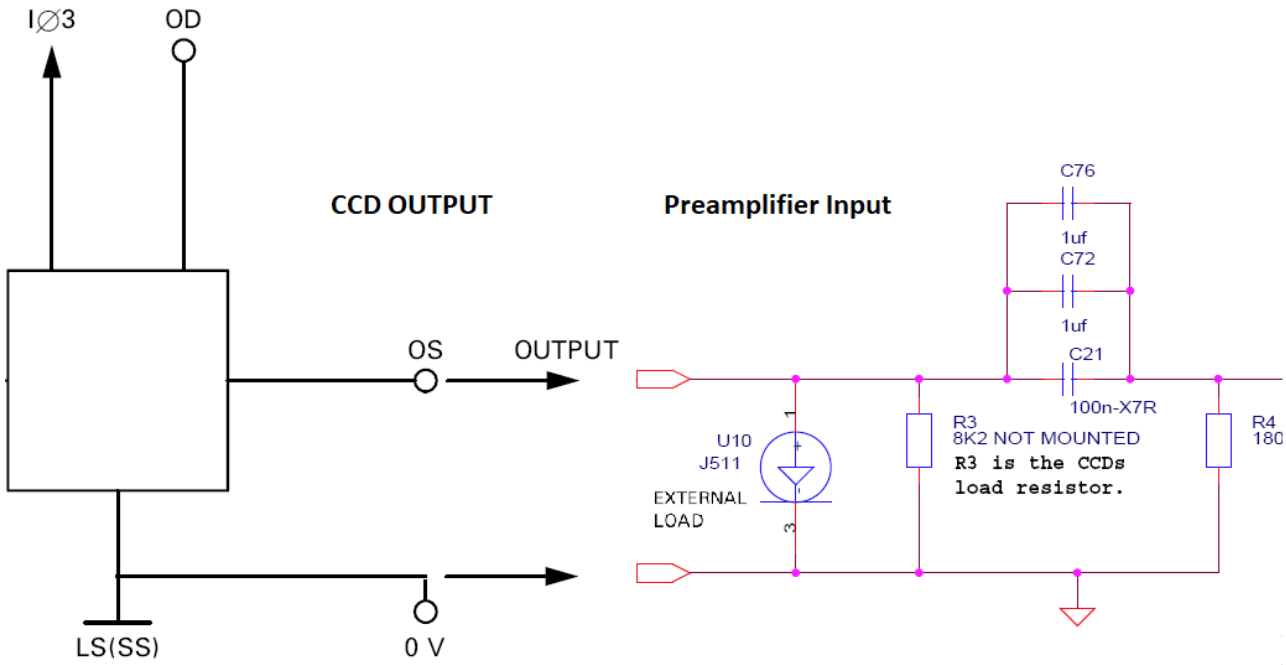


Figure 23 - On the right the ESO preamplifier input and on the left the CCD video output

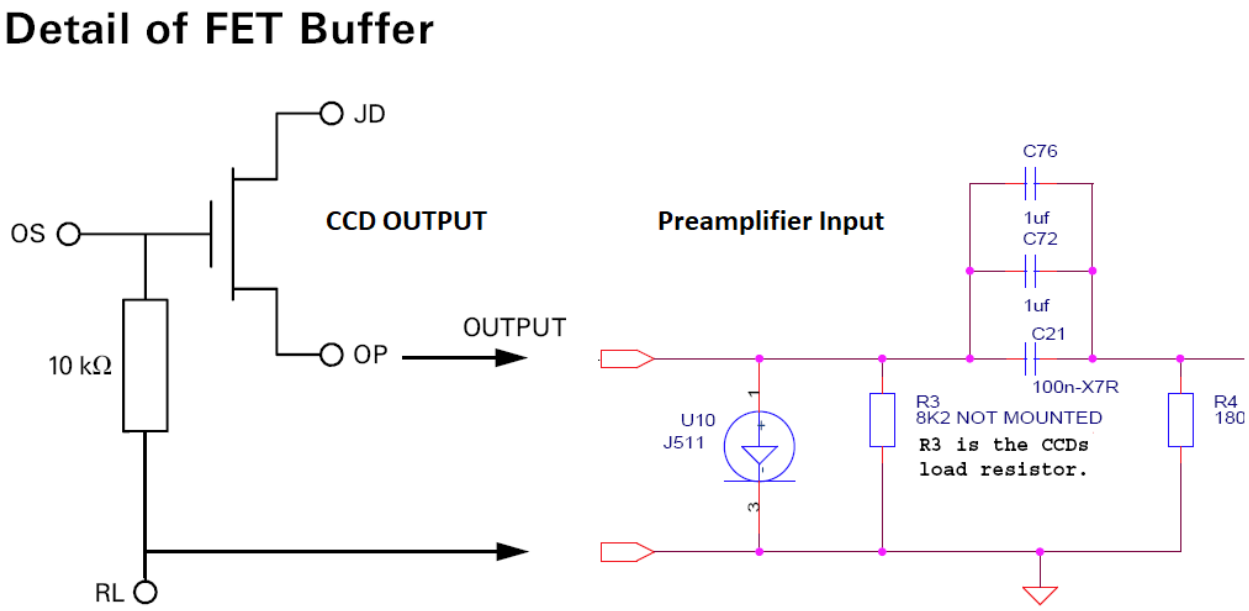


Figure 24 - On the right the ESO preamplifier input and on the left the CCD video output

7.1.1 Engineering CCD at room temperature

In these tests we used a homemade box (Figure 25) as CCD housing and the ESO NGC system Configuration:

- CCD controller NGC
- Preamplifier
- SOXS cables
- Testing bench with the CCD detector

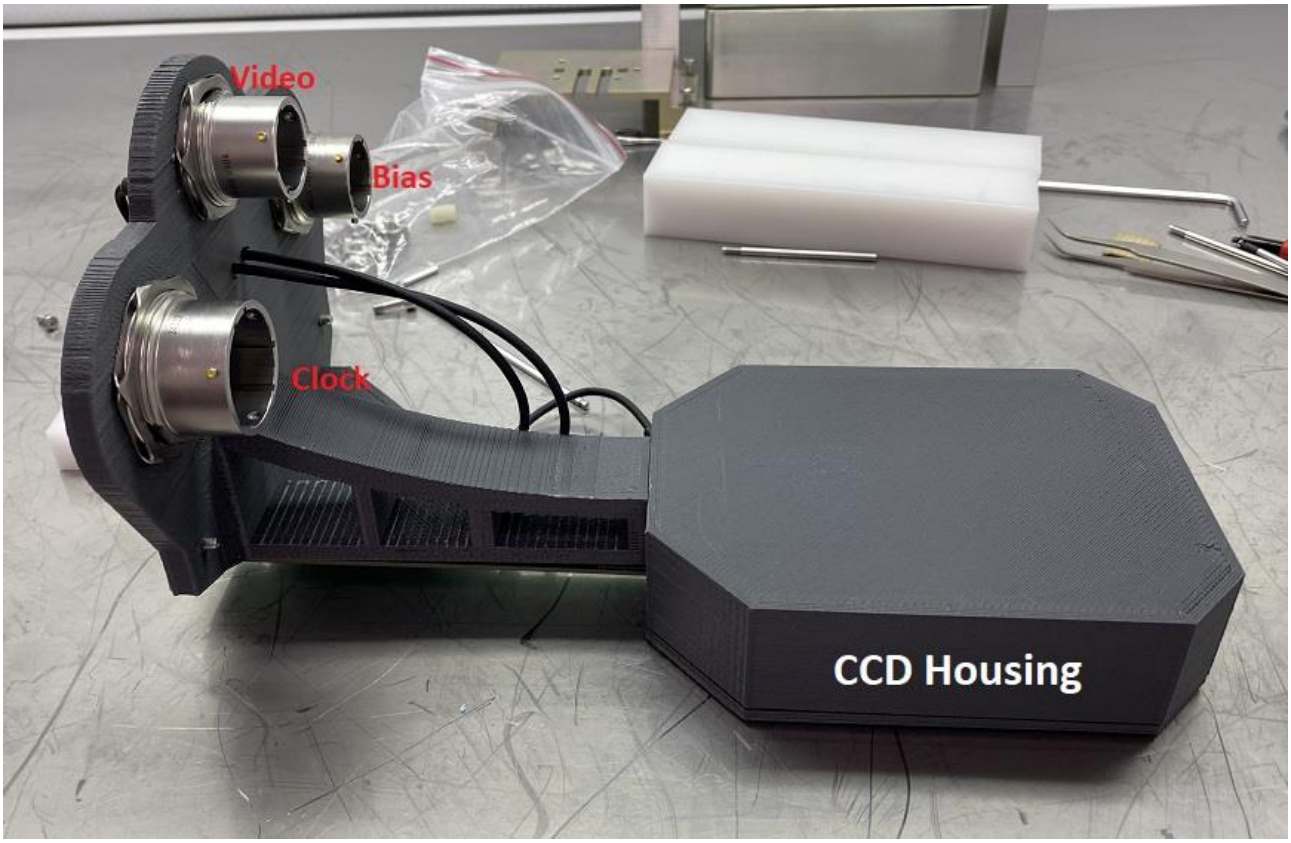


Figure 25 - CCD Test-bench

These tests have been done with an engineering CCD and at room temperature. In this condition is possible verify if the acquisition system works, because the CCD image has to show the overscan and the thermal signal. We have adjusted the video offsets to obtain the wanted value of overscan pixels and we acquired three images, one for each readout mode.

In Figure 26 are shown the CCD images, acquired in the three readouts mode available (Left-Right, Left and Right). In these images the overscan is clearly visible and the images shows the thermic electrons in the images. In this engineering CCD seems that the serial register is broken, because in the images and with more evidence in the horizontal cut (Figure 27) part of the CCD didn´t shown the thermal signal. Further investigation with the scientific CCD will be done to confirm if it is an "engineering CCD" problem or a scan issue.

The acquired images shown that the thermal signal increase with a gradient trend as expected (Figure 28)

To compare the readout noise and the signal we measured these values in two boxes:

- Bias in the overscan box
- Signal in a box in the image area near the output register, to minimize the thermal signal.

The results, shown in Table 9, shown that the best configuration is the buffered CCD output connected to the preamplifier (Figure 24).

More optimization, at cryogenic temperature, should been done.

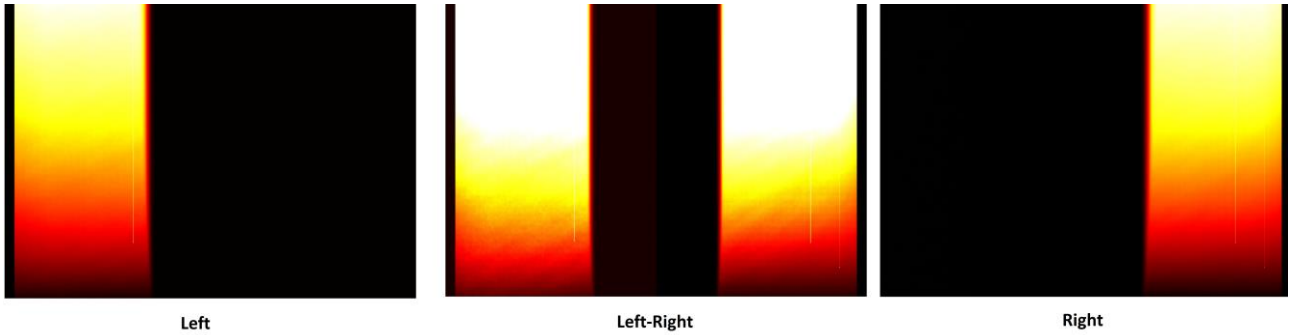


Figure 26 – CCD images for the three readout modes available

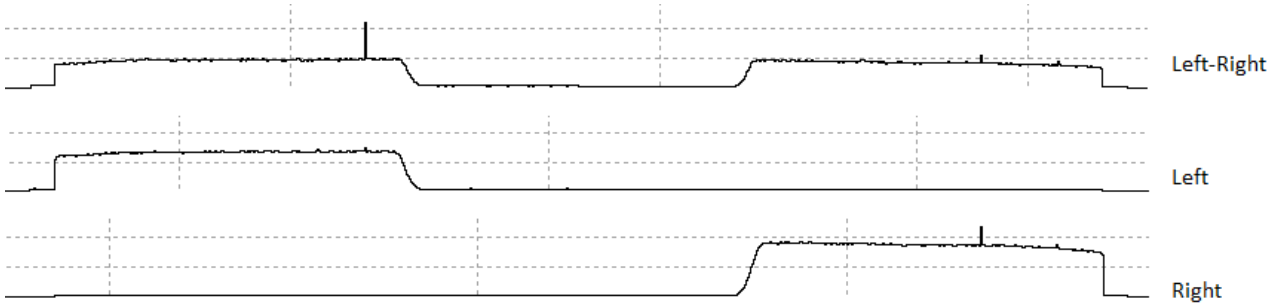


Figure 27 - Horizontal cuts of the three readout modes (the central zone is not read correctly)

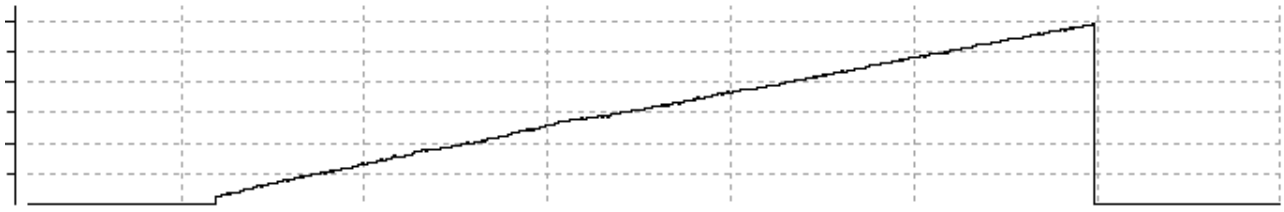


Figure 28 - Vertical cut (thermal gradient)

Table 9 - readout measures at room temperature

Readout Mode	Gain	Bandwidth	CH#3		CH#4	
			Signal	std	Signal	std
left	8	1	4500	30	NC	NC
right	8	1	NC	NC	4000	13
both	8	1	3000	29	2200	13

7.1.2 The test bench

The optical bench for detector tests is made up by some electronics apparatus, located in the optical laboratory, and the control computers, located in the annexed control room.

The source is a Xenon lamp and the light goes through the shutter, the filter wheels and the integrating sphere and come to the SOXS UV-VIS detector (Figure 29).

The filter wheels make available the wavelength from 350 to 1100 nm and the possibility to reduce the flux with neutral filter from ND 0.1 to 4.

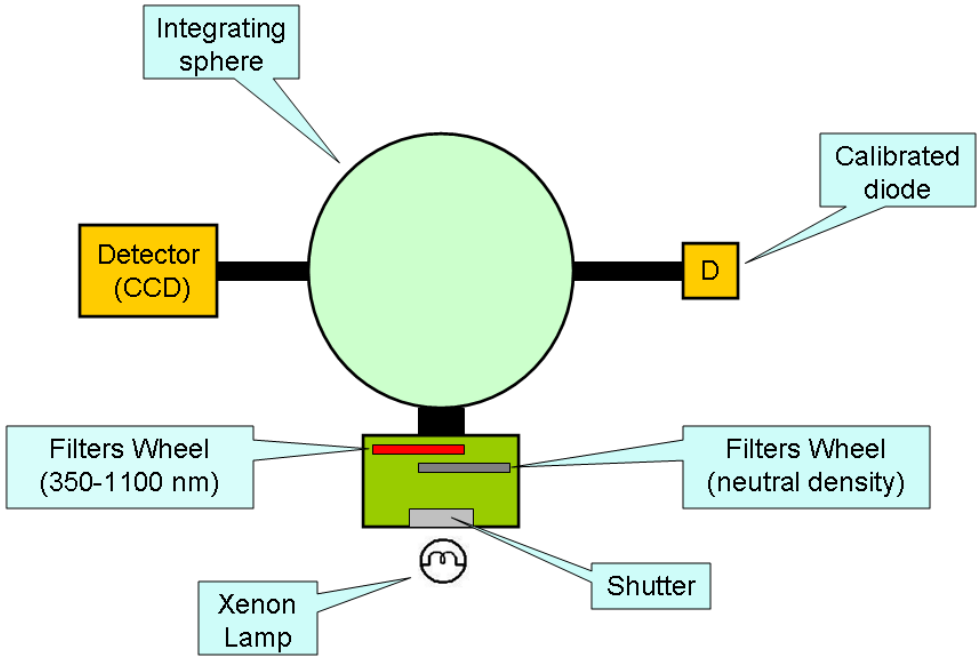


Figure 29 - Setup and test environment (block diagram)

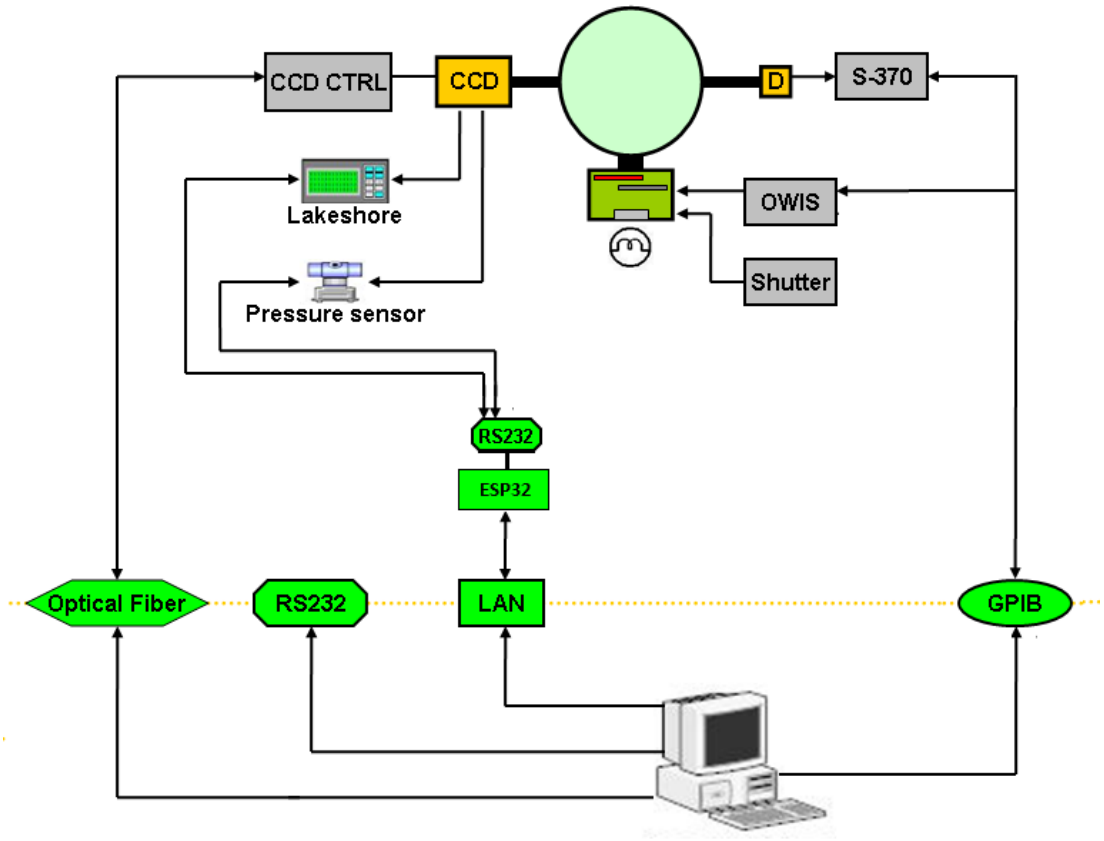


Figure 30 - Setup and test environment (architecture)

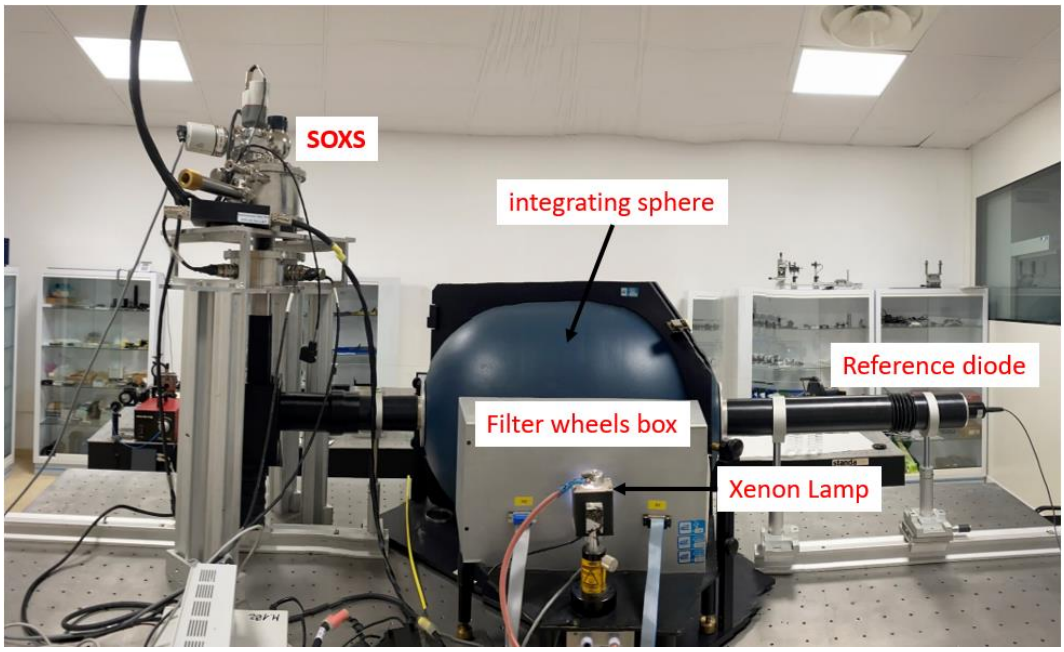


Figure 31 - SOXS detector system test bench

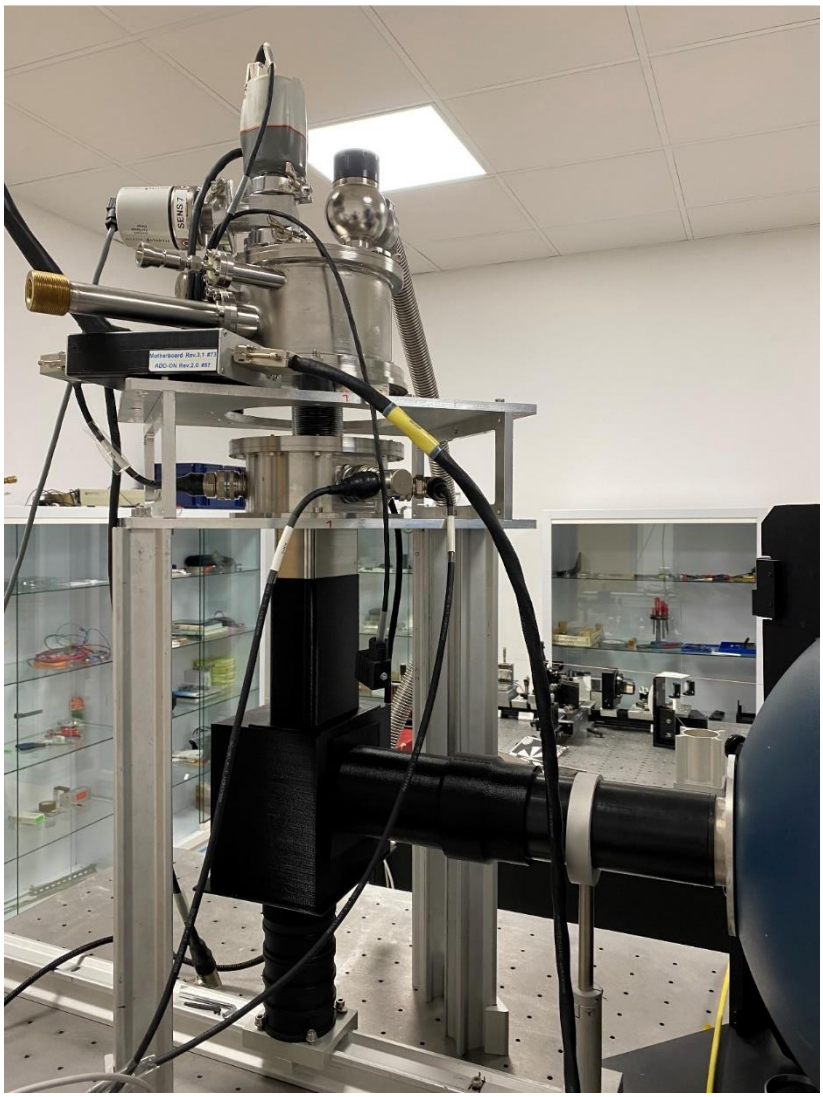


Figure 32 - Detail of the SOXS detector system

7.1.3 Scientific CCD cooled

In these tests, we will test the scientific CCD in the same cryogenic environment foreseen for SOXS.

Configuration:

- NGC controller with video-bias and Clock cables
- Preamplifier
- SOXS camera and scientific CCD
- CFC cooling system with TeePee
- Lakeshore temperature controller
- Optical laboratory facilities

Tests:

- Bias acquisition and video offset settings
- Flat field acquisition at different signal level
- Flat field at different wavelength (350-1100 nm)
- Gain measurements
- Readout noise measurement
- Linearity measurements
- Test of different readout mode
- Test of different binning (1X2, 2X2, 1X4, 2X4)

During the first test with the scientific CCD we realized that the DG (dump gate) clock was not programmed in a correct way because the central part of the CCD shown the same behavior of the engineering CCD (Figure 26). The new scan sequence, with the modified DG, provided the CCD image as we expected (right side of Figure 33)

7.1.3.1 *Gain measurements*

For the gain measurements (conversion factor CF) we used the method based on the assumption that the CCD have a fixed electron noise and the photons measured by the CCD follow the poisson statistic. The CCD is uniformly illuminated at different levels of light and we take several bias and pairs of flat fields for each exposure time. The exposure time is increased and the signal level is measured in ADUs until saturation is reached. The gains calculated for different readout speed and different gains are shown in Table 10.

7.1.3.2 *Readout noise*

The readout noise for the different speeds and gains are calculated on the bias images in ADU and converted in electron (see Table 10). These measurements will be repeated when the acquisition system will be assembled with the spectrograph.

7.1.3.3 *Linearity*

The linearity of the CCD vs the incoming signal was calculated for the different speeds and gains and the results are shown in Figure 34, Figure 35 and Figure 36.

7.1.3.4 *Binning*

Different binnings was tested (1X2, 2X2, 1X4, 2X4) and the results was as expected (no changes in readout noise and gain)

Table 10 - CCD readout modes and characteristics

Readout	Gain left	RMS Left	Gain Right	RMS Right	Readout Time	
	e/ADU	e	e/ADU	e	Full Image	Windowing 740X4096
Both G0	0.8	6.8	0.85	7.5	13	4.73
Both G8	2	9	2	10	13	4.73
Both5 G0	0.85	5	0.9	5	24	8.73
Both5 G8	2	5.2	2	5.8	24	8.73
Both10 G0	0.85	3.7	0.88	4	46	16.73
Both10 G8	2.2	4.5	2.2	4.7	46	16.73

7.1.3.5 *Windowing of the CCD*

The optical design foresee that the illuminated area is the central part of the active area of the CCD (740X4096 pixels). This means that the readout speed can be reduced by using the windowing of the CCD (see last column of Figure 33) with a notable increasing of the performances of the acquisition system. In Figure 33 are shown the simulated image of the spectra in the CCD on the left and the flat field obtained with the CCD chamber with the test bench used to test the detector system.

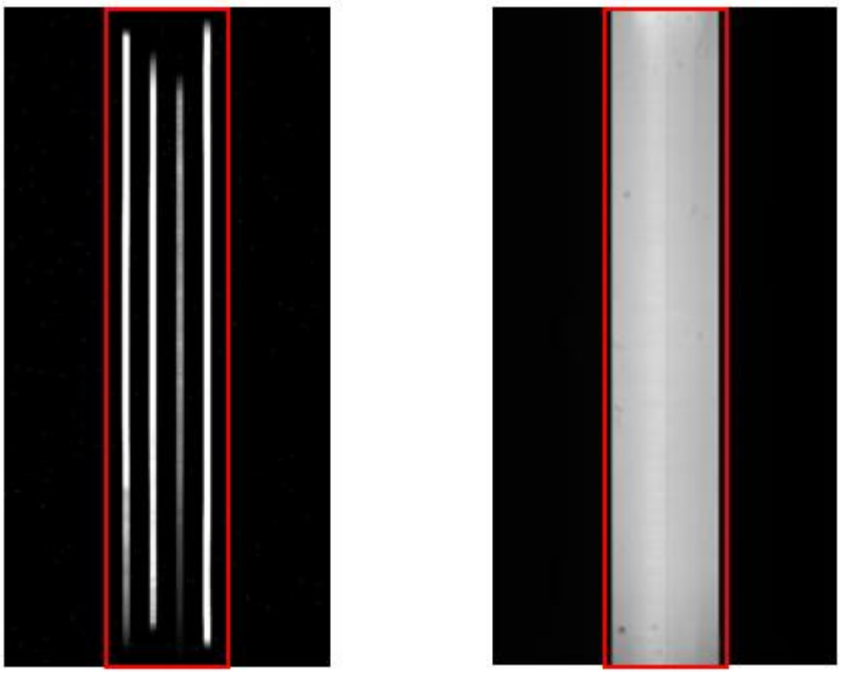


Figure 33 - On the left the simulated spectra and on the right the flat field image

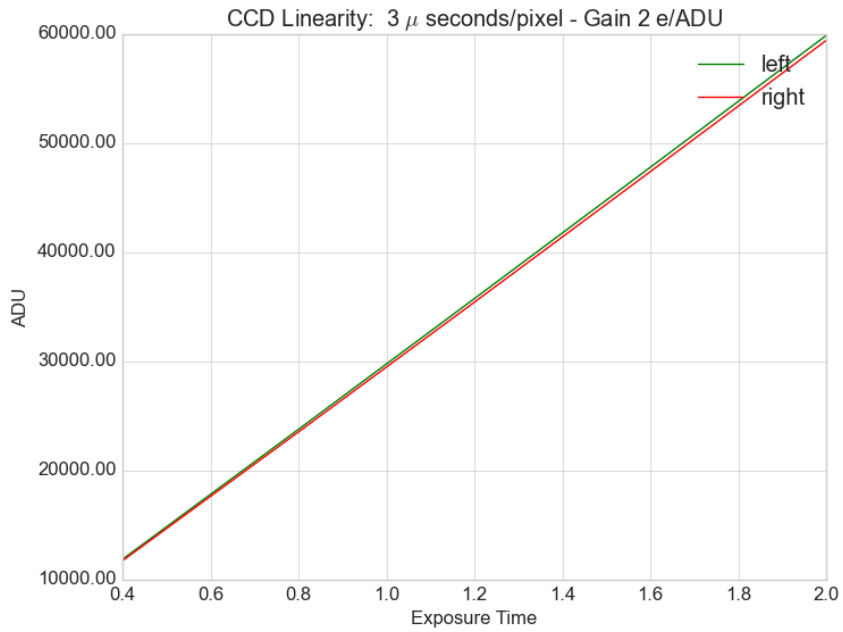


Figure 34 - linearity of fast speed and low gain readout mode

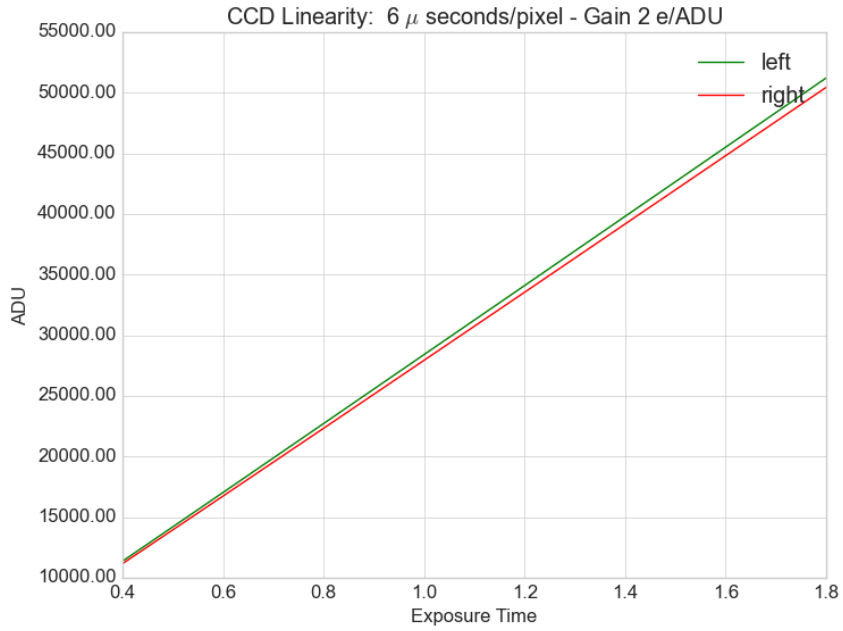


Figure 35 - linearity of fmedium speed and low gain readout mode

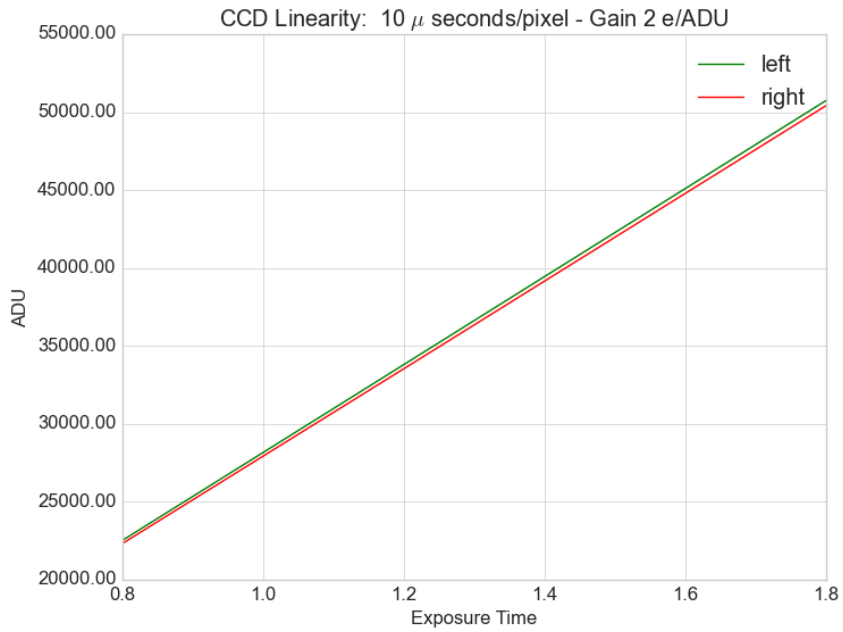


Figure 36 - linearity of slow speed and low gain readout mode

Appendix B – Document identification code

ORG-TYP-INS-NCOD

ORG = Originator field (i.e. TNG)

TYP = Document Type (see Table 11)

PRJ = project element (see Table 12)

NCOD= numeric code (i.e. 0001)

Example: TNG-MAN-HAN-0001

Table 11 - Document type code

AD	Assumption Document
AN	AN Analysis
COS	Cost Documents (Estimate/CaC/CtC, etc)
DD	Design Description
DP	Data Package
DRD	Document Requirements Description/Definition
DRL	Document Requirements List
DW	Drawing/Diagram

EID	Experiment Interface Document
FI	File (Software/Configuration/Network)
ICD	Interface Control Document
IRD	Interface Requirement Document
ITT	Invitation to Tender
MAN	Manual/User Guide/Handbook
MEM	Memo
MOM	Minutes of Meeting
MOU	Agreement/Memorandum of Understanding
MX	Matrix/Compliance
NCR	Non-Conformance Report
NOT	Note
OPS	Operations Document
PLN	Plan
PO	Proposal
PRE	Progress Report/Status Report
RFQ	Request for Quotation
SOW	Statement of Work
TOR	Terms of Reference
TN	Technical Note
TP	Test Procedure/Test Plan
TR	Test Report/Test Result
TS	Test Specification
VC	Verification Control Document
WBS	Work Breakdown Structure
WP	Working Paper
WPD	Work Package Description

Appendix C – Project Element Code

Table 12 – Project element code

BTM	Batman
CCD	CCD detector/electronic/software
HAN	HARPSN
TRK	Tracking
LRS	Low Resolution Spectrograph for TNG
SRG	SARG
SOXS	Son Of XShooter

Appendix D – List of Acronyms

ADU	Analog to Digital Units
CCD	Charge Coupled Device
CDS	Correlated Double Sampling
CF	Conversion factor
DG	Dump Gate
ESO	European Southern Observatory
FET	Field-Effect Transistor
FGG	Fundación Galileo Galilei
INAF	Istituto Nazionale di AstroFisica
INFN	Istituto Nazionale di Fisica Nucleare
JFET	Junction Field-Effect Transistor
ND	Neutral Density
NGC	New General Controller
OPL	JFET source Left
OPR	JFET source Right
OSL	Output source Left
OSR	Output source Right
RMS	Root Mean Square
SOXS	Son Of XShooter
TBC	To Be Confirmed
TBD	To Be defined
TBF	To be fixed
TNG	Telescopio Nazionale Galileo
VIS	Visible
ZIF	Zero Insertion Force