



Publication Year	2020
Acceptance in OA @INAF	2022-02-25T11:11:58Z
Title	The instrument control unit of the PLATO payload: design consolidation following the preliminary design review by ESA
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DOI	10.1117/12.2562003
Handle	http://hdl.handle.net/20.500.12386/31477
Series	PROCEEDINGS OF SPIE
Number	11443

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SPIE.

Event: SPIE Astronomical Telescopes + Instrumentation, 2020, Online Only

The instrument control unit of the PLATO payload: Design consolidation following the preliminary design review by ESA

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ABSTRACT

PLATO is an M-class mission (M3) of the European Space Agency (ESA) whose launch is scheduled in 2026. The main aim of the mission is the detection and characterization of terrestrial exoplanets orbiting around bright solar-type star. The payload consists of 26 small telescopes: 24 “normal” cameras and 2 “fast” cameras. The huge amount of data produced by the PLATO telescopes is acquired and processed on-board by the Data Processing System (DPS) made up by various processing electronic units. The DPS of the PLATO instrument comprises the Normal and Fast DPUs (Data Processing Units) and a single ICU (Instrument Control Unit), are data routed through a SpaceWire network. The topic of this paper is the description of the architecture of the ICU and its role within the DPS, the status of the Avionic Validation Model (AVM) testing at the end of the Unit Preliminary Design Review (UPDR) performed by ESA and the results of the test of the first engineering model.

(Ref. 1–8).

Keywords: Exoplanets, Transit photometry, Large survey, Data Processing System, Instrument Control Unit, Space Mission

1. INTRODUCTION

The PLATO Payload Data Processing System (Figure 1) receives the data from the cameras (normal and fast) and is the responsible of the data processing, data compression and communication with the Service Module.

The ICU, as shown in Figure 1 is the On-board computer, connected with the others subsystem of the DPS (MEU, FEU, AEU) through SpaceWire network. The ICU communicates with the Service Module (SVM) by four SpW links.

In this architecture the SVM links are independent from the DPS spacewire network and all the communication passes through the ICU, except the attitude and orbit control system (AOCS) that interface with the fast DPUs, gathered in one electronic box named FEU (Fast Electronic Unit).

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The Instrument Control Unit (ICU) is in charge of the communication with the service module (commands, data and telemetries), the management of the Data Processing System (DPS) and the compression and transmission of the scientific data from the subsystem of the DPS.

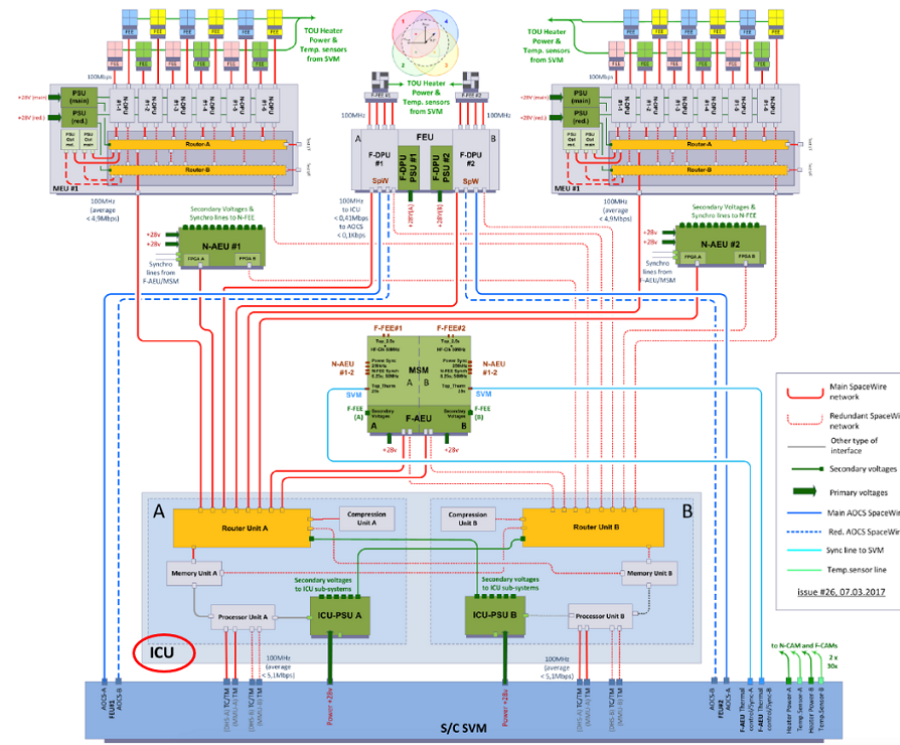


Figure 1. PLATO DPS architecture.

2. THE INSTRUMENT CONTROL UNIT (ICU)

The role of ICU is very critical because this unit is the only interface between the PLATO SVM and the mission payload and any fail in the ICU would compromise the entire mission. To minimize the risks, the ICU is made up by two identical chains, working in cold redundancy, as shown in Figure 1.

Others critical points are the complexity and the high number of the SpW link, the amount of data and the capacity requested.

The most important design challenges are:

- efficient data handling (scientific data, TM and HK);
- efficient data compression ;
- harness complexity;
- mass and power limitation.

Considering the high amount of data and the needed data rate, the communication is based on a SpaceWire network.

The two chains of the ICU, nominal and redundant, are integrated in one single box, the design architecture consists of three nominal plus three redundant modules/PCB made up by:(see paragraph 3.2)

- Power supply Unit (PSU);
- Processor and Memory Unit (CPU/MMU);
- Router and Data Compressor Unit (RDCU);
- Back-Plane (BP).

The design and development of the RDCU board is under responsibility of IWF of Graz (Austria) while the other boards are in charge of Kayser Italia.

The main functions of the ICU are the following:

- communicate with the spacecraft (S/C) via SpW links for telecommands and telemetry;
- execute telecommands and forward them to the other PLATO DPS;
- collect scientific and housekeeping data from the DPUs, both normal and fast;
- compress scientific data and send them to the S/C;
- monitor the status of the payload and provide it as telemetry;
- perform FDIR procedures for PLATO payload.

3. THE MODEL PHILOSOPHY

The model philosophy is based on the realization of some customized models, following the European standard system (ECSS). The first model for the validation of the hardware and for the Preliminary Design Review (PDR) is the Avionic Model (AVM, not delivered to the PLATO consortium).

Different models are foreseen for the ICU:

Two Engineering Models (EM):

- Engineering model - EM#1 with only the nominal unit (A);
- Engineering model - EM#2 with the nominal and redundant units A+B.

One Engineering Qualification Model (EQM):

- Engineering qualification model (EQM) - with the nominal and redundant units A+B.

One Flight Model:

- Protoflight model (PFM) - with the main and redundant units A+B.

In this paper we describe the AVM and the EM#1 models and their role in the model philosophy of the ICU.

3.1 The avionic model (COTS component)

In order to validate the ICU design and to develop the first release of the Application Software (ASW), the hardware of the AVM has to be as representative the EM and EQM.

The AVM is based on an industrial PCI bus, a commercial power supply and three boards: The CPU board, the memory board (MMU) and the router and compression board (RDCU) as shown in Figure 2. The CPU and memory boards are splitted only within the AVM, while in the following models are join together in the CPU/MMU board.

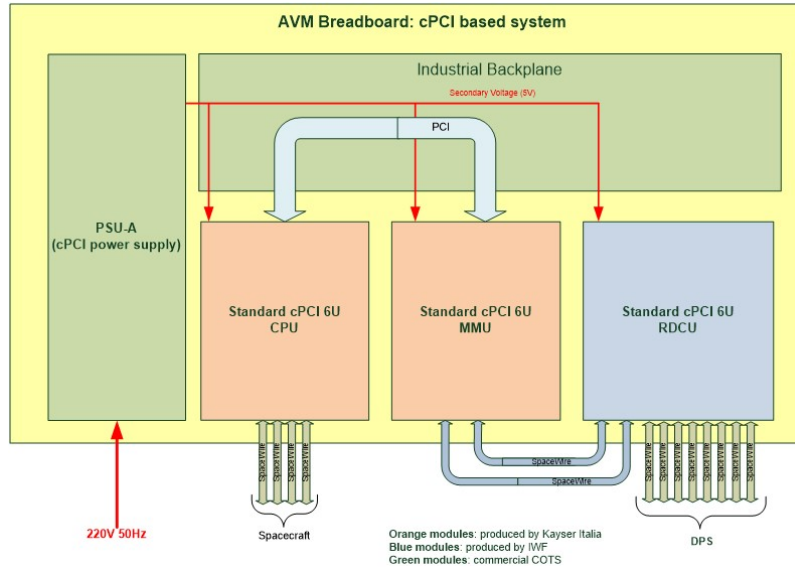


Figure 2. avionic model architecture

With the AVM model the ICU team developed the first version of the software in order to test the hardware itself and to validate the unit with the EGSE.

The software (Figure 3) is made up by:

- the boot software (BSW)
- the board support package (BSP)
- the application software (ASW)

The ICU BSW and the BSP are under responsibility of Kayser Italia, while the ASW is in charge of INAF (Inst. of Space Astrophysics and Planetology).

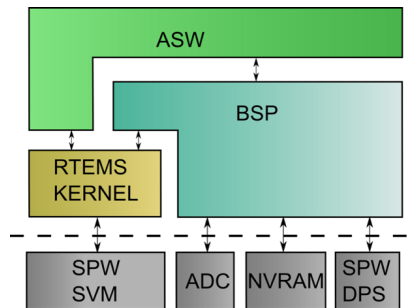


Figure 3. ICU software architecture

To test the ICU along its overall life cycle, a customized EGSE was developed by the PLATO Mission Consortium (PMC).

The EGSE for the AVM allows the validation of the ICU by providing a representative connection architecture towards the real hardware. From the spacecraft side the Spacecraft Interface Simulator (SIS) allows the simulation of the communication of data and telecommands between the ICU and the satellite while the subsystem simulator (SIMUCAM) provides the spacewire links that simulates the connection with the DPS subsystems.



Figure 4. On the left the DPS simulator (SIMUCAM) on the right the spacecraft simulator (SIS)



Figure 5. Avionic Model (ICU AVM)

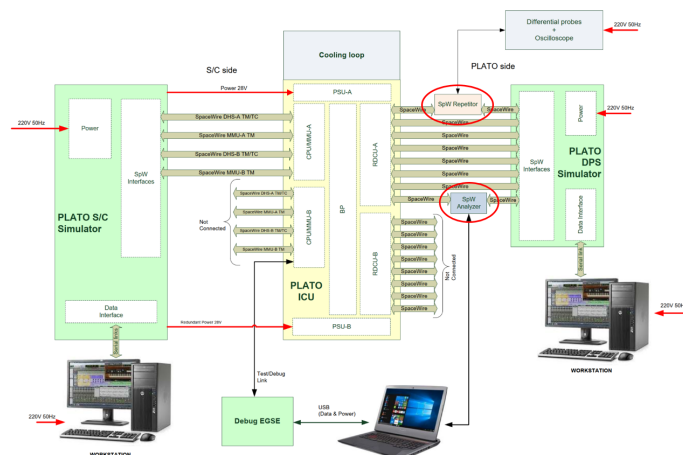


Figure 6. EGSE architecture

The AVM was tested successfully: the hardware was tested in standalone mode and with the Spacecraft simulator (SIS), the boot software (BSW) was validated and the functionality of the board support package (BSP) was verified with a preliminary version of the application software (ASW). Following the acceptance of the unit, the AVM was used by the ICU team for the development of the first official version of the ASW, in parallel with the development of the EM#1, in order to test and delivery the EM#1 model of the ICU together with the first version of the application software (ASW v0.4).



Figure 7. AVM tested with the EGSE

3.2 The engineering model

The EM#1 is the first model of the ICU to be used for the integration and functional test on DPS level, for the performance test and for the development of the ASW. In this model the CPU and the memory board (MMU) are join together in the CPU/MMU board as shown in Figure 10. In the EM#1 (see Figure 12) the mechanics and the hardware are comparable with the flight model. With this model we estimated better the mass and the power consumption of the unit for the verification of the complies with the payload budget. This model will be used for the electrical and interface tests of the nominal chain of the ICU in the DPS.

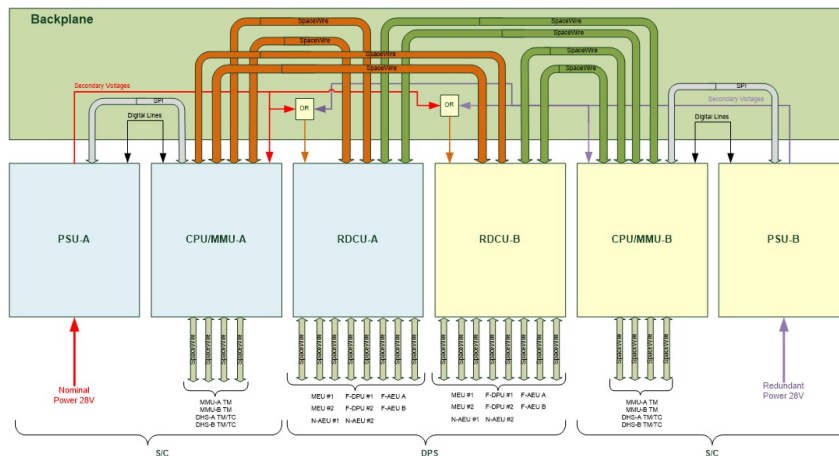


Figure 8. ICU architecture

3.2.1 The back-plane

The back-plane (upper part of Figure 8) allows the power distribution and the data sharing between the nominal and redundant modules. The backplane hosts the connectors for all the ICU boards, acting as a routing board for power, digital and analogue signals. It represents the mean through which the nominal and redundant boards are connected and share the power and signal lines with each other. Thanks to the use of the back-plane, all the I/O connectors are directly mounted on the relevant PCB modules and there are no wired connections inside the unit.

3.2.2 The power supply unit

The power supply unit (PSU) receives the 28V from the S/C and it provides the secondary supply voltages to the other modules, does the A/D conversion of the HK and provide the over-voltage and over-current protection. (Figure 9).

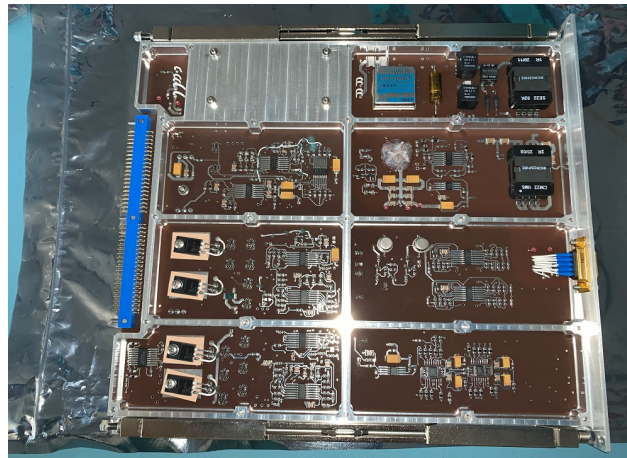


Figure 9. Power Supply Unit

3.2.3 The processor and memory unit

The processor and memory unit (CPU/MMU) is the main data-processing module of the ICU. It is responsible for payload control and for interfacing the S/C for telecommands and telemetry by means of 4 nominal SpW links (Figure 10).

This board is based on the UT700 (LEON3FT) SPARC V8 microprocessor, produced by Cobham, running at 133 MHz, as required by the processing needs and SVM I/Fs requirements. The processor has 4 embedded SpW links allowing to directly communicate with the S/C SVM, with dedicated driver/receiver interface ICs.

The UT700 microprocessor is connected to the following memories:

- 128kB of PROM: it is used to store the Boot Software (BSW);
- 16MB of MRAM: it is used to store permanently different images of Application Software (ASW) of ICU and external DPUs as well as parameters and data (e.g. the star catalogue);
- 512 MB of SDRAM: it is used to run the ASW and as buffer for data transfer;
- SDRAM memories are EDAC protected by the memory controller of UT700 with a bus of 48 bits wide (32+16 bits for EDAC function with Reed Solomon algorithm).

Due to the selected SDRAM devices and the Processor features, UT700 is able to address only 512 Mbyte of data.

To reach the required total mass memory of 1 Gbyte a FPGA is used to interface other 512 Mbyte of SDRAM in order to expand the processing, communication and storage capabilities of the processor implementing another SDRAM controller and additional SpW links, including DMA controllers, to perform high data transfer from/to RDCU.

In conclusion, the CPU/MMU board supports 8 SpW links (4 SpW to the S/C and 4 to the internal RDCUs) and 1 Gbyte of volatile mass memory as required by the data volume assessment and buffering/processing needs.

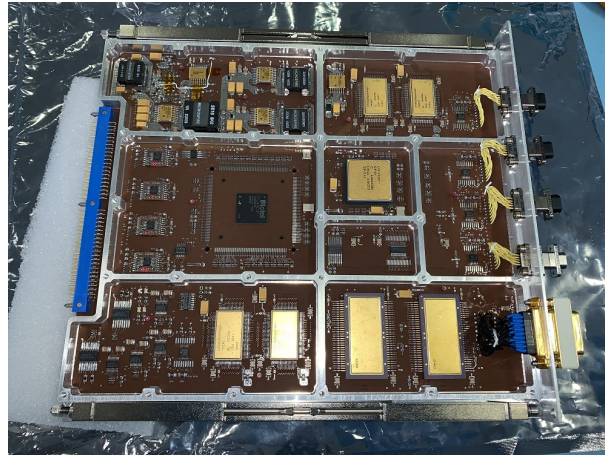


Figure 10. CPU and memory board (CPU/MMU)

3.2.4 The router and data compressor unit

The router and data compressor unit (RDCU) implements a SpW router to put in communication the CPU/MMU module with the rest of PLATO DPS and it performs a HW compression (on imagerettes only) in order to reach the performance requirements of the ICU (Figure 11).

Due to the number of data links to be handled, the ICU router unit implements an 18-channel SpW router (the GR718B from Cobham-Gaisler) with radiation hardness characteristics (i.e. dedicated to the on-space use). The SpW router board is capable of handling the data streams from the CCD detectors to the ICU in an effective and fast way. The SpW network configuration can be set-up via RMAP commands from the ICU CPU to the router component and the associated control FPGA.

As the SW compression of all the PLATO P/L scientific products (fluxes, centroids, imagerettes, etc.), performed by the ICU processor alone, has been previously demonstrated not feasible, the introduction of an HW compression engine for the imagerettes only, will reduce the computational power required by the CPU, to be addressed and devolved mainly to the overall instrument control task.

The HW compressor module manages the lossless compression of the imagerette following the following processes:

- the imagerettes coming from the DPS SpW network are firstly routed to the CPU/MU board and, from its SDRAM memory, back to the HW compressor engine that performs the compression task and stores the compressed data in a SRAM buffer. The processor can then retrieve the compressed imagerettes and write them back in the CPU SDRAM memory, waiting for the time-slot scheduled for the required science data packetization for TM towards the SVM.

In conclusion, the RDCU communicates effectively with the PLATO DPS by means of 8 SpW links and with the two CPU/MUs thanks to 4 SpW links and manages the data compression of the imagerette coming from the DPS with a minimum compression ratio of 2 .



Figure 11. Router and compression unit (RDCU)

3.3 engineering model validation

The EGSE for the EM#1 is the same used in the AVM validation: The SIS is used on the spacecraft side and the SIMUCAM to test the DPS. To validate the unit, several script has been written, in order to test the ICU EM#1 together with the first official version of the application software (ASW). The validation test of the EM#1 includes all the HW test, BSW test and BSP test as in the AVM model and in addition all the test requested by the specification on the services implemented in the ASW v0.4 in order to demonstrate the compliance of ICU respect to the requirements verifiable by test defined in the procedure documents.

The EM#1 was tested successfully: the hardware was tested in standalone mode (Figure 12) and with the spacecraft simulator (SIS), the boot software (BSW) was validated and the functionality of the board support package (BSP) was verified with the version 0.4 of the ASW (aggiungere figura del EGSE con EM#1).

After the acceptance of the EM#1 (Figure 13) the model was delivered to DLR for the integration in the data processing system and for the validation of the DPS. The results of these test will be used for the development of the following version of ASW and to fix the bugs of the version 0.4.

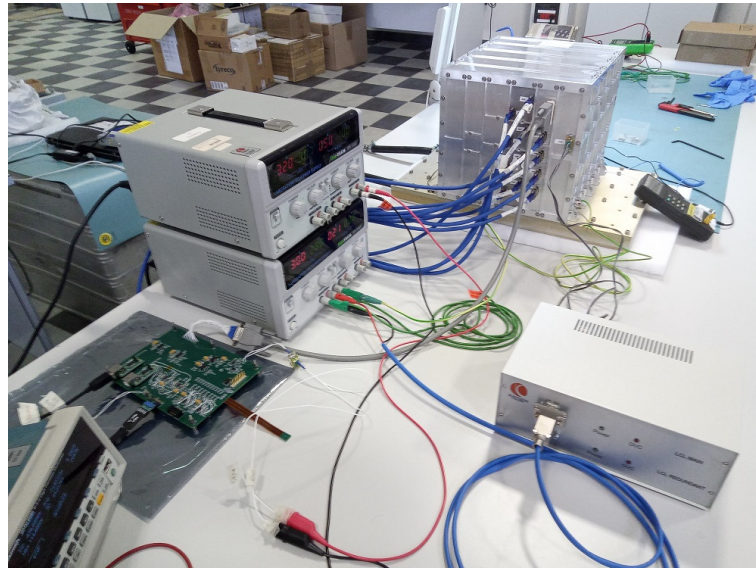


Figure 12. EM#1 EGSE

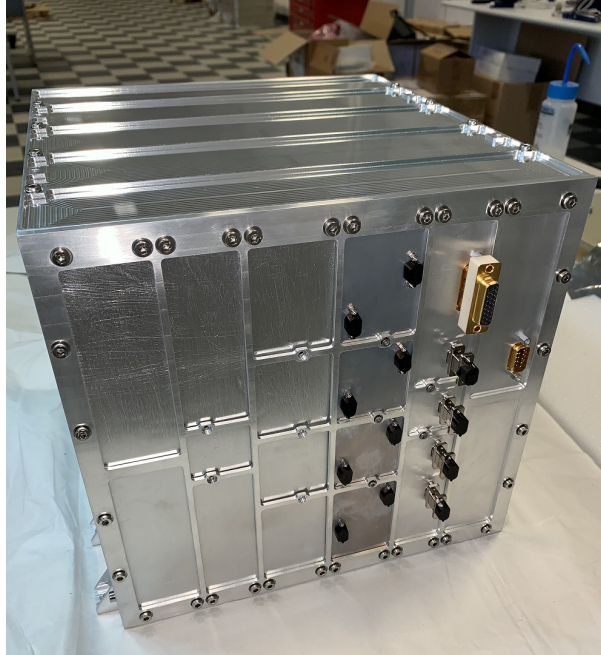


Figure 13. The ICI EM#1

4. CONCLUSION

The ICU models described in this paper relies on an efficient design to reach the performances requested by the requirement documents. All the foreseen tests on the AVM and EM#1 were done successfully in according with the procedure document and the units was accepted and delivered to PCM/DLR.

At the present time, due to several iterations between ESA and the PLATO Mission Consortium (PMC) we decided to anticipate the Critical Delta Review (CDR) to minimize the risks associated to the EQM model manufacturing and test. Next step will be the development of the EM#2 model that will be tested in February 2021 and the preparation for the CDR activities that will take place in April-June 2021 time-frame.

ACKNOWLEDGMENTS

A special acknowledgement to the European Space Agency for the support provided by the PLATO Team and to DLR leading the PLATO Mission Consortium. This work has been funded thanks to the Italian Space Agency (ASI) support of the Project, as defined within the ASI-INAF agreement n. 2015-019-R.O. "Scientific activity for the PLATO Mission - B/C Phases".

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