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CHANGE RECORD

Issue	Date	Sheet	Description of Change	Release
1	May 99	All	First Issue of the document	
2	Sep. 99	5-7 10 26 57 71-82	List of Reference Documents updated Updated sections: 4.2 - EMCH Description (Fig.4.2-2) 5.2.2 - EMAE Functional Description 6.3.10 - Overall Thermal Control System Description New sections 9.4-5 introduced (Commissioning and LEOP Procedures)	

TABLE OF CONTENTS

1. INTRODUCTION

1.1 PURPOSE

The purpose of this document is to provide a concise but clear and comprehensive definition of the design, interface and operational characteristics associated with the control of the **E**PIC **M**OS **C**amera **S**ystem (**EMCS**) in flight.

1.2 THE EPIC EXPERIMENT

The **E**uropean **P**hoton **I**maging **C**amera (**EPIC**) experiment will be flown on the ESA XMM (X-ray Multi-mirror Mission) satellite and consists of four systems:

- Two EPIC MOS Camera Systems (*EMCS*);
- One EPIC PN Camera System (*EPCS*); and
- One EPIC Radiation Monitoring System (*ERMS*).

The camera systems will investigate faint x-ray sources in the spectral region 0.1 - 15 keV. The detectors of the three camera systems are placed on the focal planes of three XMM telescopes, one camera head per telescope. The ERMS measures continuously the space radiation environment providing broad band count rates and energy spectra above 50 keV for electrons and 5 MeV for protons.

1.3 ACRONYMS

AD	Application Document
AOCS	Attitude and Orbit Control System
APID	Application Identifier
BOL	Beginning of Life
CAL EGSE	Calibration EGSE
CAL MOGSE	Calibration MOGSE
CCD	Charge Coupled Device
CDMS	Command and Data Management System
ED-EGSE	ESA-Deliverable EGSE
ED-MGSE	ESA-Deliverable Mechanical Ground Support Equipment
EGSE	Electronic Ground Support Equipment
EMAE	EPIC MOS Analogue Electronics
EMC	Electromagnetic Compatibility
EMCH	EPIC MOS Camera Head
EMCR	EPIC MOS Control & Recognition (Unit)
EMCS	EPIC MOS Camera System
EMDH	EPIC MOS Data Handling (Unit)
EMI	Electromagnetic Interference

EMVC	EPIC MOS Voltage Converter (Unit)
EOL	End of Life
EPCS	EPIC p-n Camera System
EPIC	European Photon Imaging Camera
EQM	Engineering and Qualification Model
ERMS	EPIC Radiation Monitor System
EST	EPIC System Team
FID	Function Identifier
FIT	Failure Inverse Time
FM	Flight Model
FMECA	Failure Mode Effect and Criticality Analysis
GSE	Ground Support Equipment
HBR	High Bit Rate
H/K	HouseKeeping
ICD	Interface Control Document
IC-EGSE	Integration and Calibration EGSE
LBR	Low Bit Rate
LEOP	Launch and Early Orbit Phase
LSB	Least Significant Bit
MFN	Master Function Number
MID	Memory Identifier
MOGSE	Mechanical/Optical Ground Support Equipment
MOS	Metal-Oxide Semiconductor
MSB	Most Significant Bit
OBDH	On-Board Data Handling
PFC	Parameter Format Code
PI	Principal Investigator
PID	Parameter Identification Number
PKT	Packet
PREF	Parameter Reference Number
PSD	Packet Structure Definition
PTC	Parameter Type Code
RD	Reference Document
SCET	Spacecraft Elapsed Time
SDB	Satellite DataBase
SID	Structure Identifier
SMP	Science Mission Phase
SOW	Statement of Work
STM	Structural Thermal Model
S/C	Spacecraft
TC	Telecommand
TE	Test Equipment
TID	Task Identifier
TM	Telemetry
TPN	Telemetry Packet Number
XMM	X-Ray Multi-Mirror Mission

2. APPLICABLE AND REFERENCE DOCUMENTS

2.1 APPLICABLE DOCUMENTS

All the documents listed in this Section shall be applicable to the extent agreed upon by ESA and the EPIC P.I.. In case of conflict between this document and the documents listed herebelow, precedence shall be given to the documents listed herebelow. When no issue number is specified, the latest issue published before the date of issuance of this document shall be considered.

[AD 1]	RS-PX-0016	I. 6	X-Ray Multimirror Mission, Experiment Interface Document, Part A, ESA.
[AD 2]	RS-PX-0020	I. 5	X-Ray Multimirror Mission, Experiment Interface Document, Part B, ESA.
[AD 3]	RS-PX-0024	I. 1	X-Ray Multimirror Mission, Experiment Interface Document, Part C, ESA.
[AD 4]	RS-PX-0017	I. 1	Product Assurance Requirements for XMM Experiments, ESA.
[AD 5]	RS-PX-0028	I. 6.0	XMM Operations Interface Requirements Document, ESA
[AD 6]	RS-PX-0032	I. 5.4	Packet Structure Definition. ESA

2.2 REFERENCE DOCUMENTS

All the documents listed in this Section shall be considered as a guideline to the extent established in this document. In case of conflict between this document and the documents listed herebelow, precedence shall be given to this document. When no issue number is specified, the latest issue published before the date of issuance of this document shall be considered.

Note: The Documents with hyperlink are available in the present User Manual and those marked with (*) are in pdf format.
The Documents without hypelink are only available, at the date of the present issue, "on paper"

[RD 1]	EPIC-LUX-TN-011		The Epic Filter Wheel System (*)
[RD 2]	EPIC-LUX-DD-001	I1	Design Document of the Epic Mos Camera Head
[RD 3]	EPIC-LUX-EQ-048	I.1	Requirement Specification for the EPIC MOS Camera Head (EMCH), LUX

[RD 4]	EPIC-BUX-TN-017	I.5	Vacuum Door Opening and Closure Procedures
[RD 5]	EPIC-MMS-EQ-001	I.1.	Equipment Functional Specification for the EPIC MOS Analogue Electronics (EMAE), MMS (*)
[RD 6]	EPIC-MMS-RE-001	I.1.	Design Report for the Epic Mos Analogue Electronics.
[RD 7]	EPIC-MMS-AN-005	I.2.	Failure Mode, Effects and Criticality Analysis for Epic EMAE.
[RD 8]	EPIC-MMS-IF-001	I.2.	Command Address Allocation for the EMAE
[RD 9]	EPIC-MMS-IF-003	I.4.	XMM EMAE Interface Control Data
[RD 10]	EPIC-SAP-RS-001	I.4.0	Unit Requirement Specifications for the Epic Mos Control and Recognition Unit (EMCR), SAP
[RD 11]	EPIC-SAP-DD-001	I.2.0	Unit Design Document for the EPIC MOS Control and Recognition Unit (EMCR), SAP
[RD 12]	EPIC-SAP-OP-001	I.5	Operating Manual for the CTR EMCR Unit
[RD 13]	EPIC-SAP-SP-003	I.10	Software Requirement Document for the CTR EMCR Unit
[RD 14]	EPIC-SAP-SD-001	I.4	Software Architectural and Design Document for the CTR EMCR Unit
[RD 15]	EPIC-LAB-SP-002	I.5	Requirement Specification for the EPIC MOS Data Handling Unit (EMDH), LABEN
[RD 16]	EPIC-LAB-TN-008	I.4	EPIC MOS Data Handling (EMDH) Unit Description
[RD 17]	EPIC-LAB-ID-008	I.1	Epic EMDH Unit Interface Control Document
[RD 18]	EPIC-LAB-ID-005	I.3	EMDH Hardware/Software Interface
[RD 19]	EPIC-LAB-AN-002	I.2	EMDH Failure Mode Effects and Criticality Analysis
[RD 20]	EPIC-LAB-SP-003	I.4	Baseline Document for Software Requirements of the Epic Mos Data Handling Unit (**Part A**)
[RD 20]	EPIC-LAB-SP-003	I.4	Baseline Document for Software Requirements of the Epic Mos Data Handling Unit (**Part B**)
[RD 21]	EPIC-LAB-SA-003	I.3	Sofware Architecture Design Document (ADD) for the EMDH Unit

[RD 22]	EPIC-LAB-OP-007	I.2.	Sofware User Manual – Telemetry Details for the Epic MOS Data Handling Unit
[RD 23]	EPIC-LAB-LI-022	I.4	EMDH Sofware CIDL.
[RD 24]	EPIC-SAP-SP-001	I.2.2	Requirement Specification for the EPIC MOS Voltage Converter (EMVC), SAP
[RD 25]	DES.EMVC.CI.0088	I.0/A	Dossier de Controle des Interfaces
[RD 26]	DES.EMVC.DE.0077	I.0	Rapport de Synthese d'Etude
[RD 27]	DES.EMVC.RQ.0037	I.0/B	AMDEC Bloc Functionnel (FMECA)
[RD 28]	EPIC-LAB-SR-002	I.4	Requirement Specifications for the Epic Mos Camera System
[RD 29]	EPIC-EST-SP-001	I.4	EMCS Electrical Interface Specifications
[RD 30]	E.XXM.6600	I.K	EMCH 1 I.C.D.
[RD 31]	E.XMM.6601	I.K	EMCH 2 I.C.D.
[RD 32]	E.XMM-6882	I.E	EMPS I.C.D.
[RD 33]	E.XMM.6602	I.G	EMAE I.C.D
[RD 34]	E.XMM.7178	I.C	EMCH/EMAE/EMHA 1 Unit EMCH1 I.C.D.
[RD 35]	E.XMM.7182	I.C	EMCH/EMAE/EMHA 2 Unit EMCH2 I.C.D.
[RD 36]	M5707	I.D	Epic Boitier EMCR Mechanical I.C.D.
[RD 37]	DIS.TLD.3884.ICD	I.G	Epic Mos Data Handling I.C.D.
[RD 38]	79139780	I.D	EMVC I.C.D.
[RD 39]	EPIC-EST-SP-005	I.1	Basic requirements for processing of EPIC science telemetry
[RD 40]	EPIC-LAB-SD-001	I.1	SW Detailed Design Document (DDD) for the EMDH Unit

3. EXPERIMENT DESCRIPTION

3.1 Functional Objectives

The 2 **E**PIC **M**OS **C**amera **S**ystems (**EMCS**), each one placed on the focal plane of one of the XMM telescopes, shall investigate faint X-ray sources. Their purposes are [AD 7]:

a) to detect single X-ray photons in the energy range between 0.1 and 15 keV;

b) to measure the photon arrival position on the telescope focal plane at pixel level;

c) to measure the photon energy using the conversion process in silicon, with an error of 0.1 % of the full energy range;

d) to perform timing studies by measuring the arrival time of the single photons;

e) to reject the cosmic ray traces with 99.9 % efficiency.

To this aim the system is based on solid state detectors of CCD (Charge Coupled Device) type, which reveal the absorbed X-ray photons as electrical signals: these are then converted to digital data and transmitted to ground in telemetry packets.

3.2 Operating Principle

The EMCS consists of a Camera at the focus of one of the three XMM telescopes, containing CCDs, based on Mos technology, passively cooled and thermally controlled to typically –100°C via radiators pointing toward the anti-Sun direction.
In order to cope with a wide range of sky background and source luminosity in the visible/UV band, a filter wheel with six positions (including Open and Close ones), is implemented in the Camera.
A set of radioactive sources allows the calibration of the CCDs in any of the operating modes and with any filter wheel position.
A vacuum door allows the operation of the Camera on the ground, in a vacuum chamber and/or in a controlled atmosphere, and it will protect the CCDs from contamination until the spacecraft is safely in orbit.
The Camera focal plane is composed by 7 CCDs, each with 610 x 602 pixels.
The incoming X-ray photons are detected by CCDs, the electronic chain performs the CCDs readout, the digitalisation of the analogue signals, the thresholding, the discrimination between good X-ray events and background, the organisation in packets of data and transmission, when requested, through the S/C OBDH bus together with the H/K data. Through the OBDH bus the experiment is also able to receive all the commands to be used for the various settings and operations.

4. EXPERIMENT CONFIGURATION

4.1 GENERAL OVERVIEW

Each EMCS (Fig. 4.1-1) is be composed by the following units [AD 7]:

- one EPIC MOS Camera Head (**EMCH**), which provide to interface the incoming X-ray photons and the electronic of the EMCS. It houses the CCD focal plane, which allows to convert X-ray photons into charges, the door and relevant opening mechanism, a filter wheel, whose function is to attenuate optical-UV flux , a radioactive calibration source and heaters for the thermal control of the temperature.

- one EPIC MOS Analogue Electronics (**EMAE**), which operates the EMCH, converts its output data from analogue to digital form and transmits them to the EMCR.The EMAE include also the electronics for the driving of the CDDs (clocks generator), the control of the EMCH thermal conditions and the driver of the filter wheel

- one EPIC MOS Control & Recognition (**EMCR**), which manages the EMAE, performs real time data analysis of CCD pixel data (to reduce the required event transmission rate) and recognises and rejects the non x-ray event. The EMCR provide also for the control of the Annealing Heater and the folter wheel, shared with the EMAE.

- one EPIC MOS Data Handling (**EMDH**), which is the interface between the EMCS and the OBDH bus, performs the scientific data elaboration, handle distribution of the telecommands and telemetry, and control the activation of mechanism, filter wheel and heaters.

- one EPIC MOS Voltage Converter (**EMVC**), which generates secondary power voltages from the spacecraft power supply and provides these power lines to the EMCR, to the EMAE via the EMCR and to the EMCH via EMCR and EMAE;

- one EPIC MOS Internal Harness (**EMIH**)

- one EPIC MOS Proton Shield (**EMPS**), whose main function is to protect the camera head from Minimum Ionising Particles and act to provide stray-light baffling.

The block diagram (Fig.4.1-2) shows the configuration of the EMCS.

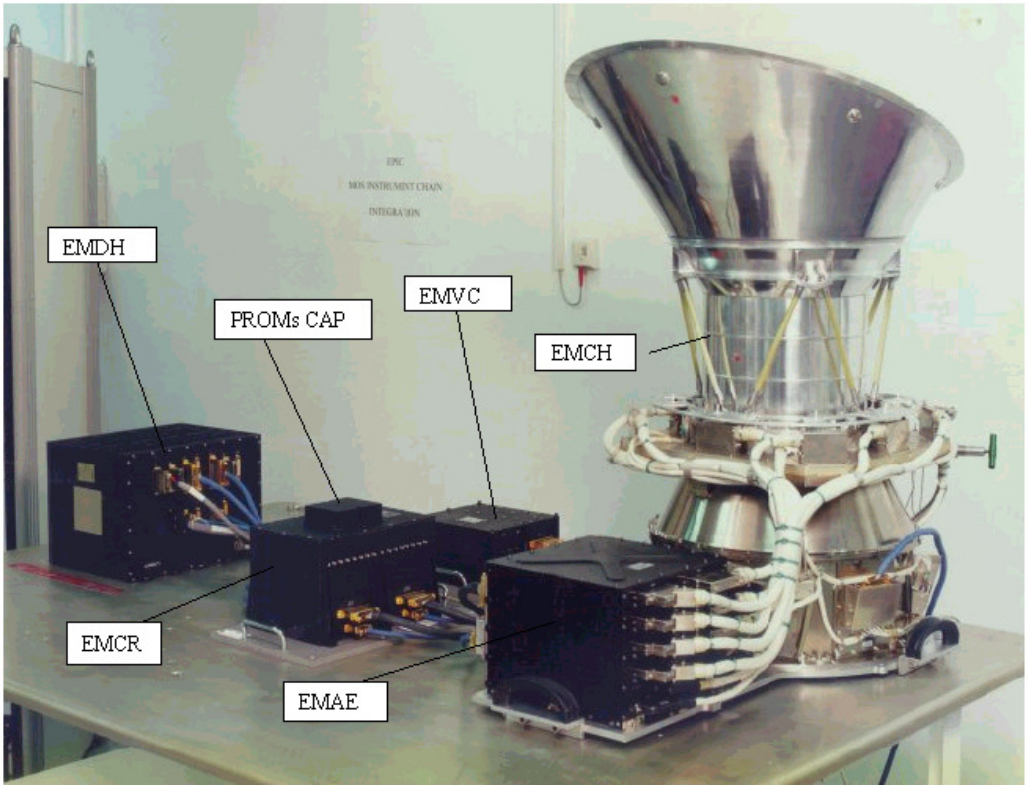


Figure 4.1-1: EPIC MOS Camera System

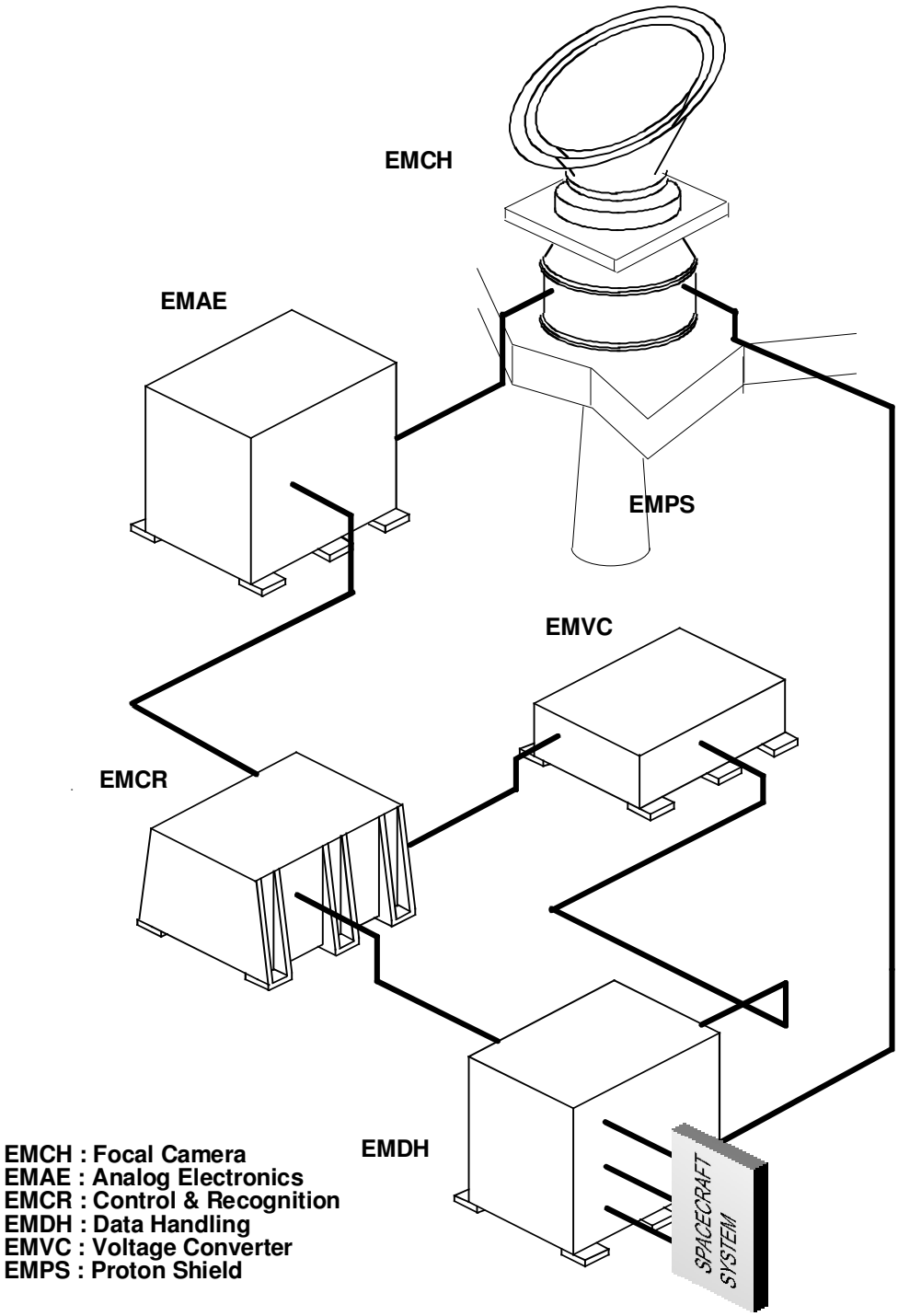


Figure 4.1-2: EMCS Block Diagram

4.2 EPIC MOS CAMERA HEAD (EMCH) (AD 7 §9.3.2.)

The EMCH contains the CCDs and the minimum electronics which must be located directly near them. The EMCS detector assembly is an array of 7 identical CCDs placed on the telescope focal plane (Fig.4.2-3): the centre of the focal plane coincide with the centre of the central CCD (AD 7, §3.1):

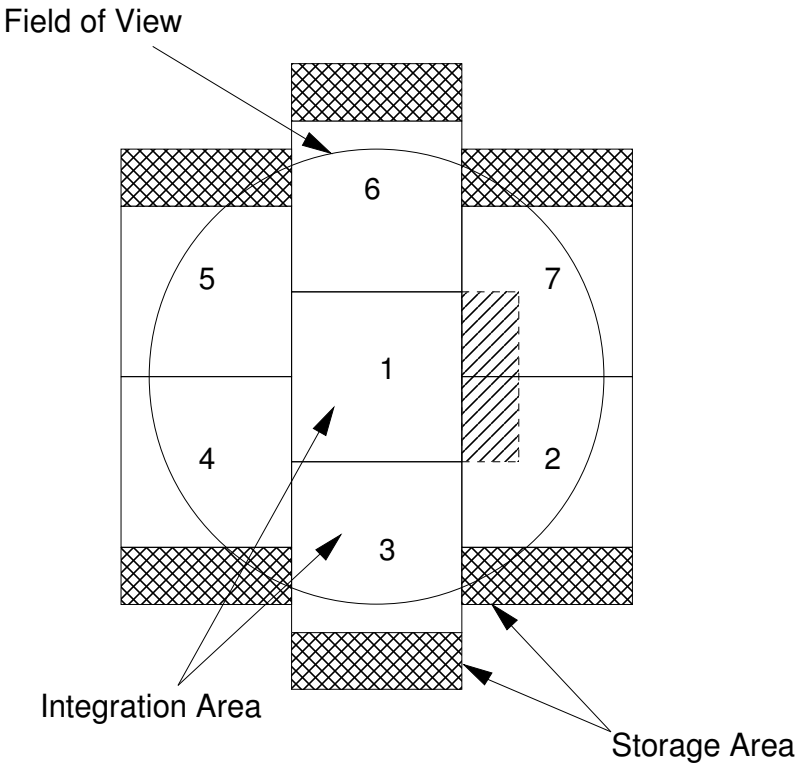


Figure 4.2-1: Layout of the focal plane, as seen from Radiator side.

Each CCD is made of two areas (Fig.4.2-2):

1) The integration area is of 600 x 600 square pixels 40 μm in size, plus 2 pixels per column and 10 pixels per row, for a total configuration of 610 x 602 pixels: the pixels exceeding the 600 are used as over-scanning features. In this area the image of the detected source is formed.
2) The storage area, having the same number of pixels but smaller pixel size (40 x 12 μm^2).

For each CCD there are two output read-out nodes and two dedicated output channels: the CCDs are interfaced to the EMAE unit, which provide for the Analogue to Digital Conversion of the incoming pixel signals, via 14 preamplifiers, one for each output reading node of each CCD.

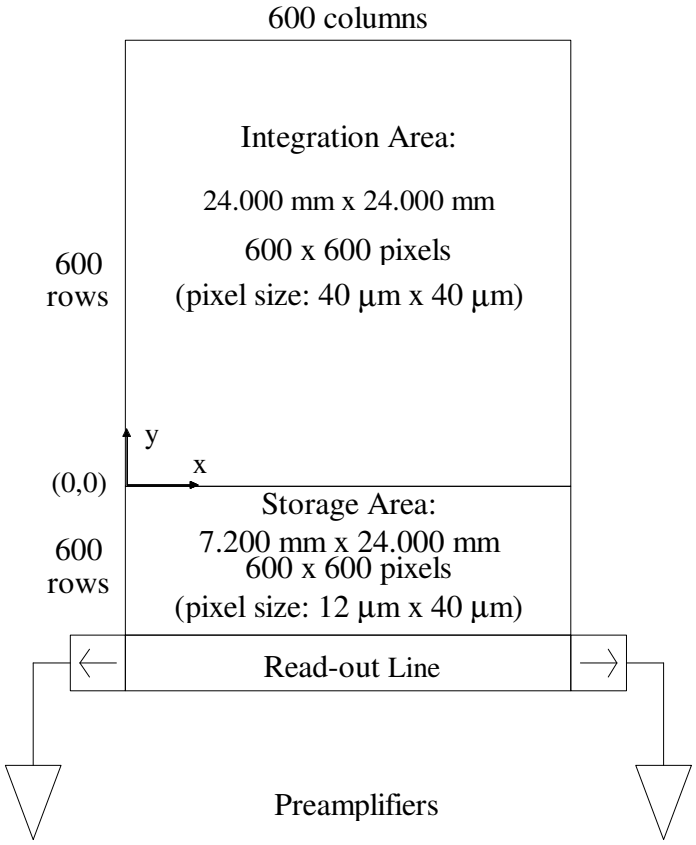


Fig. 4.2-2: Structure of a single CCD

The EMCH includes a filter_wheel mechanism above it (Fig.4.2-4), in order to protect the detector against dangerous particles and to reject incoming optical flux. The filter wheel is driven by a stepper motor, controlled by the EMCR and driven by the EMCR, having main and redundant windings driven by redundant drive electronics giving 1600 steps per revolution. It has six positions: closed, open, filter a (thin), filter b (medium), filter c (medium), filter d (thick). The filter wheel position is monitored by main and redundant Hall effect sensors giving 6 “stops”. In addition there are three Hall effect sensors giving a unique bit pattern for each of the 6 filter positions.

The EMCH has the capability of in-flight calibration. To this aim, the camera head includes a fixed calibration source which directly illuminates the CCDs through one of the 6 holes of the filter wheel (each nearby one of the 6 filter wheel standard positions) (AD 7, §3.2.5).

The EMCH is provided of protective mechanism (Fig.4.2-5) to avoid contamination and damage of the CCDs during on ground and pre-orbit activity. When it is subject to the ambient pressure, the CCDs is under low pressure conditions (< 10 mbar) (RD 4, §12). It has a venting_valve (Fig.4.2-6), a protective door and a door mechanism containing the door bellows (Fig.4.2-7).

One bellow pressure sensor is provided for each camera, in order to monitor the pressure of the door bellows. A diodes oring the bellows power supply is provided to guarantee safety operation during all ground phases. The protective door is opened and closed, via telecommand, by High Output Paraffin (HOP) actuators, which are directly driven by the EMDH (RD 5, §1.8).

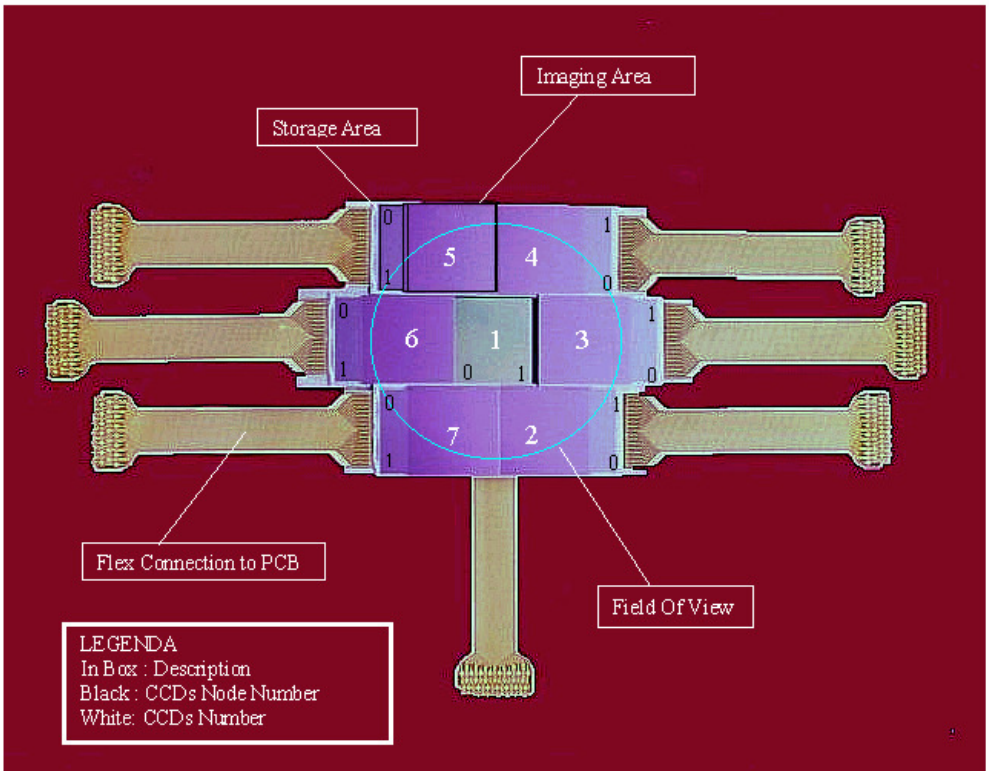
Two vacuum sensors are provided for each camera, in order to monitor the pressure of the camera itself: the first sensor is powered via TC and is monitored on TM; the second sensor is powered and monitored via EGSE.

The EMCH contains a cooling system (i.e. a set of thermal radiators) to cool the CCDs at the requested operating temperature. Moreover it has the following heaters:

1) Annealing Heater;
2) CCD Thermal Control Heaters (one nominal and one redundant);
3) Secondary Shroud Heater;
4) Stand-by Heater (controlled by the S/C).

Finally, it has thermistors monitored by the EMAE and one thermistor monitored by the S/C.

Figure 4.2-3: EPIC MOS Focal Plane



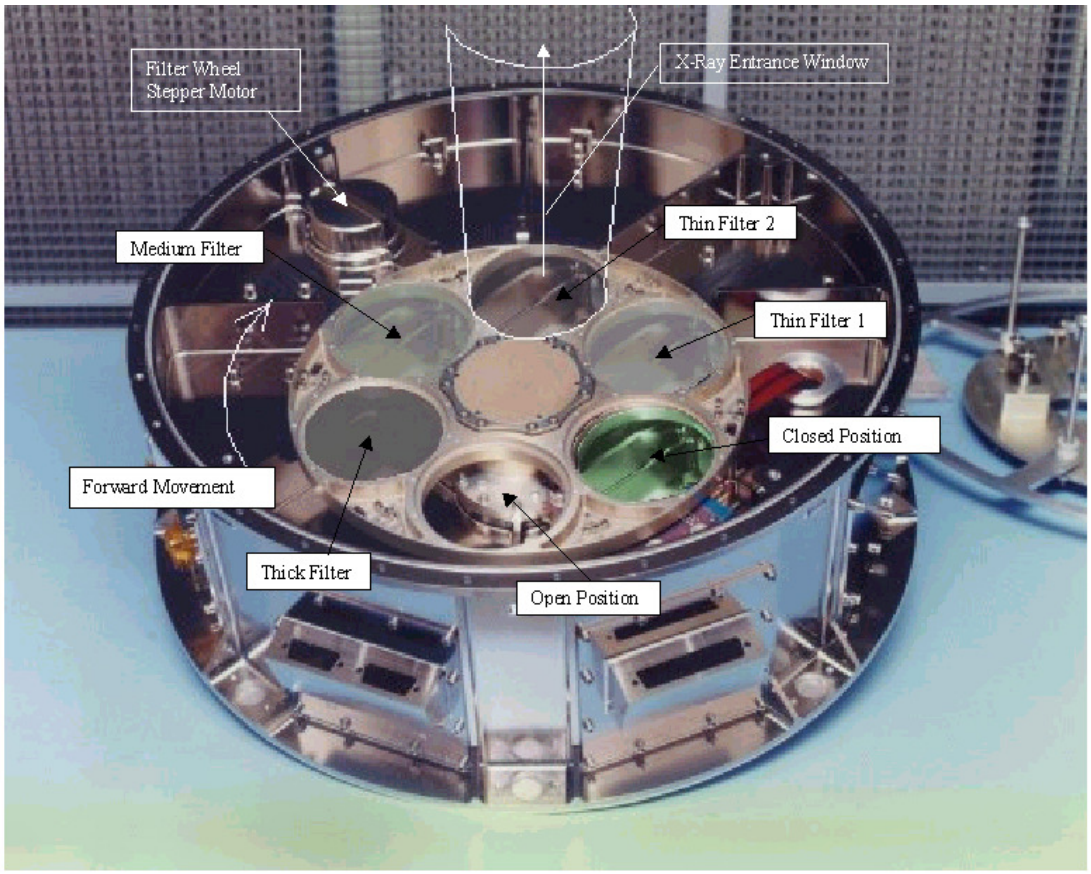


Figure 4.2-4: The Filter Wheel mechanism

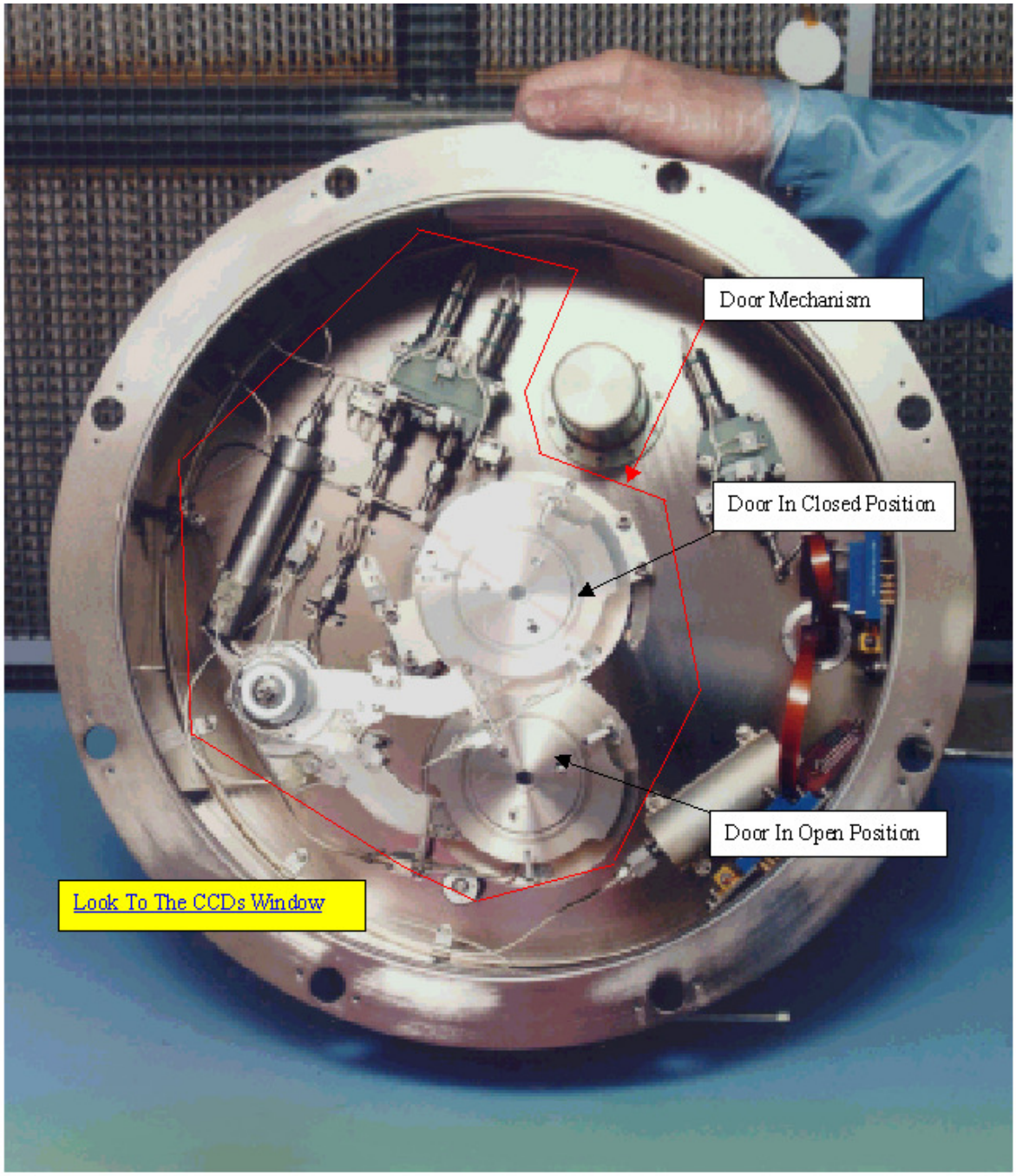


Figure 4.2-5: The Door protective mechanism

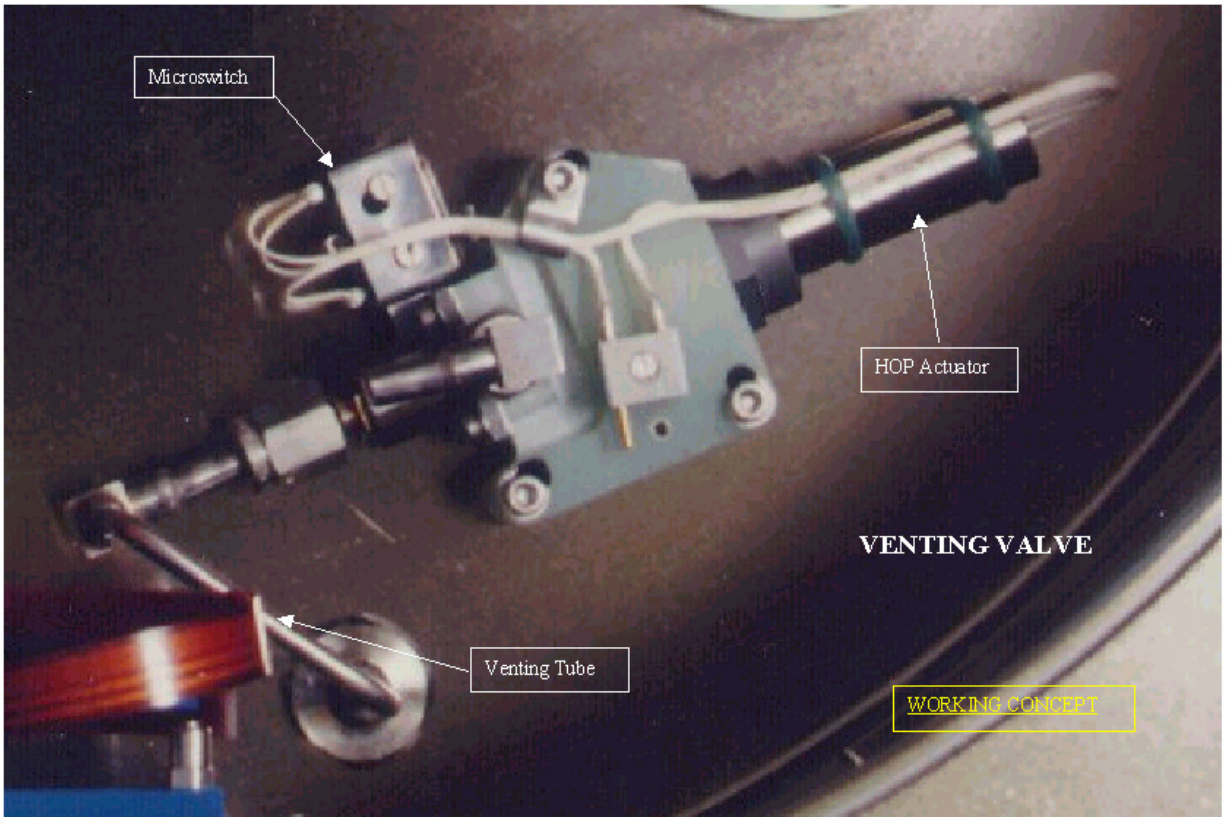


Figure 4.2-6: The Venting Valve mechanism

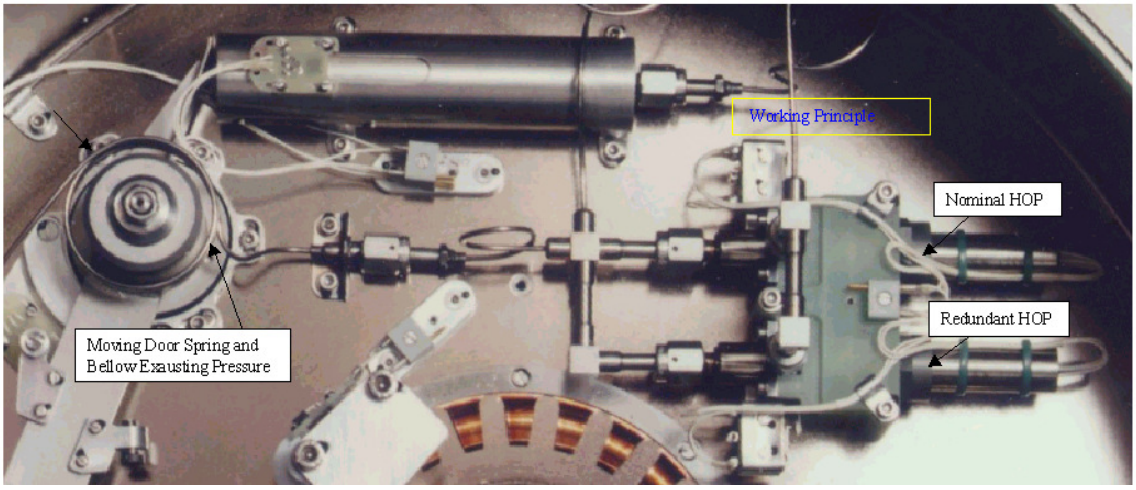


Figure 4.2-7: The Door HOP mechanism

4.3 EPIC MOS ANALOGUE ELECTRONICS (EMAE) (AD 7, §9.3.3.)

Each EMAE is constituted by (Fig.4.3-1):

- 8 Analogue to Digital Conversion chains, each composed by a 3-input Analogue Multiplexers and an Analogue to Digital Converter
- 5 Sequencers
- 7 bias generators (one for each CCD)
- 7 clock driver devices (one for each CCD)
- 4 CCD Simulators
- a nominal and a redundant EMCH Thermal Control Device
- a nominal and a redundant Filter Wheel Driver Device

Each of the 7 CCDs has its own bias generator and clock driver. The central CCD and the three pairs of the outer CCDs are each associated to a sequencer, a CCD simulator and 2 analogue chains. A redunded sequencer is dedicated to drive the filter wheel stepper motor. Each sequencer can be loaded with sequences furnished by the EMCR.

The central CCD and each pair of the outer CCDs are read out to a pair of processing chains, giving 8 possibly active channels. Each sequencer provides CCD clocks (via the clock drivers) and timing signals for the analogue processing and serial readout. Each CCD is linked by fast serial interface to its dedicated input to the EMCR. Thus there are 8 analogue chains in total and 4 associated sequencers.

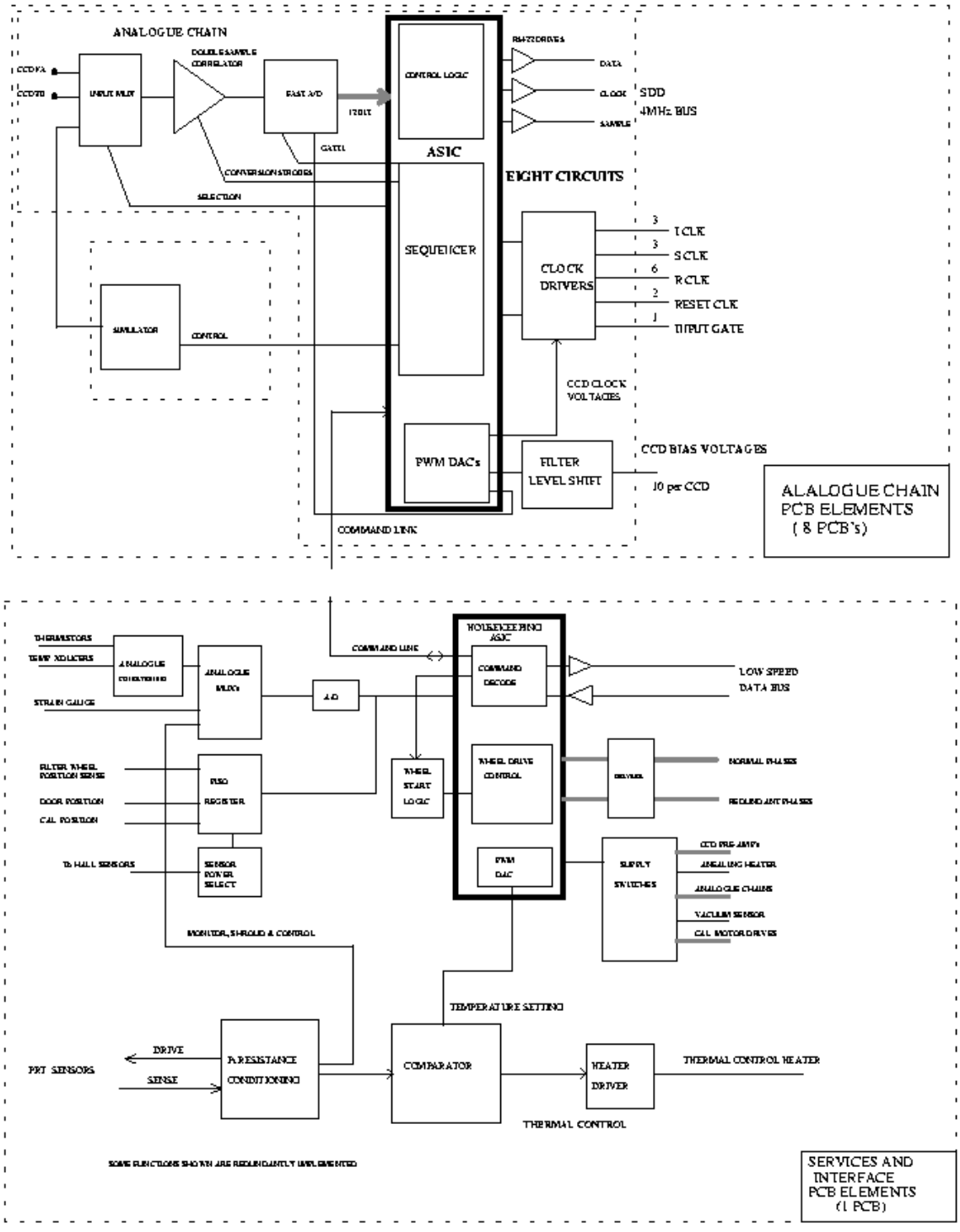


Figure 4.3-1: EMAE Block Diagram

4.3.1 CHAIN CONFIGURATION

The CCD chain is the path defined by the node of the CCD up to the High Bit Rate Interface of the EMDH.
Due to the complex structure of the telecommands involved and to a possible re-configuration of the chain, in the following figures is shown a relation between numbering of CCD, premplifiers, analog channels, sequencer and Event Detection Unit (See relevant paragraph), involved in the signals handling.

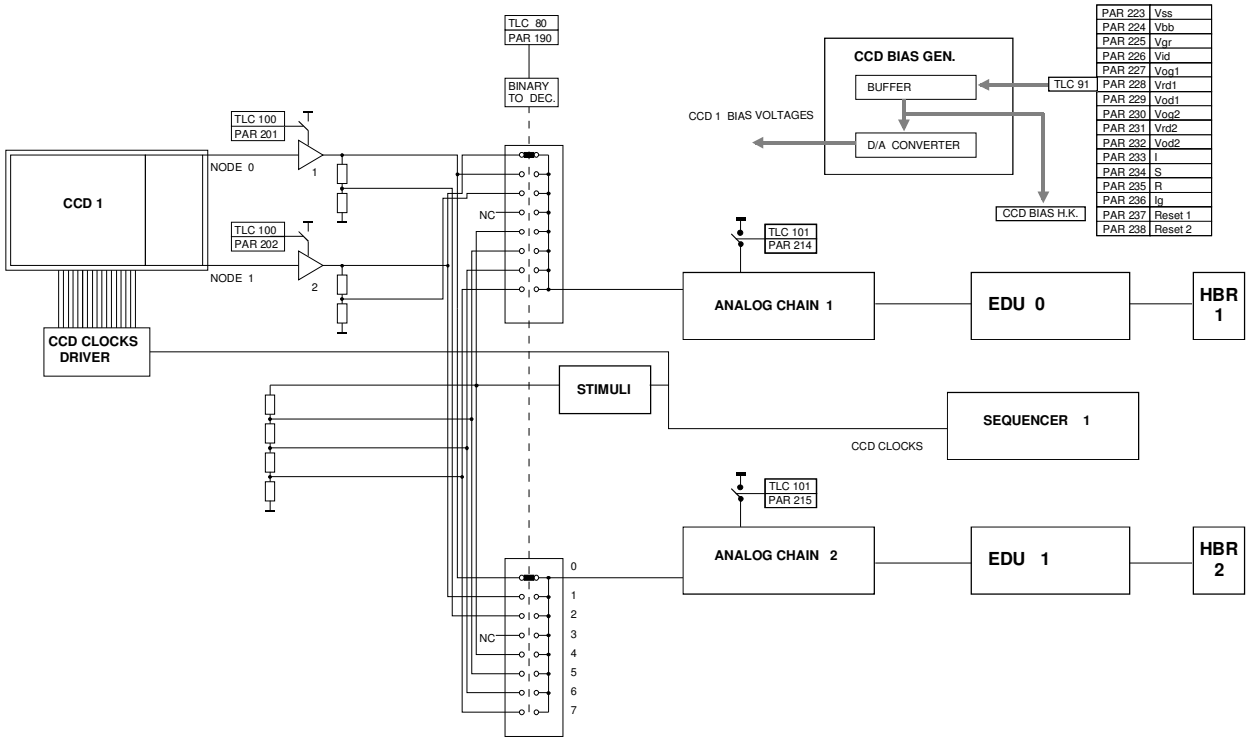


Figure 4.3.1-1: Analogue Chain configuration for the central CCD

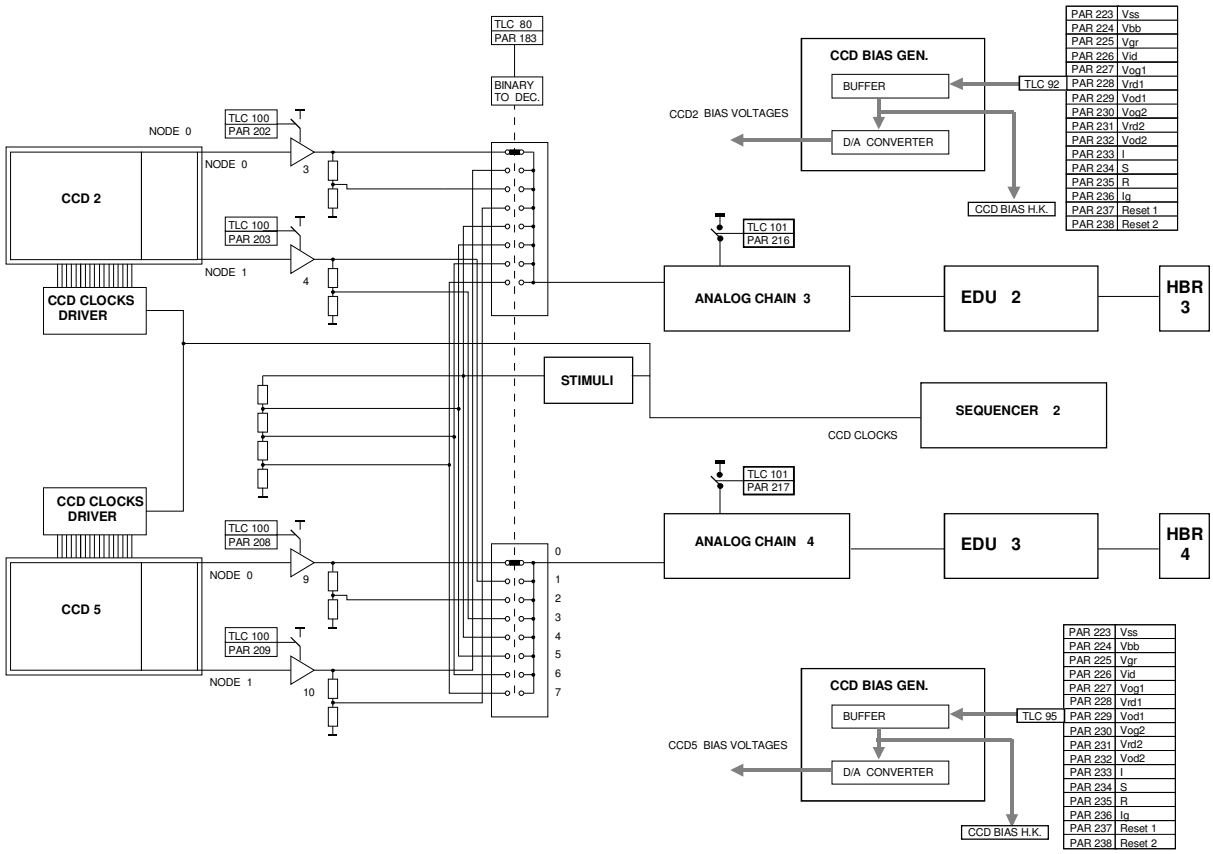


Figure 4.3.1-2: Analogue Chain configuration for the peripheral CCDs

4.4 EPIC MOS CONTROL & RECOGNITION (EMCR)

The EMCR architecture is based on a microcomputer in charge of the control of the operation (commands and housekeeping handling) of the unit (CTR) and hardwired computers (EDU) in charge of the scientific data analysis. A set of latching relays is in charge of the secondary power supplies switching (generated by the nominal and redundant converter of the EMVC unit).

The major components of the EMCR are :

- a microprocessor
- RAM devices
- PROM devices
- DMA, IT and USART controllers
- analog multiplexer and ADC (for H/K acquisition)
- an applicative software

for the microcomputer

- a gate array
- RAM and FIFO devices

for the hardwired computer

4.4.1 Top level architecture

The below Block Diagram shows the overall architecture of the EMCR unit.

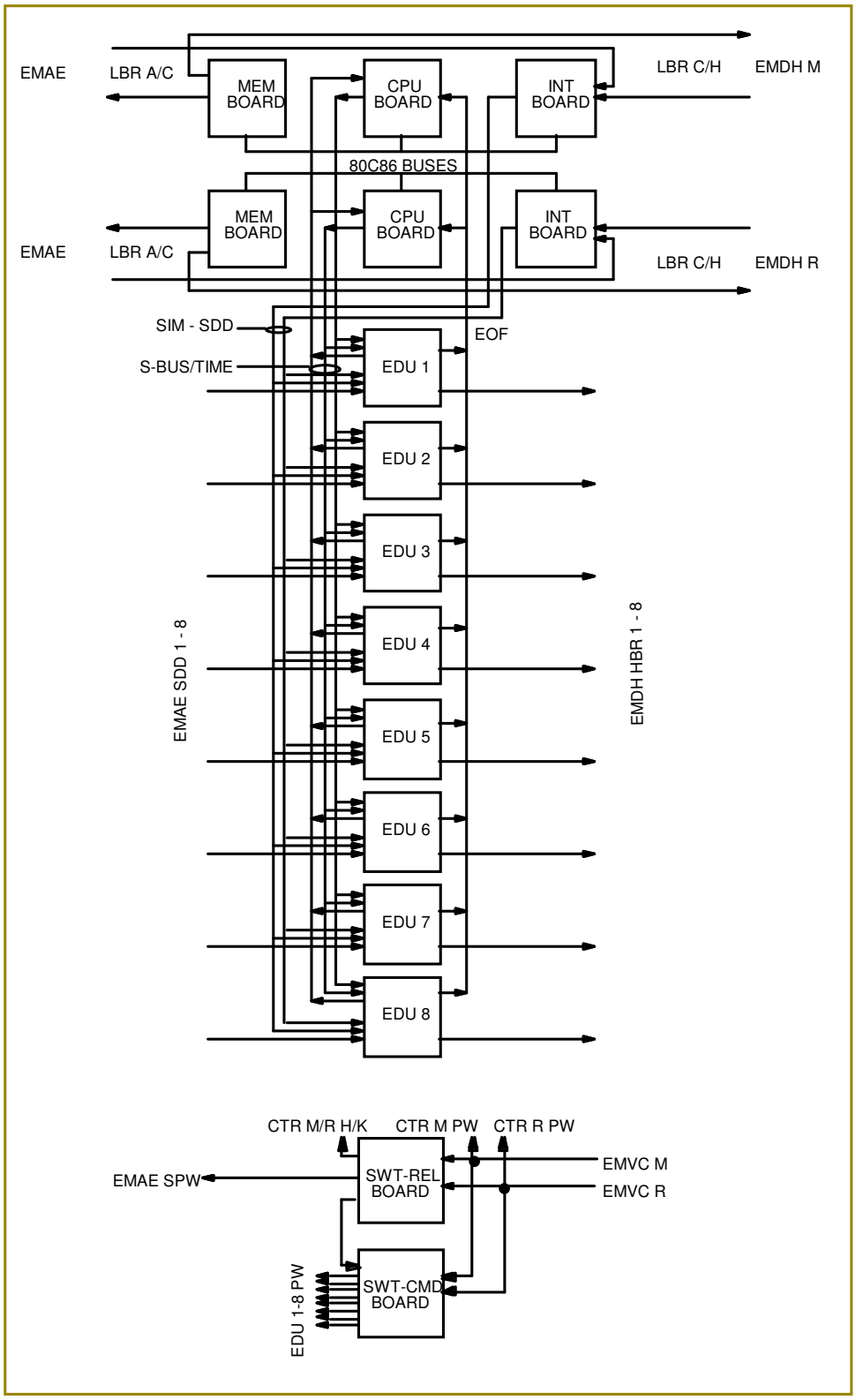


Figure 4.4.1-1: EMCR Block Diagram

4.4.2 Controller design

The controller hardware takes place on three single europ boards: memory (mem), central processing unit (cpu) and interface (int).

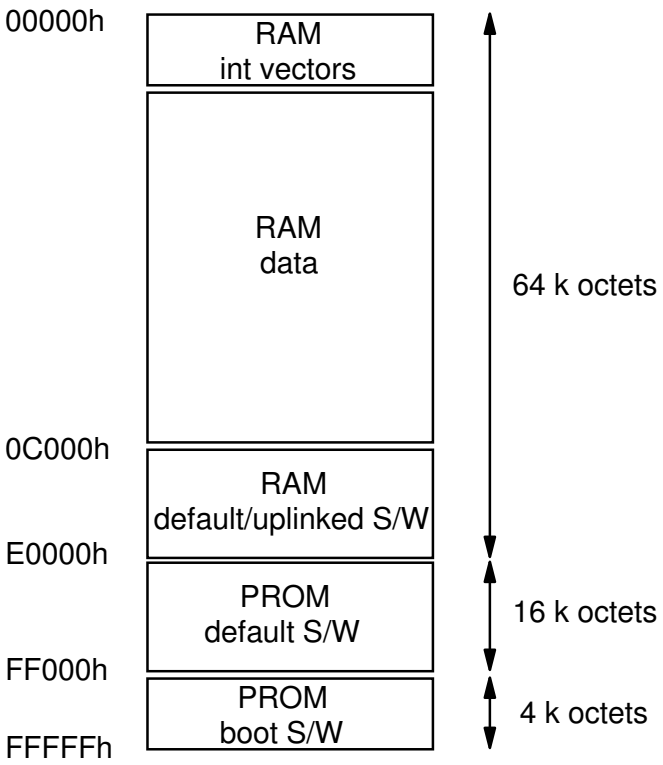
4.4.2.1 Memory Board

The Block Diagram of the EMCR Memory Board is shown in Fig.4.4.2.1-1.

This board contents the RAM and PROM memories required to store and to execute the controller software :
• a boot PROM of 4 kbytes (for initialisation and LBR C/H protocol)
• a program PROM of 16 kbytes (for default S/W)
• a program and data RAM of 64 kbytes (for program execution after transfer from program PROM or uplinking)

It also contents the drivers and latches for interfacing with the other controller boards.

The following table gives the memory mapping of the controller.



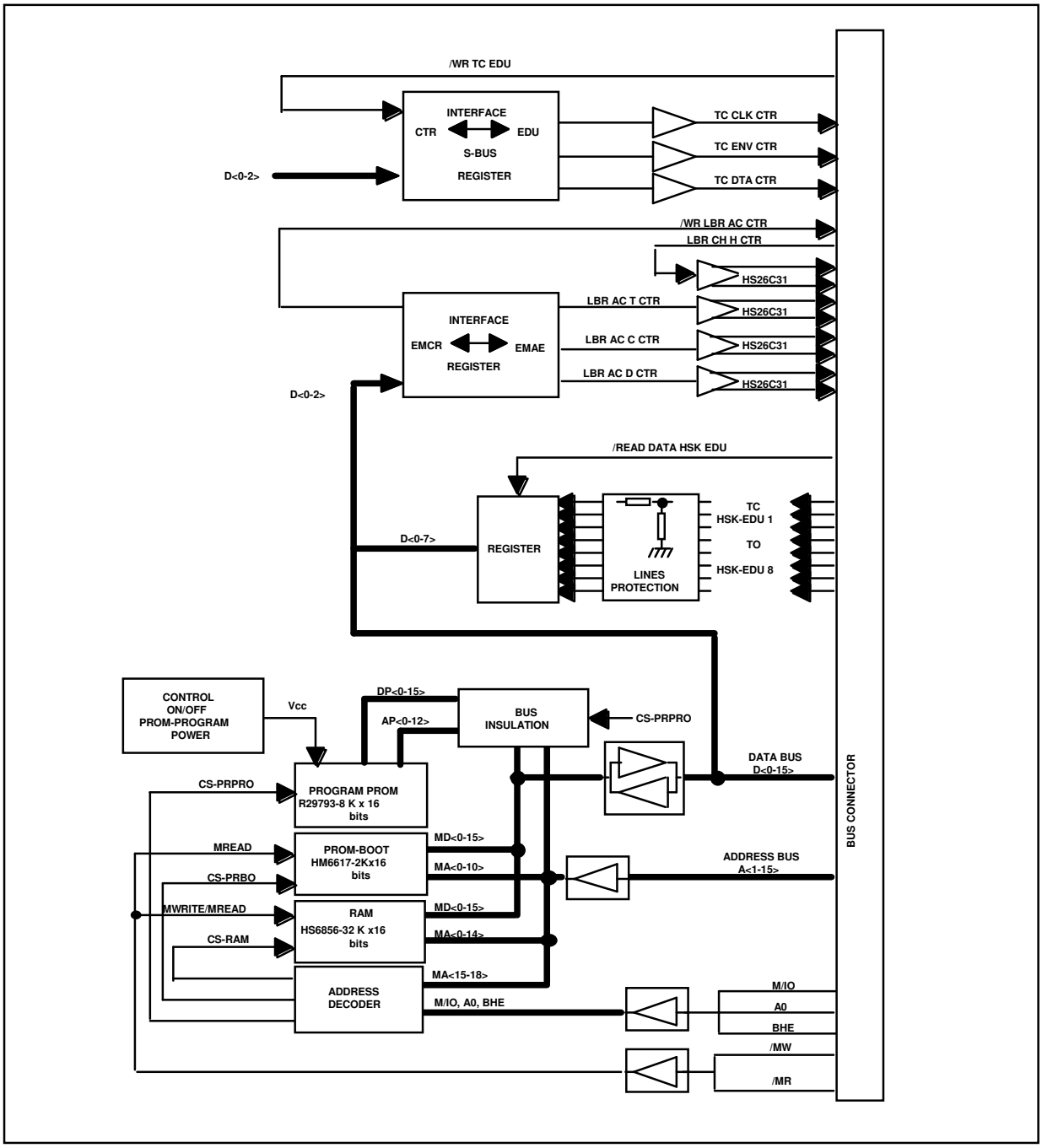


Figure 4.4.2.1-1: Block Diagram of the EMCR Memory Board

4.4.2.2 CPU Board

The Block Diagram of the CPU Board is shown in Fig.4.4.2.2-1

This board contents the microprocessor and its associated controllers :

• a 80C86 microprocessor at 4 MHz running the controller S/W
• a 82C85 for clock generation (12 MHz crystal)
• two 82C59 for interrupts control : one is used for S/W synchronisation with the 8 EDU (by using the End Of Frame signal), while the second is used for S/W synchronisation with the internal time base -frame tic- (which defines the time resolution of the commands sent to the EMAE sequencers).
• a 82C37 (DMA) for SDD simulation and EDU in-flight test

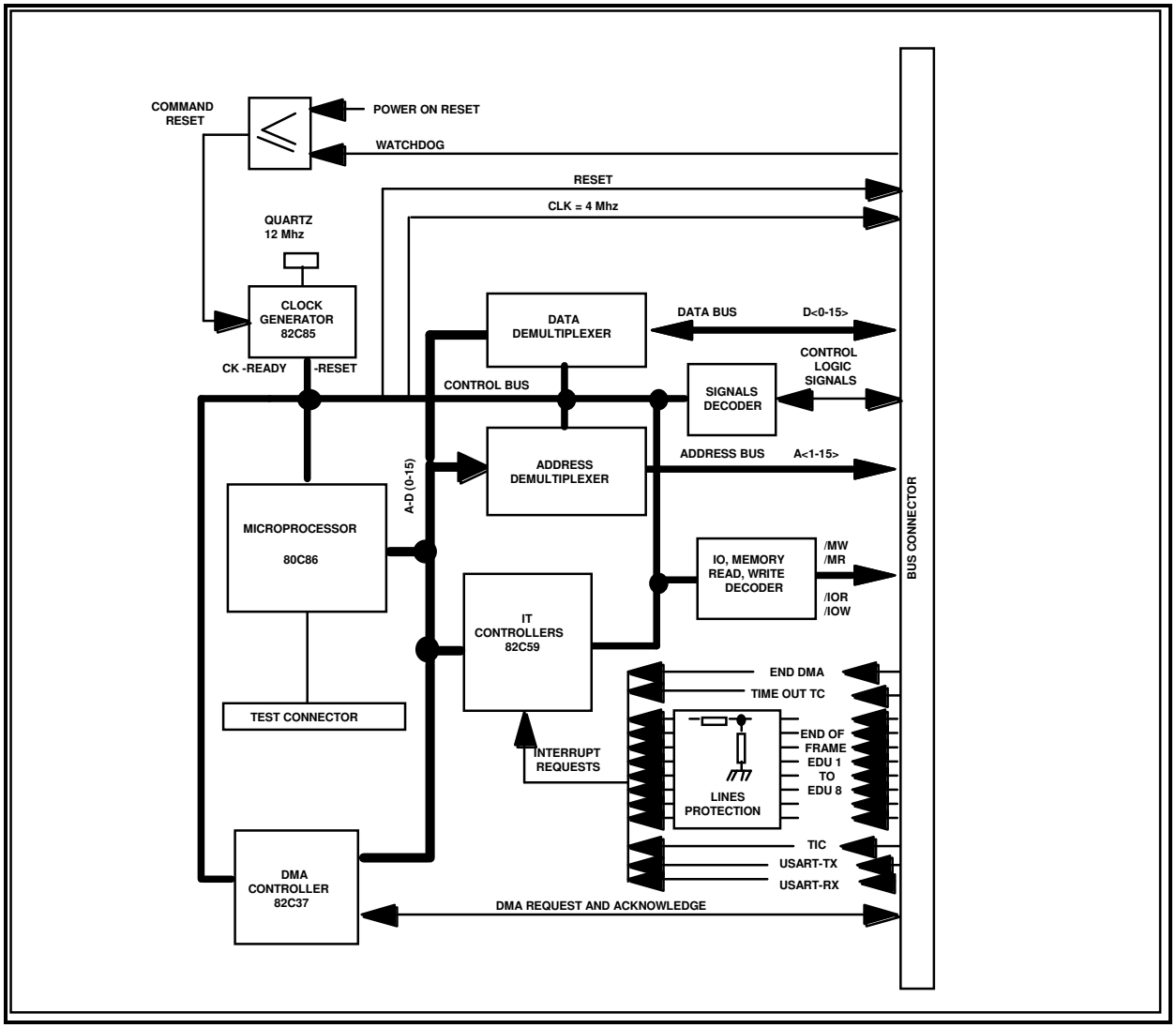


Figure 4.4.2.2-1: Block Diagram of the EMCR CPU Board

4.4.2.3 Interface Board

The Block Diagram of the Interface Board is shown in Fig.4.4.2.3-1

This board contents the logic required to interface with the EMDH LBR C/H, to generate internal time bases, to simulate the SDD protocol and to convert the EMCR/EMVC H/K from analog to digital:

- a 82C51 (USART) for LBR C/H electrical protocol handling
- two 82C54 for time bases generation : frame tic, LBR C/H time-out and baud rate
- a binary counter for watchdog activation
- an analog switch and 8-bit ADC for H/K acquisition and conversion.

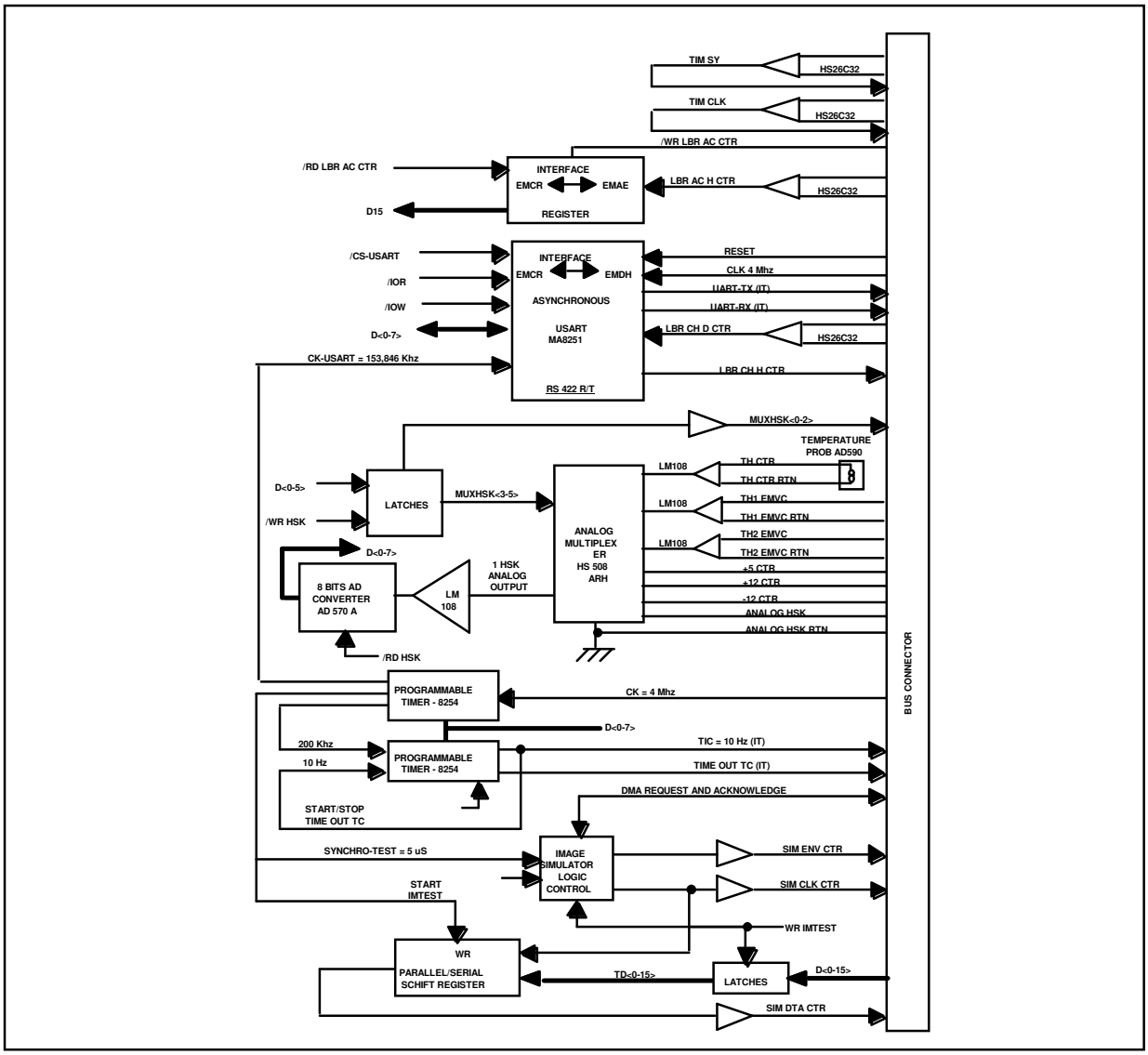


Figure 4.4.2.3-1: Block Diagram of the EMCR Interface Board

4.4.3 Event Detection Unit design

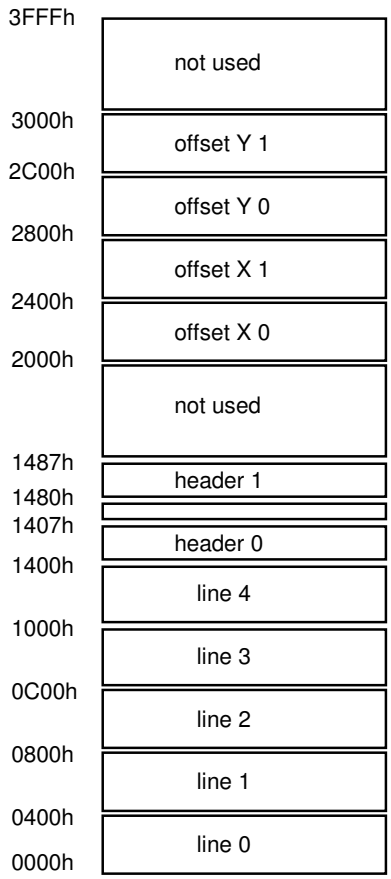
4.4.3.1 EDU Board

The EDU hardware takes place in one single europ board. This board contents the gate array and the memory devices used for buffering data and parameters :

- a 16-kgates ASIC
- a RAM of 32 kbytes for scientific data buffering and offset tables storage
- a FIFO of 1k x 18 bits for output data rate smoothing

The Block Diagram shows the global architecture of the EDU board (Fig.4.4.3.1-1).

The following table shows the memory mapping of an EDU.



Notes :

- line 0 to line 4 are used by the EDU to store the last 5 lines and allows the 5x5 matrix analysis.
- Two sets of offset X/Y and header buffers are inplemented to enable the alternate analysis of two CCD (in degraded configuration of the EPIC camera) with no dead time between successive frames.
- The depth of the buffers is sized to handle CCD of up to 1024x1024 pixels [i].

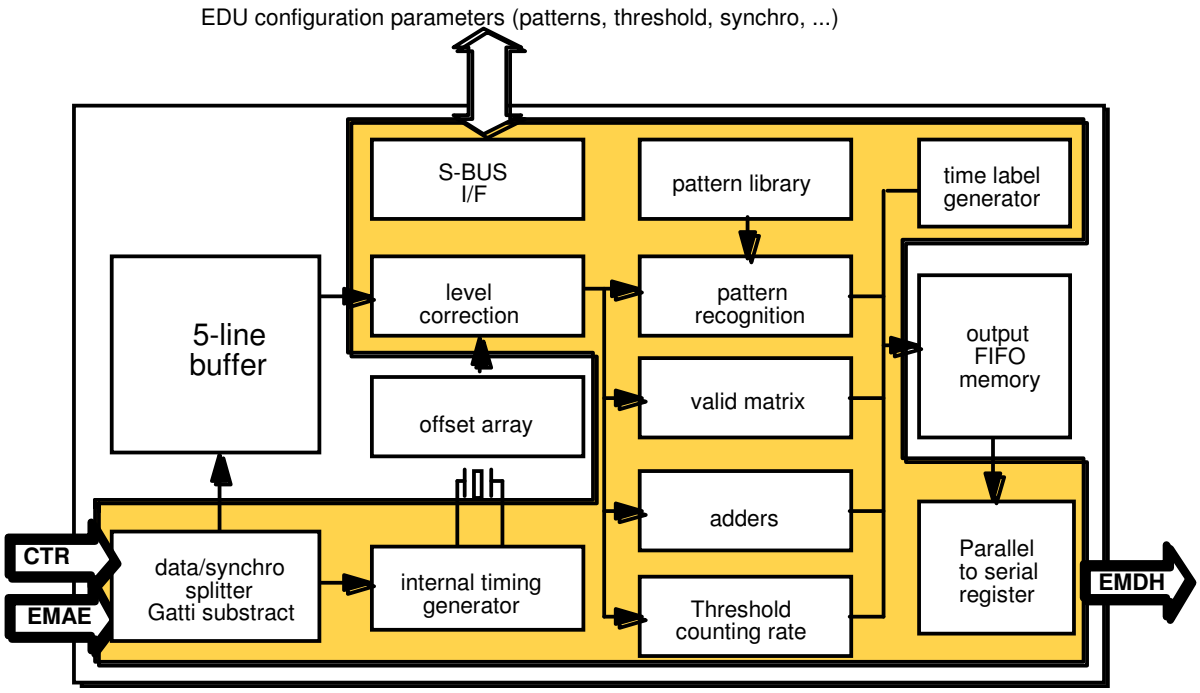


Figure 4.4.3.1-1: Block Diagram of the EDU Board

4.4.3.2 List of EDU commands

This commands are generated by the active controller via a bidirectionnal serial interface (S-BUS). They enable the EDU configuration (mode, node, load/run status, …) and parameters loadings (offsets, threshold, patterns library, …).
The controller will check the proper configuration of the EDU by two ways :
• while in write mode the EDU echoed the received word (command or data) via S-BUS H/K line.
• the I/F can also be operated in read mode and allows the read back of all parameters.

Here below is the list of this commands :

Name	Code	Function	Format
RAZ-C	00	Reset Internal Pointers/Register	1 cmd
C-NOD	01	Set the CCD node number	1 cmd + 1 arg
C-PTN	03	Load/Read the patterns table	1 cmd + 100 arg
C-HDR	04	Load/Read the header	1 cmd + 5 arg
C-OFFX	05	Load/Read the X offset table	1 cmd + up to 1024 arg
C-OFFY	06	Load/Read the X offset table	1 cmd + up to 1024 arg
C-GAT	07	Set the Gatti value	1 cmd + 1 arg
C-MOD	08	Set the SDPM	1 cmd + 1 arg
C-EOF	09	Force the EDU to generate a trailer format	1 cmd

C-STAT	10	Read EDU status : Threshold value + SDPM + FIFO status	1 cmd

Comments : the EDU gate array will have two SDD interfaces : one is for interfacing with the EMAE unit while the second is connected to the SDD simulator of the controller for in flight tests purpose. The active SDD interface is set by a S-BUS command.

4.4.4 Auto switch module Design

The autoswitch module hardware takes place on two single europ boards named SWT_CMD and SWT_REL.

4.4.4.1 SWT_CMD Board

This board contents the analog electronics required to command the latching relais when the nominal or redundant converters of the EMVC are powered. The design is based on comparator with hysteresis and time constant to insure a minimal winding command duration. It also contents current limiters (one per EDU) to avoid failure propagation in a case of overcurrent.
The maximum current is set to twice the maximum current supply of an EDU. See annexe 2 for measurement results on Q.M. limiters.

4.4.4.2 SWT_REL Board

The block diagram (Fig.4.4.4.2-1) shows the architecture of the switching board.
This board contents a set of latching relays for EMAE power supplies switching and a differential analog multiplexer for EMAE voltages measurement. The analog output is then routed to the controller ADC.

Note : in the previous block diagram some voltages have been changed since its drawing. The actual values are: EMCR SPW

+5 N & +5 R	swap to	+5.2 N & +5.2 R
+/-12 N & +/-12 R	swap to	+/-13 N & +/-13 R
EMAE SPW +5	swap to	+6
+/-12	swap to	+/-13

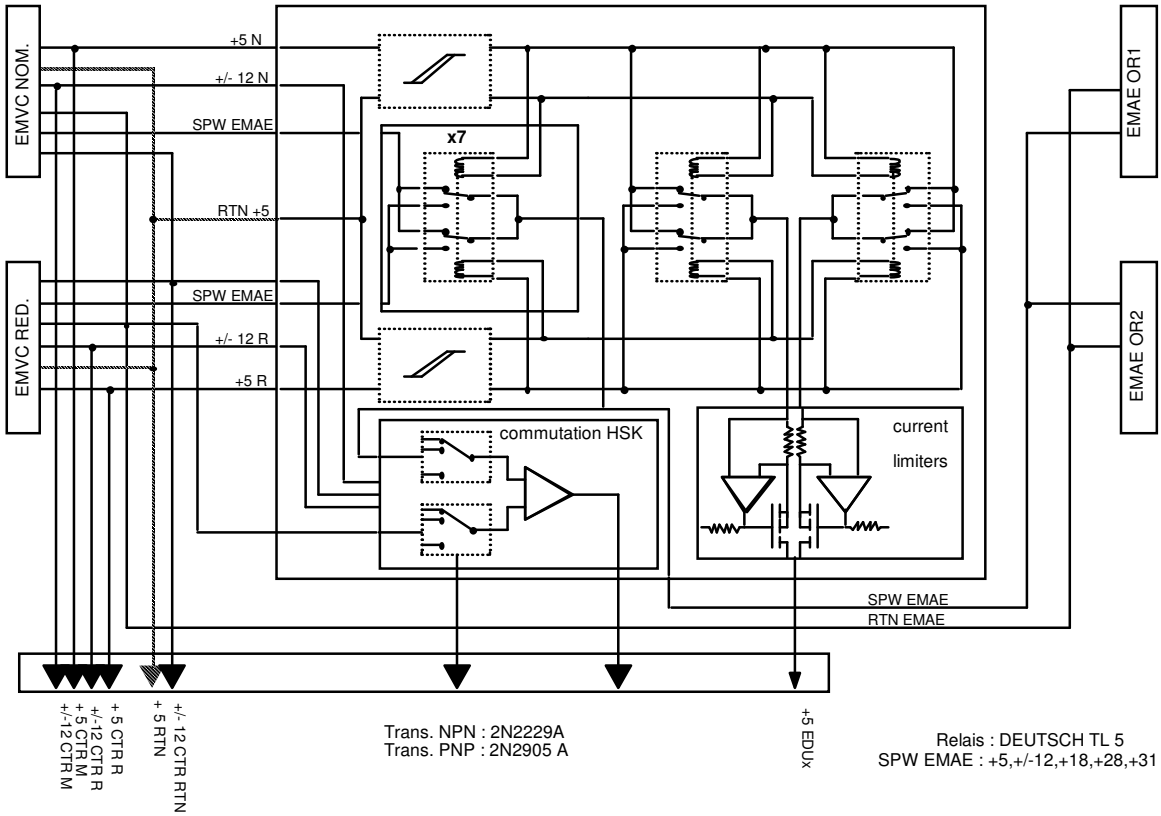


Figure 4.4.4.2-1: Block Diagram of the Switching Board

4.5 EPIC MOS DATA HANDLING (EMDH)

The EMDH contains 2 electrical independent sets (one nominal and one redundant) of the following H/W components:

PROM BOARD
MASTER µPROCESSOR BOARD
SCIENTIFIC µPROCESSOR BOARD
HBR I/F BOARD
RBI I/F BOARD
GENERAL
MISCELLANEOUS BOARD
POWER SWITCHES BOARD
DC/DC CONVERTER BOARD
EMI FILTER
FRB MOTHERBOARD

Note: The following description is a summary of the performances. In case of need for detailed information, click on the relevant hyperlink.

PROM_board

It provides PROM areas, which are dedicated to store permanently the EMDH S/W code.

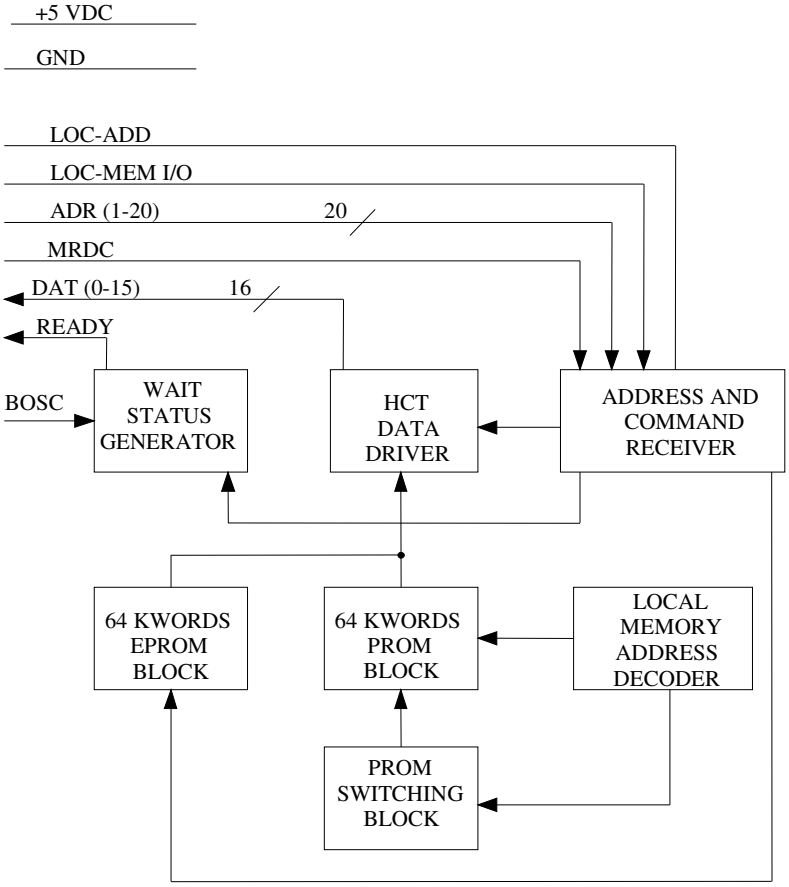


Figure 4.5-1: PROM Board Block Diagram

Master_Microprocessor_Board

This board co-ordinates the activities of the whole unit and controls all H/W devices connected to the System Bus (SBUS90). It's main role is to provide Data Handling functions (e.g. TLC/TLM management, unit/system operating modes management etc.)
This board provides:

interface to LBR channel in order to allow data exchanging with the EMCR
interface to the TEST channel in order to exchange data and commands with the Test Equipment during on-ground testing.
boot-strap PROM for cold restart.
RAM for storage of S/W Code and Constants
RAM for S/W data
RAM for scientific data storage
Timer function for TIM-RST generation function

This board is interfaced to system bus and it has capability to act as unit bus master.

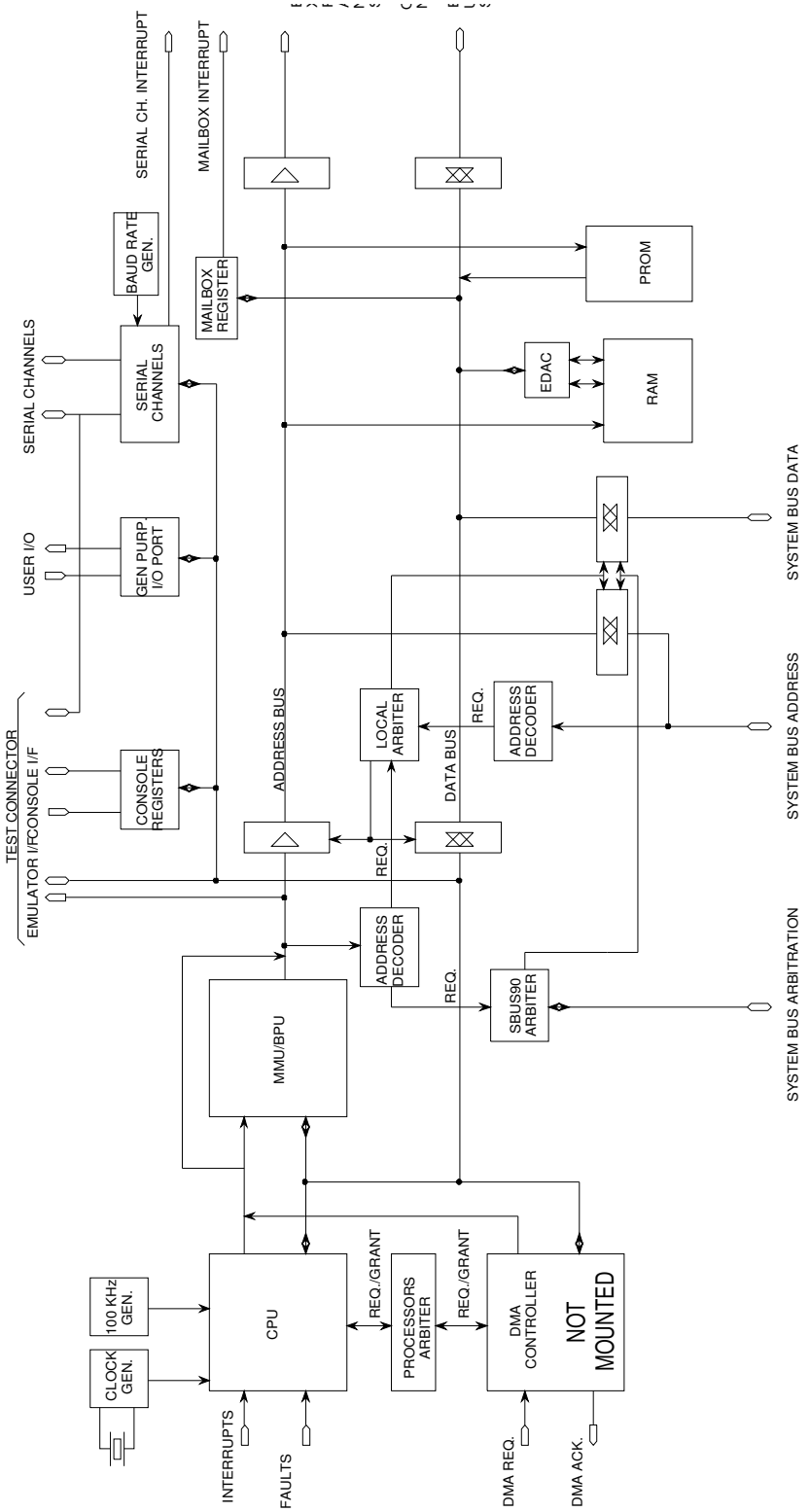


Figure 4.5-2: Microprocessor Board Block Diagram

Scientific Microprocessor_board
This board provides:

interface to the TEST channel in order to exchange data and commands with the Test Equipment during on-ground testing.
boot-strap PROM for cold restart.
RAM for storage of S/W Code and Constants
RAM for S/W data
RAM for scientific data storage
interface to HBR board via local bus.

This board is interfaced to system bus and it has capability to act as unit bus master.

HBR I/F_board 1
This board is aimed to receive the scientific data coming from the EMCR unit.

This board provides:

interface to 8 HBR serial channel
8 KWord FIFO per each channel

This board is not connected to system bus. It is connected to the scientific processor via a local bus.

This board provides an interface to 4 HBR channels of the EMCR (HBR1, HBR3, HBR5 and HBR7).

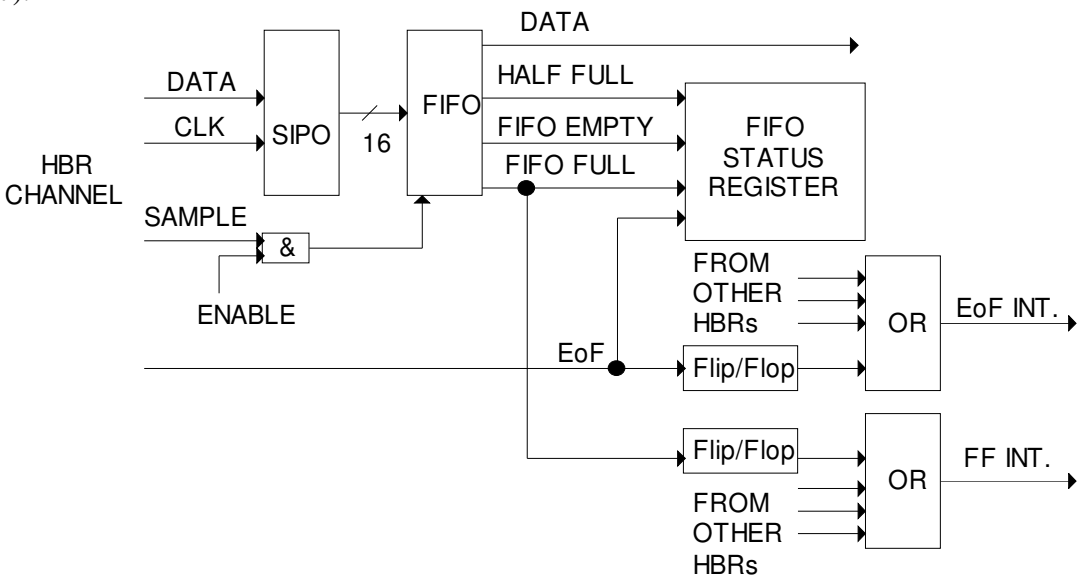


Figure 4.5-3: HBR – Receiver & Buffering Stages

HBR I/F board 2
As for HBR I/F board 1 but for HBR2, HBR4, HBR6 and HBR8.

RBI_I/F_ & Time Management board

This board mainly aims to interface the EMDH unit to XMM OBDH bus.

This board provides:

- RBI protocol management (including low level RBI commands)
- TLC/TLM data exchange between the EMDH and the OBDH
- EMDH OBT management
- Generation and/or distribution of synchronisation signals for EMCR (TIM_CLK and TIM_RST)

This board is interfaced to system bus and it has capability to act as unit bus master.

In case of contemporary access to system bus by the bus masters, this board has got priority.

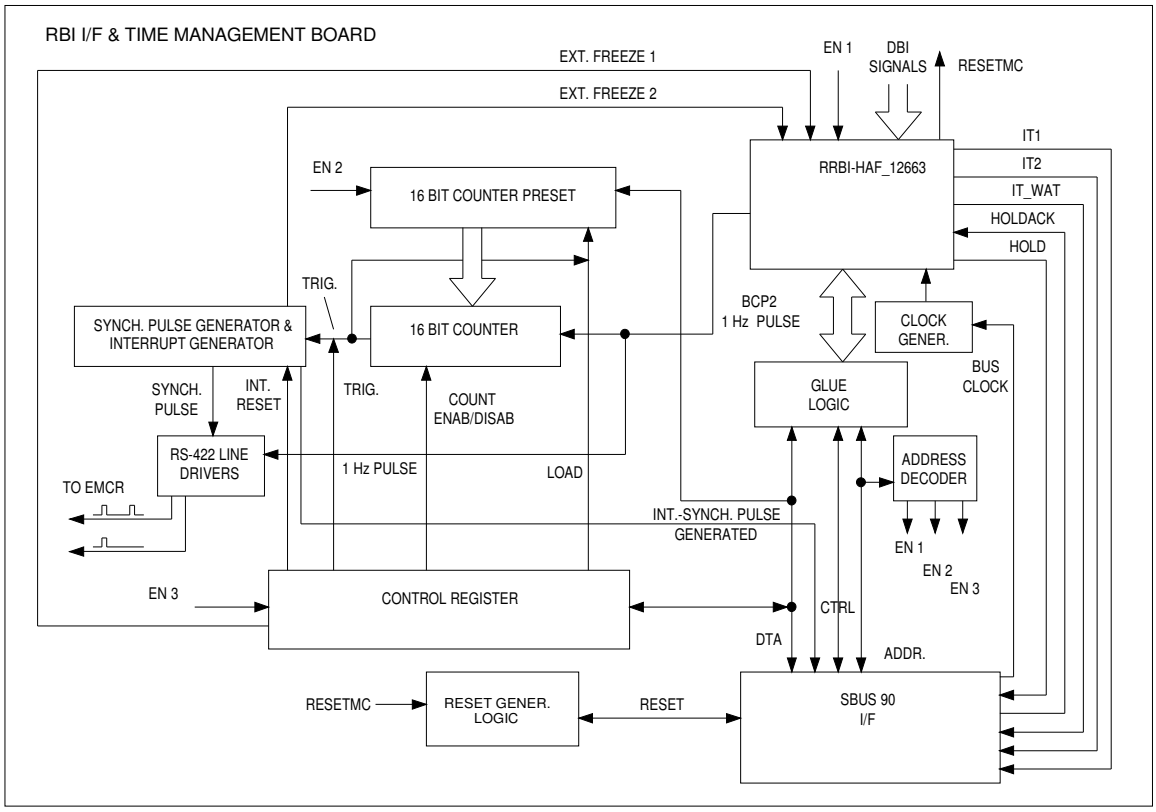


Figure 4.5-4: RBI I/F & Time Management Board Block Diagram

Miscellaneous Device board

This board provides several miscellaneous functions.

This board provides:

- interface between Master processor board and Switches board
- generation and de-coupling of Power synch. Signals
- routing of S/C Stand-By Heater Power
- signal conditioning, acquisition and A/D conversion of EMDH internal parameters
- generation of DBU power supply

This board is interfaced to system bus.

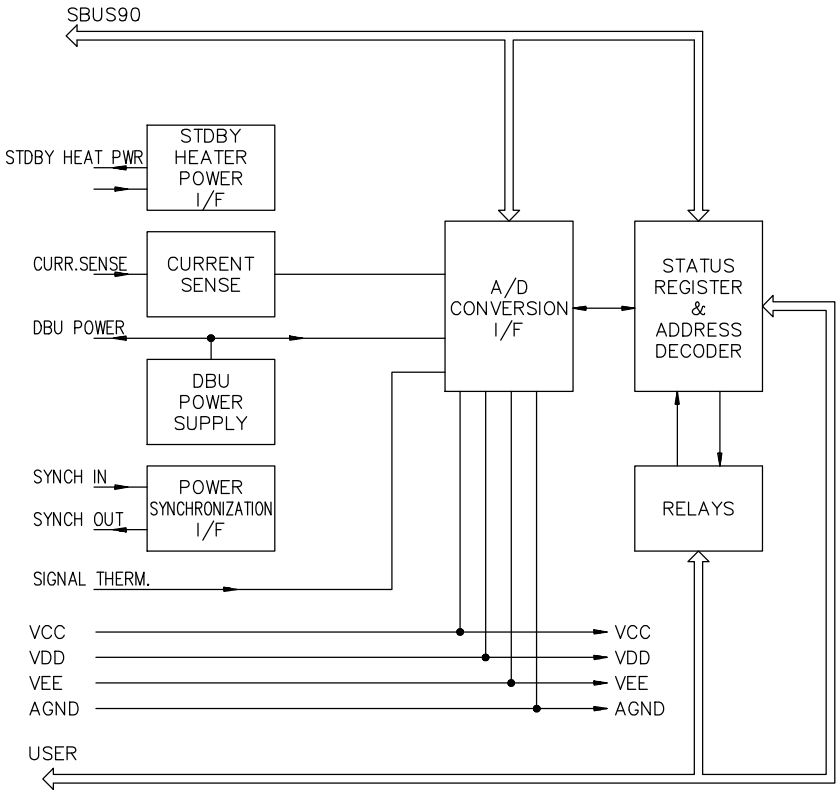


Figure 4.5-5: Miscellaneous Board Block Diagram

Switch_board

This board aims to distribute Conditioned Primary Power (CPPW) to some devices of the EMCH.
This board provides:

S/W commanded switches to power a.m. devices
Current limitation and auto cut-out function in case of short circuit.
Monitor signals relevant to switches status

This board is interfaced to Miscellaneous board.

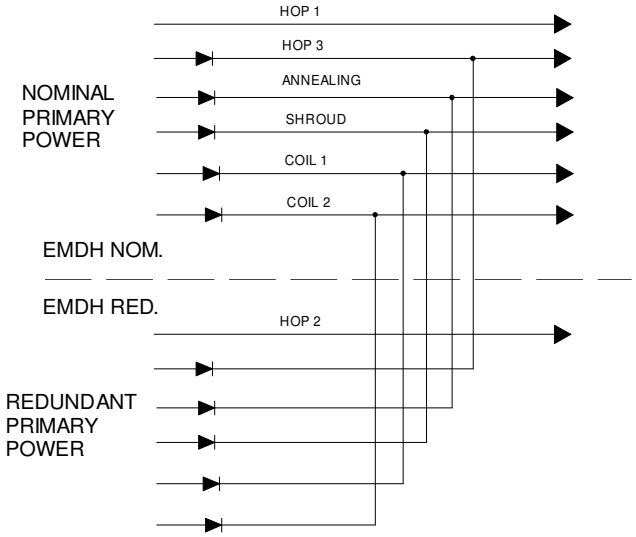


Figure 4.5-6: Switch Board Block Diagram

DC/DC Converter_board

This board is devoted to convert the 28 VDC power coming from the XMM power line and to distribute the converted power to all the other electronic boards. It also provides secondary power to the DBU.

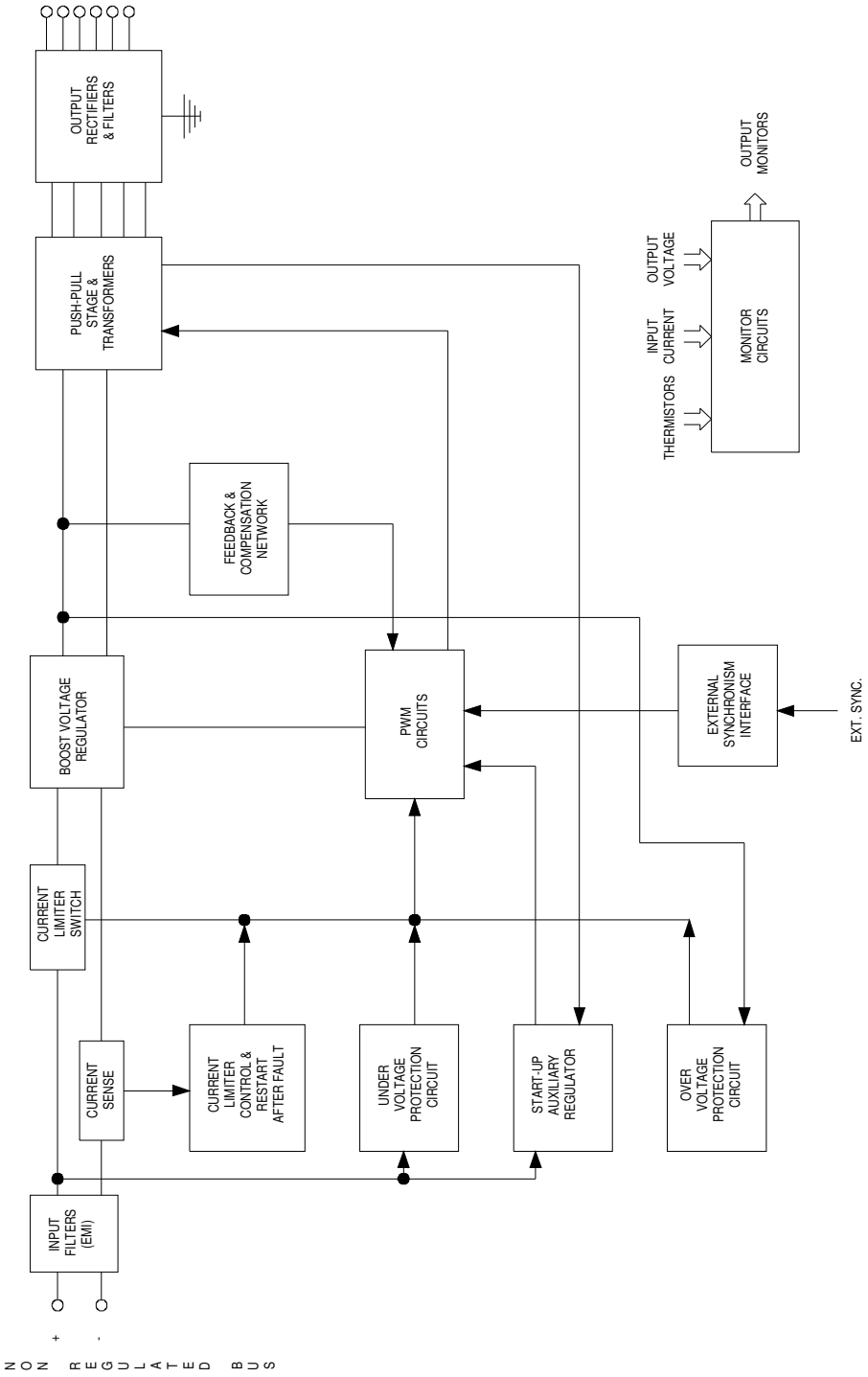


Figure 4.5-7: DC/DC Converter Board Block Diagram

EmiFilter_board
The EMI Filter provides electro-magnetical interface protection for the input primary power.

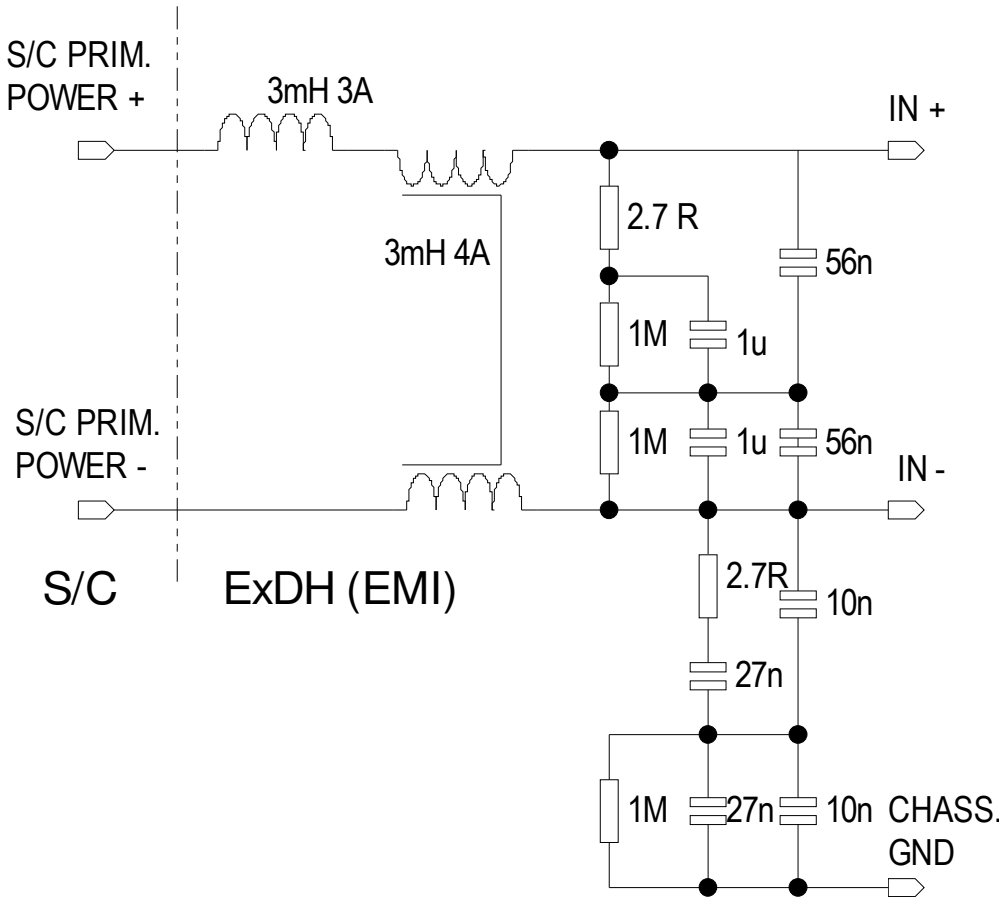


Figure 4.5-8: EMI Filter Electrical Diagram

Mother_board
The Motherboard allows communication and data transfer among the boards connected to the unit bus.

4.6 EPIC MOS VOLTAGE CONVERTER (EMVC) (AD 7, §9.3.5.)

The EMVC unit is composed of two cold redundant components (RD 9, §1.4.1.):
- LVC M main converter
- LVC R redundant converter

The input power voltage is +26 ÷ +30 V (RD 9, §3.1.). The EMVC unit has two input primary power lines from EMDH unit. It is synchronised by a EMDH supplied clock at 131.072 kHz +/- 0.1 % and operates at the same frequency: if this clock is not available, the DC/DC converters of the EMVC unit operates within their requirements with a free running switching frequency of 131.072 kHz +/- 10 %. The synchronisation signal is provided through transformer decoupling (RD 9, §3.3.). The secondary voltages with dedicated return lines are available at EMVC output connectors. All return connection combination are performed using isolated studs (RD 9, §3.4.).

5. UNIT FUNCTIONS AND MODES

5.1 EPIC MOS CAMERA HEAD (EMCH) (AD 7 §9.3.2.)

5.1.1 Allocated Functions

The goal of the Camera Head is to convert the incoming X-ray photons, in the energy range between 0.1 and 15 keV, into electrical signals. Its scientific output is made of analogue signals as generated by preamplifiers: any signal conditioning shall be performed by the downstream electronics.
To this aim, the Camera Head has to reject both cosmic rays and incoming low-energy (i.e. IR-optical-UV) photons; moreover, it must be possible to monitor and control both temperature and pressure.

5.1.2 Operating Modes

There are two basic types of read-out for a single CCD:
1) Imaging
2) Timing
It must be noted that they do not coincide with the modes of operation of the whole Camera System (AD 7, §3.1.5.).

Imaging readout

There are 6 parameters for the imaging read-out of a single CCD:

x_0 = x-position of the pixel at the lower left-hand corner of the window;

y_0 = y-position of the pixel at the lower left-hand corner of the window;

Δx = window size in the x-direction in number of pixels;

Δy = window size in the y-direction in number of pixels;

T_{int} = frame integration time;

N = (1,0) read-out from left node;
(0,1) read-out from right node;
(1,1) read-out from both nodes.

In the "Full Window" option, $x_0 = y_0 = 1$, $\Delta x = 610$ and $\Delta y = 602$ and the following sequence of operations is performed:

a) The image is transferred from the integration area to the storage area by shifting the rows 602 times;

b) Pixels of the lowermost line of the storage area (read-out line) are read out either from one node or from both nodes (half-line to each node);

c) The image in the storage area is shifted by one row;

... The operations b) and c) are repeated for a total of 602 times;

d) The operation a) is repeated starting with a time delay of T_{int} from the time when the previous operation a) ended.

It is understood that T_{int} can be both greater and lower than T_0, where T_0 is the read out time for a frame. In principle, if T_{int} is less than T_0, the CCD is operated by first rejecting the image formed in the integration area during the readout of the previous frame and then using the sequence listed above with a time delay of T_{int}. In this case, the CCD is "active" only partially, i.e., during a periodic window in time.
The "Partial Window" option is similar to the Full Window option with the only difference that only the pixels in the window $(x_0, y_0, \Delta x, \Delta y)$ are actually read out while the others are rejected. Since T_0 is smaller than that in the full window case, then T_{int} can be smaller.

Timing readout

There are 3 parameters for the timing read-out of a single CCD. They are as follows:

Δx = size in the x-direction (in number of pixels) of the strip of columns which are under observation. This strip is always located centrally with respect to the CCD;

Δy = size in the y-direction (in number of pixels) of the section of the strip that is binned (summed);

N = (1,0) read-out from left node;
(0,1) read-out from right node;
(1,1) read-out from both nodes.

The following sequence of operations is performed:

a) The image is partly transferred from the integration area to the storage area by shifting the rows Δy times; the Δy rows that enter the storage area are integrated into the topmost row (602nd);

b) The content of the storage area is shifted by one row (after this operation, the 602nd row of the storage area has no charge);

c) The content of the read-out line (the lowermost of the storage area) is read either fully (if $\Delta x=610$) or partly (if $\Delta x<610$). In the latter case, the pixels not belonging to the strip are rejected. The reading can occur from one or both nodes according to the option selected.

d) The operation a) is repeated.

It is understood that no valid information is obtained for the first 602 times that this sequence is performed, because at the beginning the storage area does not contain valid information.

5.2 EPIC MOS ANALOGUE ELECTRONICS (EMAE) (AD 7, §9.3.3.)

5.2.1 Allocated Functions

The EMAE has two main functions:
- to generate the appropriate clocks and bias voltages for the required functioning of the CCDs;
- to convert the analogue signals from the EMCH into digital signals with a 12 bit resolution and to send them to the EMCR through 8 channels (2 related to the central CCD, the other ones pairwise to the peripheral CCDs).

Moreover, it has to perform the following operations:
- to manage the thermal control of the CCD array;
- to drive the filter wheel and the calibration source;
- to monitor the camera head vacuum and the door bellows pressure;
- to receive commands from EMCR through a redundant interface;
- to receive secondary power from the EMCR;
- to read-out relevant parameters including temperatures, heater power consumption, voltages, calibration source and filter wheel position.

5.2.2 Functional Description

Each analogue chain amplifies and conditions the signal prior to the ADCs. The amplifiers are preceded by multiplexers to select which head amplifier is connected to each input (i.e. the CCD output nodes and the CCD simulator). The configurations given in Tab.5.2.2-1 and 2 ensure that all the CCDs can be readout even with a faulty chain or faulty CCD node (but not with both faults) (RD 5, §3.2).

Mux State	Analogue Chain 1	Analogue Chain 2
0	CCD 1 node 2	CCD 1 node 1
1	CCD 1 node 1	CCD 1 node 2
2	CCD simulator	CCD simulator

Table 5.2.2-1: input multiplexing for central CCD

Mux State	Analogue Chain 1	Analogue Chain 2
0	CCD a node 1	CCD b node 2
1	CCD b node 2	CCD a node 1
2	CCD simulator	CCD simulator

Table 5.2.2-2: input multiplexing for outer CCDs for each pair (CCD a and b refer to CCD pairs CCD2 and 3, CCD4 and 5, CCD6 and 7)

Each analogue chain has an ADC, with a resolution of 12 bits, which transmits serially the output data to the EMCR (RD 5, §3.3). Moreover it includes power switching so that the total power

consumption of the instrument may be reduced when chains are not active. In case of failure and use of contingency operation, the power switching ability will also be needed (RD 5, §3.2).

All functions within the EMAE are controlled by programmable sequencers synchronised to a single timing source. They control:

- CCD clocks
- Analogue Processing
- ADCs
- Data output to the EMCR

The sequencers are driven by a high-stability crystal oscillator of a fixed frequency: this oscillator determines the signal integration time and, hence, the system gain. The sequencers are commandable to take their timing from a second, redundant oscillator (RD 5, §3.4).

The logic outputs from each sequencer are amplified and shaped, to drive the CCDs. Each CCD has separate clock drive circuits. The serial clocks are switchable between one-node readout in either direction and two-node readout. These selections are available for all CCDs (RD 5, §3.5.1).

The EMAE shall monitor the following two interfaces: a reed switch monitoring the camera door open (reed closed when door fully open) and a Hall sensor monitoring the door rotate bellows fully retracted (active when retracted) (RD 5, §4.11).

5.3 EPIC MOS CONTROL & RECOGNITION (EMCR)

5.3.1 Allocated functions (RD 3, §6)

The EMCR has two main functions:
- to manage the EMAE via the controller (CTR);
- to perform real time data analysis via the Event Detection Unit (EDU).

It has the following capabilities:
- to acquire and decode the digital scientific data coming from EMAE through 8 Scientific Digital Data (SDD) interfaces (one for each Analogue Chain);
- to implement the event recognition algorithm, separately for each input channel;
- to process the scientific data according to the selected operating mode;
- to transmit the processed scientific data to the EMDH through 8 channels (one for each SDD I/F);
- to store and load all the read-out sequences (see INITIALIZATION mode), with their relevant parameters;
- to store permanently (i.e. in PROM) all the data and the program necessary for its full performance;
- to perform temperature control in the extra-heating process (de-icing, annealing and decontamination mode);
- to send commands to the EMAE and to collect HK data from the EMAE;
- to control the EMAE sequencer programs;
- to acquire and process the monitors from the EMVC;
- to receive, decode and execute the commands coming from the EMDH;
- to send HK data to the EMDH through a redundant interface;
- to receive secondary power (main and redundant) from the EMVC;
- to make the “oring” of the secondary power and to forward it to the EMAE;
- to control the filter wheel and the calibration source;
- to provide software & data load capabilities;
- to provide EDU test & self test capabilities.

The EDUs can be in different Scientific Data Processing Modes of operation (SDPM): the mode of each EDU is selectable by command. The EDU has the following functions common to all SDPMs:
- to subtract the “Gatti number” (see below)
- to subtract the offset in x and y axis
- to compare the result with the threshold
- to count the pixels above the threshold in a frame or pseudo-frame
- to memorise the status of the time counter at the beginning of a frame
- to inhibit lines and rows
- to transmit an header at the beginning of frame or sequence towards the EMDH
- to transmit a trailer at the end of a frame or sequence towards the EMDH
- to generate a pulse at the end of a frame or pseudo-frame towards the EMDH
- to store a library of patterns and associated masks.

The EDU has the following SDPM specific functions:

- imaging SDPM
  - to seek the pattern of the 5x5 matrix in the library
  - to determine the position of the pixels with the highest energy
  - to compute the sum of the pixels above the threshold in the 3x3 matrix
  - to compute the sum of the pixel below the threshold in the 3x3 matrix
  - to compute the sum of the pixel below the threshold in the periphery
  - to count the number of pixels above the threshold in the periphery
  - to transmit an imaging data block if the pattern is recognised with the highest energy in the central pixel
- timing SDPM
  - to seek the pattern of the 5x5 matrix in the library
  - to transmit a timing data block if the pattern is recognised towards the EMDH
  - to transmit a timing block at the end of a pseudo-frame towards the EMDH
- transparent SDPM
  - to transmit for each pixel a transparent data block towards the EMDH
- threshold SDPM
  - to seek the pattern of the 5x5 matrix in the library
  - to transmit a threshold data block if the pattern is recognised towards the EMDH

In timing mode a pseudo-frame is defined as a block of 1024 lines and a sequence is a block of pseudo-frames. The uplinkable library contains up to 32 patterns and associated masks.

The transmission of the processed scientific data to the EMDH is done by means of the High Bit Rate interfaces (HBR): any HBR channel can be active at the same time. Each HBR is in one of the following modes, according to the EDU SDPM: 1) imaging; 2) timing; 3) transparent; 4) threshold; 5) inactive.

The EMCR receives and decodes commands coming from the EMDH by means of the Low Bit Rate interface between EMCR and EMDH (LBR C/H). It sends an acknowledge format to the EMDH after reception of a command: in case a command has not been correctly received, a negative acknowledge code is transmitted. The EMCR transmits a command execution status when requested by the EMDH.

The EMCR can route to the EMAE, by means of the Low Bit Rate interface between EMCR and EMAE (LBR A/C), the commands and the parameters received from the EMDH in any mode of operation (except Off and Initialisation): it is able to generate and send commands and parameters to the EMAE. It is able to store in its RAM up to 5 sequencer programs equivalent to 4 kbytes: it generates and transmits a 8-bit sequential number (called “Gatti”) to the EMAE via the LBR A/C line.

The EMCR controls the timing of the focal plane while receiving a “Start Observation” command and until it receives a “Stop Observation” command from the EMDH. It controls the execution of up to 4 sequencer programs: a sequencer can be controlled synchronously or asynchronously among the other sequencers. It performs the frame timing controlling of the focal plane with a resolution of 0.1 s and operates a sequencer with a maximum integration time of 25.6 s (in a frame by frame mode only).

The EMCR has to send 16 bit housekeeping data words to the EMDH as a single block of data and to ask for 8 bit housekeeping data words to the EMAE by means of the LBR A/C interface (in order to refresh its housekeeping data area). The EMCR controller maintains a housekeeping data area in RAM: all the housekeeping data are updated regularly with a period of 8 s. The transmission of the HK data packet is initiated by an EMDH command. The H/K data block shall content the following informations:

⇒ the status of the eight EDUs
⇒ the EMCR/EMVC analogue H/Ks (temperature and voltage)
⇒ the EMAE digital H/Ks
⇒ the PROM program version
⇒ the RAM program version
⇒ the initialisation check status
⇒ the status of the interfaces

While in Extra-heating mode, the EMCR is able to monitor and control the focal plane extra-heating process (de-icing/annealing/decontamination). It sends to the EMAE (by means of the LBR A/C) a command to switch on the annealing heater when the housekeeping of the annealing temperature sensor is below a previously set low threshold. In the same way, the EMCR sends to the EMAE a command to switch off the annealing heater when the housekeeping temperature sensor is above a previously set high threshold. Both the low and the high thresholds have to be set by a LBR C/H command. The annealing temperature is monitored by the EMCR every 30 s.

While in Stand-by mode the EMCR is able to control the EMCH filter wheel by means of command/status via the LBR A/C interface. When requested by the EMDH the EMCR performs a synchronisation sequence of the filter wheel mechanism and sends the number of steps required for reaching the asked position.

While in Stand-by mode the EMCR is able to control the EMCH calibration source by means of command/status via the LBR A/C interface.

The EMCR has the capability to dump the content of its own memory devices (both PROM and RAM) when requested by the EMDH only if in Stand-by mode: it allows the EMDH to patch/dump block of data and to load/dump entire software code. Before loading software into RAM it is mandatory to switch the CTR to its PROM program.

While in EDU test mode the CTR is able to simulate the EMAE scientific data by means of a SDD interface; moreover, it is able to generate pre-defined images or to use uplinked test image. One or more EDU are operated in test with the same test image.

The EMCR supplies the EMAE with secondary power lines whatever the active EMVC part (main or redundant).

An EMCR self test can be executed on request, usually during the initialisation mode. During this self test the EMCR performs:

- a PROM check to verify the integrity of the code store there;
- a RAM check to verify the functionality of all the RAM devices (the current content is then lost);

- check of EDU hardware (I/F, offset & patterns RAM, threshold register).

Since the RAM check algorithm is a destructive one the software code and data block must be re-loaded after a self test.

5.3.2 Modes of operation (RD 3, §6.3)

5.3.2.1 General

The modes of operation of the EMCR are:

- Off
- Initialisation
- Stand-by
- Observation
- EDU Test
- Extra-heating

The selection of the mode of operation is made by means of the EMDH commands: the EMCR is not required to automatically switch from one operative mode to another (except for Initialisation to Stand-by).

5.3.2.2 Off Mode

In this mode the EMCR is completely OFF: it does not receive power from neither the Nominal nor the Redundant Secondary Power lines.

5.3.2.3 Initialisation Mode

The EMCR enters this mode whenever a power-on occurs: during this mode it performs a “unit self initialisation”. When all the jobs to be performed in Initialisation Mode have been completed the EMCR enters the Stand-by mode.

The EMCR can enter this mode from any other mode (except Off) by command: in this case it re-executes all the Initialisation steps.

5.3.2.4 Stand-by Mode

The EMCR enters this mode of operation when:

1) the Initialisation phase has been completed;
2) the EMCR is in any mode of operation (except Off) and an EMDH command to enter Stand-by mode is received.

The EMCR has the possibility to execute (in RAM) the PROM default code or an uplinked code. When the EMCR is commanded to enter this mode from Observation Mode or EDU Test Mode by the EMDH, the transmission of data formats through the HBR interfaces is resumed.

5.3.2.5 Observation Mode

The EMCR can enter this mode from the Stand-by mode only. In this case the EMCR loads into the EMAE all the required parameters and sequences and trigs the execution of the EMAE sequencer programs (by means of LBR C/H commands) according to a pre-defined configuration. The EMCR resumes this mode when receiving a Stop Observation command.

5.3.2.6 EDU Test Mode

The EMCR can enter this mode from the Stand-by mode only. Before the execution it configures data processing mode of the EDU under test according to a previously uplinked configuration. The EMCR resumes this mode when receiving a Stop EDU Test command.

5.3.2.7 Extra-heating Control Mode

The EMCR can enter this mode from the Stand-by mode only. During the execution the EMCR uses the previously uplinked thresholds. This mode is resumed when a Stop Extra-heating Control command is received.

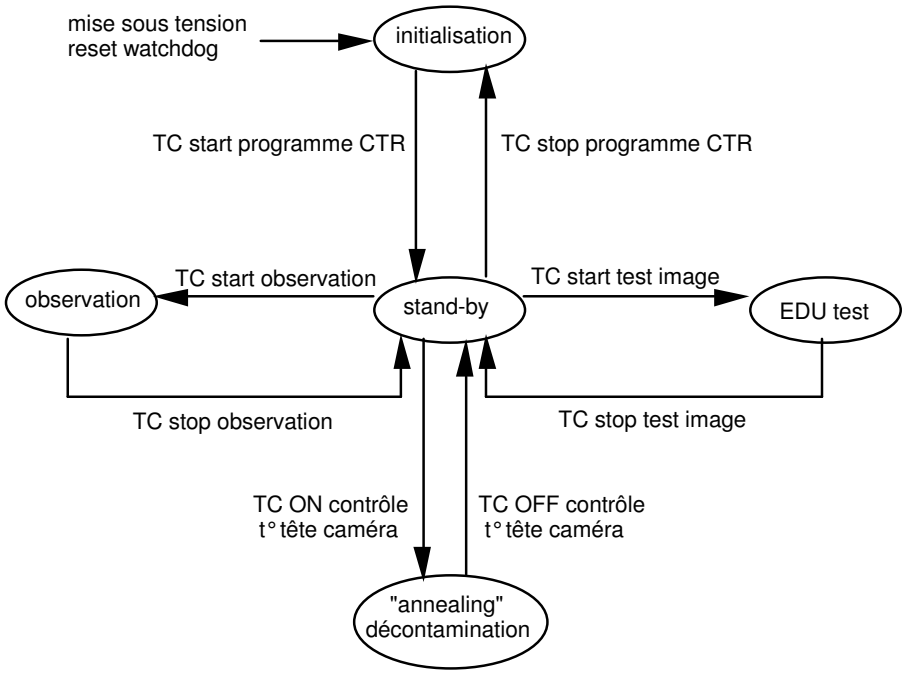
5.3.2.8 Relations to the EMCS Modes of Operation

In the following Table the relations between the EMCS and the EMCR operating modes are outlined:

EMCS operating modes	EMCR operating modes
Off	Off
Stand-by	Stand-by
Idle	Stand-by
Annealing	Extra-heating
Prime	Observation
Fast	Observation
In-Flight Test	Observation/EDU Test/Stand-by
Calibration	Observation

5.3.2.9 Transitions between modes of operation

In the following Figure the transition diagram relevant to the modes of operation of the EMCR is shown:



5.4 EPIC MOS DATA HANDLING (EMDH)

5.4.1 Allocated functions (AD 7, §9.3.6.)

The EMDH is the master unit of the EMCS. It has to perform the following tasks:
- to receive the intermediate scientific data from the EMCR through 8 channels (one for each SDD I/F), according to the selected operating mode;
- to perform the upper/lower thresholding of the event energies (see PRIME and FAST mode);
- to reject the contribution from the bright pixels and to store the bright pixel table;
- to implement the pattern discrimination related to the event recognition algorithm (see PRIME and FAST mode);
- to implement the algorithm for the offset/variance mode;
- to implement the non-destructive data compression;
- to implement the telecommand and telemetry packet structure;
- to prepare and store in the appropriate queue the telemetry source packets and to transmit them to the OBDH bus;
- to manage the output overflow conditions (see PRIME and FAST mode);
- to store 360,448 (16-bit) words of scientific intermediate data (in order to fulfil the EMCS storage requirements of 40,000 events);
- to implement the requirement on SCET and local time management;
- to manage the telecommand packets received from the OBDH and to forward the appropriate commands to the EMCR and, through the EMCR, to all the other units of the chain, according to the selected operating mode;
- to manage the SW patch and dump of the EMCR;
- to manage the collection of the HK data coming from the EMCR and, through the EMCR, from the other units of the chain;
- to activate and deactivate the EMCH devices;
- to receive primary power from the S/C and to re-route it to the EMVC;
- to control and forward primary power to the EMCH;
- to control the Venting Valve and the Door Mechanism;
- to store permanently (i.e. in PROM) all the data and the program necessary for its full performance;
- to control the secondary shroud heater according to the telecommands received.

The EMDH is fully cold redundant.

The EMDH has the capability to receive the scientific data coming from the 8 HBR channels. Since all the HBR channels may be active at the same time, the EMDH is able to collect the data coming from these channels in a parallel manner. The number of HBR channels active at the same time is specified according to the selected mode of operation.

The EMDH has the capability to store input scientific data coming from the HBR channels in a temporary manner. The temporary storage area for scientific data allows the storage of all the data of one HBR in transparent channel mode, i.e. 360,448 (16 bits) words; moreover, it allows limited storage of the data from all the active HBRs. The memory size related to each active channel (buffer) is properly sized according to the scientific needs, but the global size can not be lower than 192 kword. The temporary storage area is divided into sub-areas (buffers), each one dedicated to each active HBR channel. The EMDH indicates the amount of used memory for each buffer (HBR)

in the HK TM report. A warning flag in the HK data is generated when more than 75 % of the buffer related to a given HBR channel is filled (in imaging, threshold or timing mode only). In case the storage area assigned to a given HBR is about being filled, the further incoming events are recognised by the EMDH but it suspends the scientific data storage for that HBR: this function is named “Counting Mode”. The number of frames (cycles) rejected as well as the number of 16 bit words rejected is counted and included in an HK TM report together with the start and end time of this overflow condition. The ending of the overflow condition is set when the related storage area is less than about 25 % filled (in Imaging, Threshold and Timing channel mode only) (RD 7, §7.2.2.).

The EMDH is able to process the data received from each HBR channel. The following capabilities are implemented:

- Upper Thresholding (Cosmic Ray Rejection);
- Lower Thresholding (Noise Rejection);
- Bright Pixel Rejection;
- Pattern Discrimination (Cosmic Ray Rejection);
- Non-Destructive Data Compression;
- Data Reduction;
- Offset/Variance Computation;
- Threshold Mode Data Reduction.

For each single HBR the execution of upper thresholding, lower thresholding, pattern discrimination, data reduction, non-destructive data compression and bright pixel rejection functions can be enabled or disabled together by an OBDH command. The characteristics of these capabilities are established in RD 7, §7.2.3

The EMDH has the capability of OBDH packet terminal, as established in AD 1 (RD 7, §7.2.4).

The EMDH is capable to generate telemetry source packets for any OBDH bus bandwidth equal to or lower than 16 kbits (RD 7, §7.2.5). It implements the telemetry packet structure established in AD 6 and generates source telemetry packets.

The EMDH receives and decodes commands as specified in AD 6 as well “low level” RBI commands (RD 7, §7.2.7.).

The EMDH has the capability to distribute towards the EMCR all those OBDH telecommands whose destination is the EMCR or the EMAE/EMCH, according to the specified LBR I/F protocol. It has also the capability to send local commands and data to the EMCR and to receive responses from it according to the specified LBR I/F protocol.

The EMDH has the capability to receive housekeeping data from the EMCR. Each single information is coded on one 16-bit data word. At least once every 8 seconds the EMDH commands the EMCR to transmit in a single shot its HK data on the LBR channel. It has a time-out function on the request of HK data: in case of response time-out, the EMDH flags the error condition in the HK source packet and includes in the TM packet the EMCR last updated HK data. The HK data collection and TM packet generation functions are always active in any mode of operation of the EMDH (Initialisation and On-Ground Test excluded). The function may be “non active” when the EMDH is under test during the In-Flight Test mode (RD 7, §7.2.9.).

The EMDH has the capability to load or dump the content of its own memory devices (both PROM and RAM) when requested by the Command and Data Management System (CDMS). Two kinds of patch/load are foreseen:

- Data/Parameters patch/load;
- EMDH Nominal S/W patch/load.

Three kinds of dump/checksum are foreseen:

- Data/Parameters dump/checksum;
- EMDH Nominal S/W dump/checksum;
- EMDH Basic S/W load or dump.

Any patch/load operation related to EMDH S/W is executed only when the unit is in Basic S/W Mode (RD 7, §7.2.10).

The EMDH allows the CDMS to load or dump parameters and S/W code into/from the EMCR; (RD 7, §7.2.11.).

The EMDH provides an on board timer of at least 43 bits, directly clocked by the OBDH clock signal (524288 Hz), in order to allow counting up to 2^{23} seconds with a resolution of 2^{-19} seconds. It forwards a 1 Hz pulse signal and a synchronisation pulse to the EMCR: these signals are synchronous with the OBDH bus clock. The time interval between two consecutive synchronisation pulses is, by default, of 9 hours, but it can be changed by the CDMU with the proper TC. The EMDH sends a synchronisation pulse before entering any scientific observation mode (RD 7, §7.2.12.).

The EMDH is capable to activate/deactivate the conditioned primary power switch devices upon reception of the specific telecommand from the OBDH or when some condition occur. In case of reception of a TLC for the activation of any of the HOP switch device, the EMDH automatically de-activates the switch device after a fixed number of seconds from the switch activation. The EMDH is capable to automatically deactivate the conditioned primary power switch devices whenever an overcurrent condition on the driven line is detected (cut-off function): after the automatic intervention the EMDH allows the CDMU to activate the switch again; whenever the cut-off function has intervened the EMDH flags such a condition with a major anomaly TM packet. At least every 8 seconds the EMDH monitors the status of the conditioned primary power switch devices and the status of the current cut-off function. Whenever the status of the switch devices does not match the expected one the EMDH signals the condition by means of a major anomaly TM report (RD 7, §7.2.13.).

The EMDH is able to monitor the temperature of the CCD focal plane against a minimum and a maximum value: the temperature value of the CCD focal plane is part of the EMCR/EMAE HK data. The CCD thermal monitoring function is active in any EMDH operating mode (except for Initialisation, Basic S/W and In-Flight Test). The temperature limits are set by proper TC. In case the acquired temperature value lies outside the set range, the EMDH generates a major anomaly TM report, in order to flag such a condition to the OBDH bus master (RD 7, §7.2.14.).

The EMDH has to detect the missing of the OBDH bus link. In case the OBDH clock signal is lost for more than 250 ms, the EMDH automatically enters the Safe Stand-by operating mode (RD 7, §7.2.15.).

The EMDH provides a watch-dog function with a time-out value that shall not be greater than 8 seconds. In case of watch-dog time-out occurrence, the EMDH continues its activities but flags the condition into the RBI status register (RD 7, §7.2.16.).

The EMDH provides a dedicated memory buffer devoted to allow temporary storage of EMCR down-loaded/up-loaded data (RD 7, §7.2.17.).

5.4.2 Operating Modes (RD 7, §7.3.)

5.4.2.1 General (RD 7, §7.3.1.)

The operating modes of the EMDH resumes those ones of the whole EMCS. In detail, they are as follows:

- Off
- Initialisation
- Safe Stand-by
- Idle
- Prime
- Fast
- CCD Diagnostic
- Offset/Variance
- Extra-Heating
- In-Flight Test Mode
- On-Ground Test Mode
- Basic S/W Mode

The selection of the mode of operation is done by means of mode transition OBDH commands, i.e. the EMDH is not required to automatically switch from one operative mode to another (except for initialisation to stand-by and initialisation to on-ground test mode).

5.4.2.2 Off Mode (RD 7, §7.3.2.)

In this mode the EMDH is completely off. The EMDH does not receive power from either the nominal and the redundant power lines.

5.4.2.3 Initialisation Mode (RD 7, §7.3.3.)

The Initialisation Mode is subdivided into two phases:

1) *First Initialisation Phase:* the EMDH initialise its H/W devices and checks the integrity of the S/W codes;
2) *Second Initialisation Phase:* the EMDH prepares its following mode transition.

5.4.2.4 Safe Stand-by Mode (RD 7, §7.3.4.)

The EMDH enters this mode of operation when:

- the Initialisation mode operations have been completed
- the EMDH is in any operating mode and a mode transition TC to enter the Safe Stand-by mode is received
- The EMDH is in On-Ground Test Mode and a dedicated command to enter the Safe Stand-by Mode is received from EGSE

This Mode foresees an initialisation phase to be performed only in case of transition from the Initialisation Mode: in this phase the EMDH initialise its S/W and Operating System, requires to the EMCR the transmission of EMCR/EMAE initialisation report and generates the event TM report containing the initialisation results.

In this Mode the EMDH is capable to perform, for all operating mode duration, the following operations:

- EMDH/EMCR/EMAE H/K data periodic collection and H/K TM report generation
- to receive, decode and execute all the foreseen TCs
- on-board time management
- CCD thermal monitoring
- conditioned primary power switch devices control and monitoring (arming and activation of HOPs)
- OBDH bus link monitoring
- watch-dog function

In this mode the EMDH can perform just once:

- closure of the Filter Wheel device, by activating the relevant conditioned primary power switch and sending the proper local command to the EMCR;
- activation of the EMAE focal plane thermal control, by sending the proper local command to the EMCR.

5.4.2.5 Idle Mode (RD 7, §7.3.5.)

The EMDH enters this mode of operation when the EMDH is in any mode of operation (Off and Initialisation excluded) and a mode transition TC to enter the Idle mode is received. In this Mode the EMDH is capable to perform, for all operating mode duration, the following operations:

- to receive, decode and execute all the foreseen TCs
- on-board time management
- CCD thermal monitoring
- conditioned primary power switch devices control and monitoring (activation of Coil 1 and Coil 2 switches for powering the Filter Wheel)
- OBDH bus link monitoring
- watch-dog function

It must be noted the the Idle Mode is the status which allow to configure the experiment before to execute one of all successive modes.Parameters, thermal settling, chains configuration, CCDs sequences are loaded in that mode, and executed when the system is commanded to run the main scientific or engineering modes.

5.4.2.6 Prime Mode (RD 7, §7.3.6.)

The EMDH enters this mode of operation when it is in Idle and a mode transition TC to enter Prime Mode is received. In this Mode the EMDH is capable to perform, for all operating mode duration, the following operations:

- EMDH/EMCR/EMAE H/K data periodic collection and H/K TM report generation
- on-board time management

- CCD thermal monitoring
- conditioned primary power switch devices monitoring
- OBDH bus link monitoring
- watch-dog function

When the OBDH command to enter the Prime Mode is received, the EMDH performs the mode initialisations (HBR channels programming, data structure preparation, etc.) and starts the scientific data collection from the HBR channels according to the HBR configuration previously received in Idle mode by means of the proper TCs.

Once the scientific data acquisition is started, the EMDH performs the scientific data storage and the scientific data processing according to the configuration TCs received during the Idle mode.

Once the EMDH is ready to acquire and process the scientific data of the HBR channels, it sends a synchronisation pulse to EMCR and commands the EMCR to start the observation by sending the proper local command.

5.4.2.7 Fast Mode (RD 7, §7.3.7.)

The EMDH enters this mode of operation when it is in Idle and a mode transition TC to enter Fast Mode is received. In this Mode the EMDH is capable to perform, for all operating mode duration, the following operations:

- EMDH/EMCR/EMAE H/K data periodic collection and H/K TM report generation
- on-board time management
- CCD thermal monitoring
- conditioned primary power switch devices monitoring
- OBDH bus link monitoring
- watch-dog function

When the OBDH command to enter the Fast Mode is received, the EMDH performs the mode initialisations (HBR channels programming, data structure preparation, etc.) and starts the scientific data collection from the HBR channels according to the HBR configuration previously received in Idle mode by means of the proper TCs.

Once the scientific data acquisition is started, the EMDH performs the scientific data storage and the scientific data processing according to the configuration TCs received during the Idle mode.

Once the EMDH is ready to acquire and process the scientific data of the HBR channels, it sends a synchronisation pulse to EMCR and commands the EMCR to start the observation by sending the proper local command.

5.4.2.8 CCD Diagnostic Mode (RD 7, §7.3.8.)

The EMDH enters this mode of operation when it is in Idle and a mode transition TC to enter Diagnostic Mode is received. In this Mode the EMDH is capable to perform, for all operating mode duration, the following operations:

- EMDH/EMCR/EMAE H/K data periodic collection and H/K TM report generation
- on-board time management

- CCD thermal monitoring
- conditioned primary power switch devices monitoring
- OBDH bus link monitoring
- watch-dog function

When the OBDH command to enter the CCD Diagnostic Mode is received, the EMDH performs the mode initialisations (HBR channels programming, data structure preparation, etc.). Once ready the EMDH sends a synchronisation pulse to the EMCR and sends a “start observation” local command to the EMCR. Then the EMDH starts the data acquisition, from one HBR only (according to the HBR configuration TC received in Idle mode) and for one frame only starting from the frame specified in the mode transition TC itself.

The EMDH is capable to collect scientific data from that HBR working in transparent channel mode. Any data coming from other HBR channels are ignored.

The EMDH implements the scientific data storage capability. At least 360000 (16-bit) words of the scientific data storage area are reserved to the one only HBR active channel.

Whenever all pixel data have been received, the EMDH implements the science report packet preparation capability. At the end of transmission of all TM packet necessary to send to the OBDH the stored pixel data, the EMDH continues its own activities (scientific one excluded) and stands waiting for an Idle Mode transition TC.

5.4.2.9 Offset/Variance Mode (RD 7, §7.3.9.)

The EMDH enters this mode of operation when it is in Idle and and a mode transition TC to enter Offset/Variance Mode is received. In this Mode the EMDH is capable to perform, for all operating mode duration, the following operations:

- EMDH/EMCR/EMAE H/K data periodic collection and H/K TM report generation
- on-board time management
- CCD thermal monitoring
- conditioned primary power switch devices monitoring
- OBDH bus link monitoring
- watch-dog function

When the OBDH command to enter the Offset/Variance Mode is received, the EMDH performs the mode initialisations (HBR channels programming, data structure preparation, etc.). Once ready the EMDH sends a synchronisation pulse to the EMCR and sends a “start observation” local command to the EMCR. Then the EMDH starts the data acquisition, from one HBR only (according to the HBR configuration TC received in Idle mode) and for one frame only starting from the frame specified in the mode transition TC itself.

The EMDH is capable to collect scientific data from that HBR working in transparent channel mode. Any data coming from other HBR channels are ignored.

The EMDH implements the scientific data storage capability. At least 360000 (16-bit) words of the scientific data storage area are reserved to the one only HBR active channel.

Whenever all pixel data have been received, the EMDH performs the on the received data the Offset/Variance determination function. Then the EMDH stores the results in the EMCR data temporary storage area and generates all the TM packets necessary to send to the OBDH the computed offset and variance data. At the end of all TM packets transmission, the EMDH continues its own activities (scientific ones excluded) and stands waiting for an Idle Mode transition TC.

5.4.2.10 In-Flight Test Mode (RD 7, §7.3.10.)

The EMDH enters this mode of operation when it is in Idle and and a mode transition TC to enter In-Flight Test Mode is received. The TC brings a parameter which indicates which In-Flight Test Mode is required. The following sub-modes are foreseen:

- EMDH test
- EMCR test
- EMCS test

Regardless the required sub-modes, when in In-Flight Test Mode the EMDH is capable to perform, for all operating mode duration, the following operations:

- to receive, decode and execute all the foreseen TCs
- on-board time management
- CCD thermal monitoring
- conditioned primary power switch devices monitoring
- OBDH bus link monitoring
- watch-dog function

In case the required sub-mode is “EMDH Test” the EMDH is able to perform internal checks upon reception of proper TCs (Start Sporadic or Periodic Task). When the commanded check has been completed (or stopped by a Stop Periodic Task TC), the EMDH saves in a dedicated memory area the test results.

In case the required sub-mode is “EMCR Test” the EMDH activates all functions to:

- acquire data from HBR channels
- store the data
- process the data
- generate scientific TM packets

and sends a “start EDU test image” local command to the EMCR. The above functions are activated in accordance with the HBR configuration TCs received during the Idle mode, exactly as the EMDH does during the Prime or Fast operating mode: all the requirements stated in Prime and Fast mode are also applicable when EMDH is commanded to enter this sub-mode. This In-Flight Test sub-mode aims to check the behaviour of both the EMCR (which works with test data and not with the real ones) and the EMDH (which works has in Prime or Fast modes).

In case the required sub-mode is “EMCS Test” the EMDH activates all functions to:

- acquire data from HBR channels
- store the data
- process the data
- generate scientific TM packets

in accordance with the HBR configuration TCs received during the Idle mode, exactly as the EMDH does during the Prime or Fast operating mode: all the requirements stated in Prime and Fast mode are also applicable when EMDH is commanded to enter this sub-mode. Moreover, the EMDH sends to the EMCR a “turn filter wheel” local command, commanding the positioning of the filter wheel at the calibration source, and a “start observation” command. This In-Flight Test sub-mode aims to check the behaviour of the whole EMCS chain, by using a known radiation source.

5.4.2.11 On-Ground Test Mode (RD 7, §7.3.11.)

The EMDH enters this mode of operation when the first phase of the Initialisation mode has been completed and the unit detects the presence of test connectors plugged in. This mode provides two sub-modes: 1) Low-Level On-Ground Test; 2) High-Level On-Ground Test.

When the transition from Initialisation to On-Ground Test takes place, the EMDH automatically enters in Low-Level On-Ground Test sub-mode: in this sub-mode the EMDH is able to communicate with the external Test Equipment (T.E.) by means of the test interface. In this phase the EMDH can perform the following functions:

- S/W and data upload into RAM
- S/W and data dump
- Read & Write of I/O devices

Each single function is activated by proper T.E. Command received from the test I/F. The EMDH can exit this sub-mode in two ways:

- by entering the 2nd phase of the Initialisation mode, on the reception of a proper T.E. command;
- by performing a sub-mode transition to High-Level On-Ground test, on reception of a proper T.E. command from the test I/F.

When in High-Level On-Ground Test sub-mode, the EMDH performs the initialisation of S/W and the Operating System, as in the first phase of the Safe Stand-by mode. Once the initialisation has been performed, the EMDH:

- allows the activation/deactivation of tasks by executing proper TCs received from the RBI I/F;
- allows the execution of any kind of TC coming from the RBI I/F, without applying the restrictions used in the other operating modes.

When in High-Level On-Ground Test sub-mode, the EMDH can perform a mode transition to Safe Stand-by on reception of the relevant mode transition TC from RBI I/F.

5.4.2.12 Basic S/W Mode (RD 7, §7.3.12.)

The EMDH enters this mode of operation when:

- the Enter Basic S/W start task TC is received;
- a Start EMDH (with parameter) RBI command has been received.

When in this mode the EMDH does not execute high level S/W and it is only able to receive, decode and execute those TCs relevant to EMDH memory patching, dumping and checksum computation.

5.4.2.13 Relation to EMCS modes of operation (RD 7, §7.4)

EMCS Modes	EMDH Modes
Off	Off
Initialisation	Initialisation
Safe Stand-by	Safe Stand-by
Idle	Idle
Prime	Prime
Fast	Fast
Offset/Variance	Offset/Variance
CCD Diagnostic	CCD Diagnostic
Annealing	Extra-Heating - Annealing
Secondary Shroud De-Icing	Extra-Heating - De-Icing
CCD Decontamination	Extra-Heating - Decontamination
In-Flight Test	In-Flight Test/EMCS In-Flight Test/EMCR In-Flight Test/EMDH

5.5 EPIC MOS VOLTAGE CONVERTER (EMVC) (AD 7, §9.3.5.)

The EMVC has the capability to:

- receive unconditioned primary power (two lines: main and redundant) from EMDH;
- receive converter synchronisation signals (two lines: main and redundant) from EMDH;
- generate two temperature housekeeping data for each EMVC section for controlling its internal status;
- generate output voltage housekeeping;
- generate the necessary secondary power output for EMCR and EMAE.

5.6 EXPERIMENT FUNCTIONAL BLOCK DIAGRAM

In the following figure it is shown the functional block diagram of the whole EMCS:

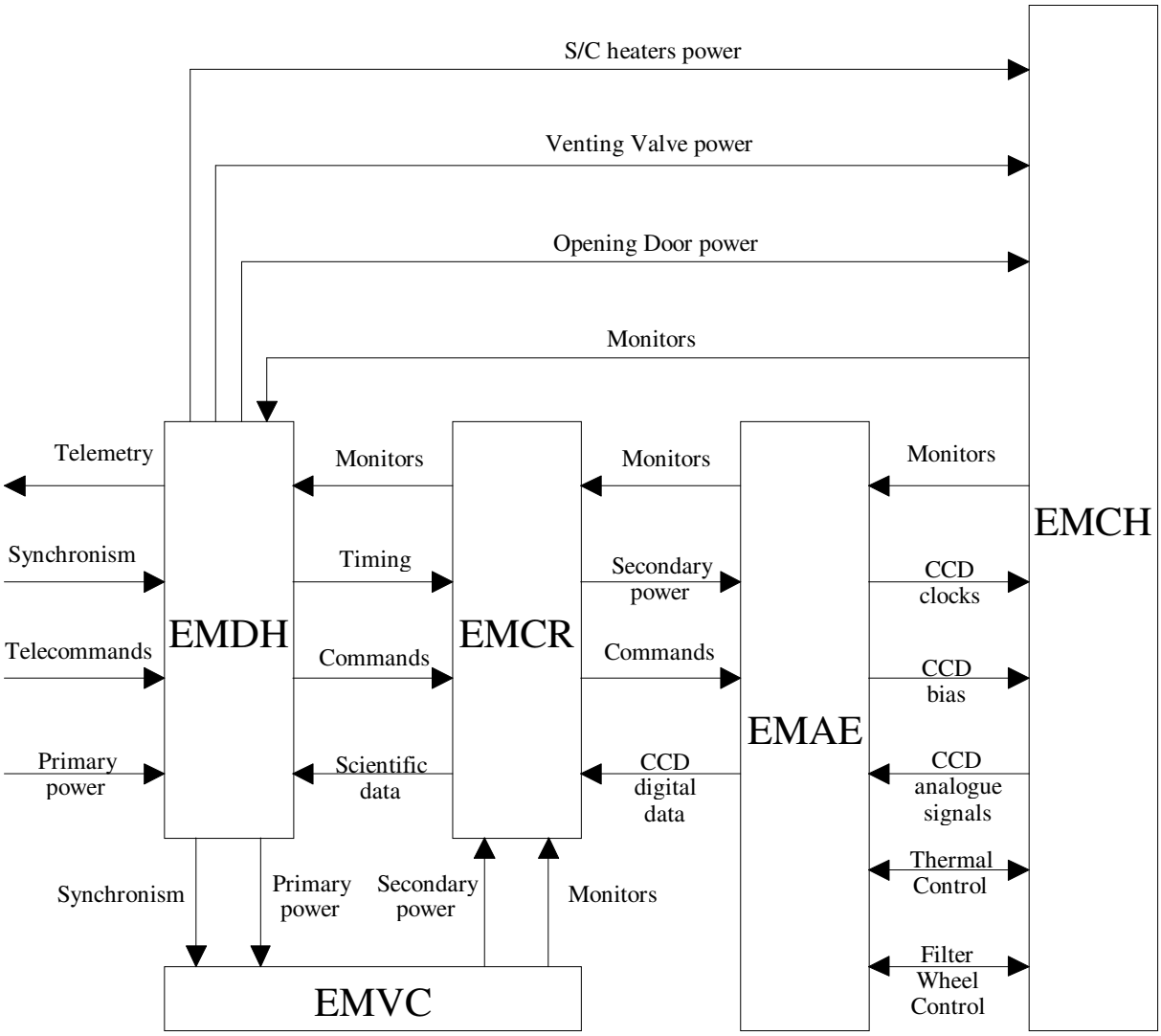


Figure 5.6-1: EMCS functional block diagram.

6. EXPERIMENT INTERFACES

6.1 EXTERNAL INTERFACES

6.1.1 Power Interfaces

6.1.1.1 Primary Power Interface

The EMCS receives primary power from the S/C: there are 2 circuits (nominal and redundant), with 2 lines each (nominal and redundant), for a total of 4 lines, both in input and in output. The power characteristics are:

- Minimum Voltage: + 26 V
- Nominal Voltage: + 28 V
- Maximum Voltage: + 30 V

Nominal and redundant I/Fs can not be energised at the same time.
Primary power is received by EMDH, which re-routes it to EMVC .

XMM Power lines

Nom. Primary Power Bus I/F	PPWR
Red. Primary Power Bus I/F	PPWR

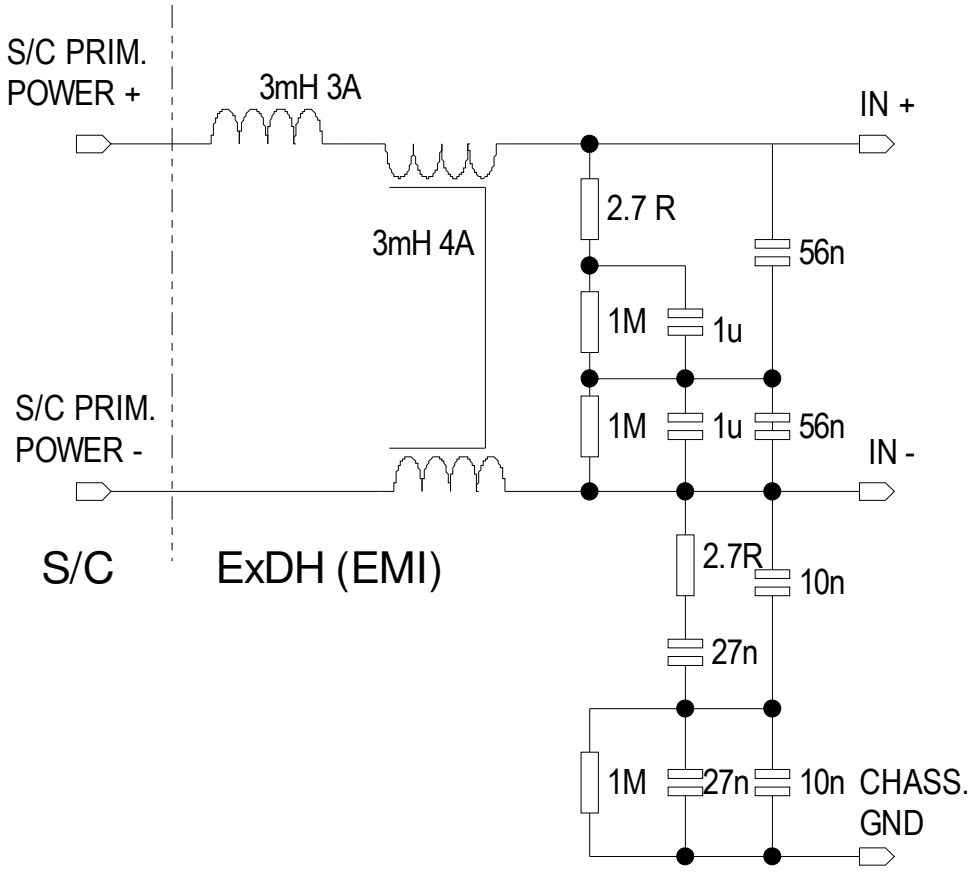


Figure 6.1.1.1-1: EMI Filter Electrical Diagram

6.1.1.2 Secondary Power Interface to DBU

The EMCS provides secondary power to the DBU of the OBDH System by means of 2 independent power lines (nominal and redundant) with the following characteristics:

- Minimum Voltage: + 5.7 V
- Nominal Voltage: + 6.0 V
- Maximum Voltage: + 6.3 V

The nominal secondary power line is active when primary power is applied to EMCS through the nominal primary power line; the redundant secondary power line is active when primary power is applied to EMCS through the redundant primary power line.

XMM DBU Power

Nom. DBU Sec. Power I/F	SPWR
Red. DBU Sec. Power I/F	SPWR

6.1.1.3 Stand-By Heater Power Interface

The EMCS has a nominal and a redundant interface (both in input and in output) for a CCD stand-by heater powered by the S/C. This heater is allocated in order to satisfy the temperature requirement for the CCDs during the Off mode. Nominal and redundant I/Fs can not be energized at the same time.
The EMDH receives the Heater Primary Power Bus from the S/C and distributes it to the EMCH

XMM Stand-By Heater Power

Nom. Stand-By Heater Power I/F	HPWR
Red. Stand-By Heater Power I/F	HPWR

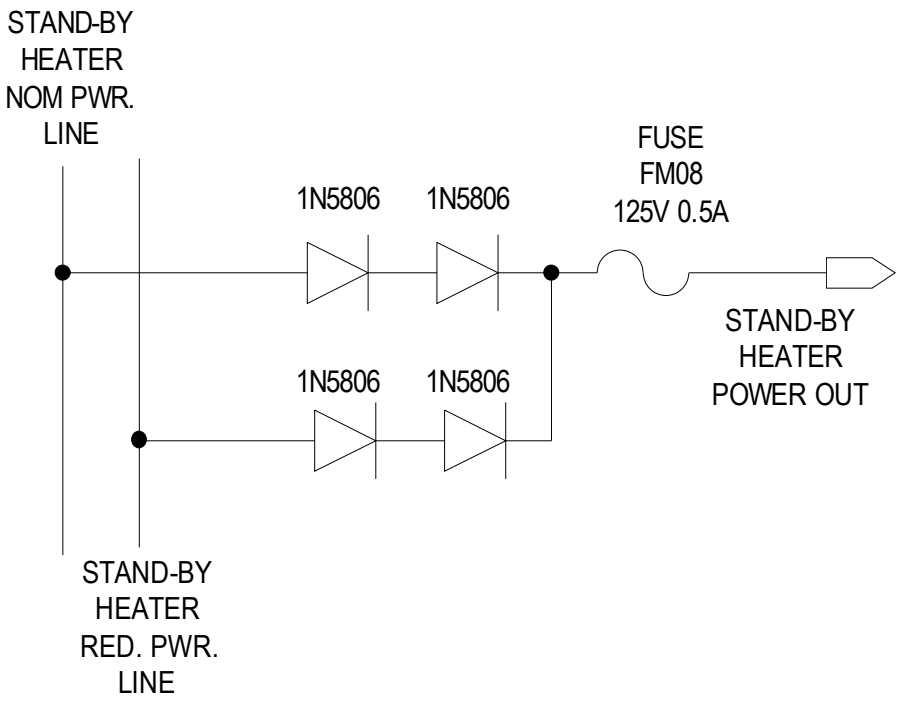


Figure 6.1.1.3-1: Stand-By Heater I/F

6.1.2 Converter Synchronisation Interfaces (AD 7, §3.9.1.2)

The EMCS has two converter synchronisation lines (one in input and one in output) for each primary power line, for a total of 4 lines. It receives the synchronisation signal with a frequency of 131.072 kHz ± 10 % and operates at this frequency or at half of it. In the absence of a clock signal, the EMCS converters are free running at a nominal frequency of 131.072 kHz ± 10 % or 65.536 kHz ± 10 %.
The Synchronisation Signal is received by EMDH, which delivers to EMVC and EMCH two signals of the same type (AD 8, §5.3).

XMM Power Converter Synchronisation lines

Nom. Power Supply Synch. I/F	PSYNCH
Red. Power Supply Synch. I/F	PSYNCH

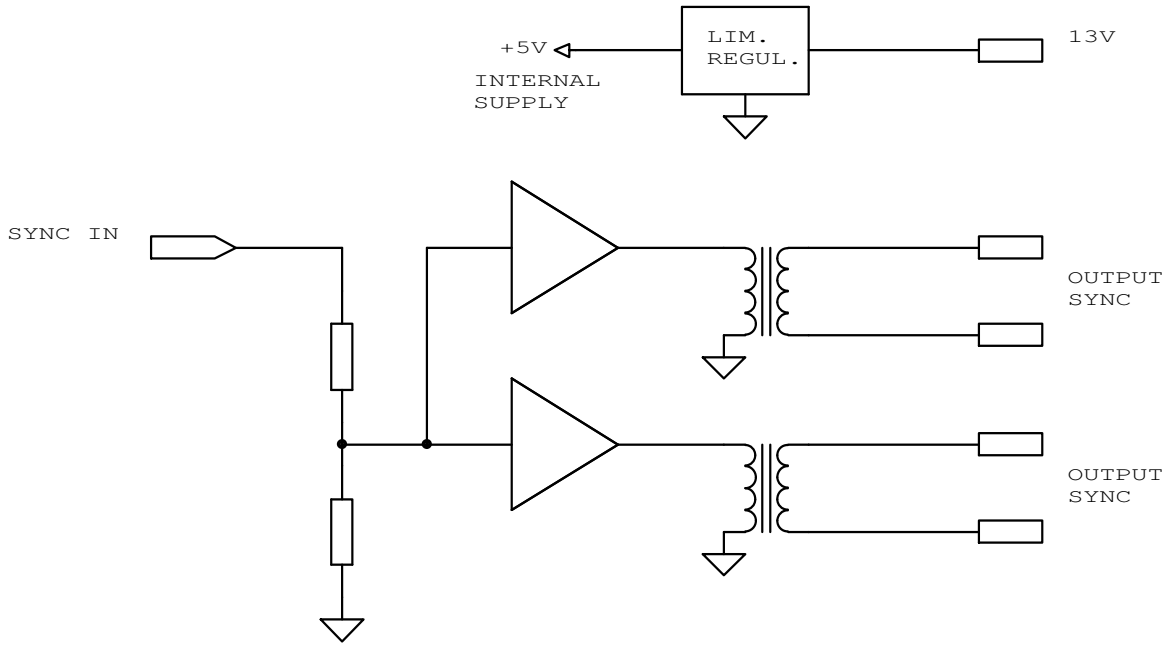


Figure 6.1.2-1: Power Synchronisation I/F Diagram

6.1.3 OBDH Bus Interface (AD 7, §3.9.2)

The EMCS has a redundant interface to the DBU of the OBDH Bus according to the DBI standard: this interface allows the telecommand transmission from the OBDH bus, through the DBU, to the EMDH unit and the telemetry packet transmission from the EMDH unit, through the DBU, to the OBDH bus. It provides an interface to both the Interrogation Bus and the Response Bus of the OBDH.

XMM DBU Signals

Nom. OBDH Interrogation Bus I/F	DBI
Nom. OBDH Response Bus I/F	DBI
Red. OBDH Interrogation Bus I/F	DBI
Red. OBDH Response Bus I/F	DBI

6.1.4 S/C Powered Temperature Sensor Interfaces (AD 7, §3.9.4)

The EMCS has an interface, with both an input and an output line, for each of the two thermistors which are conditioned by the S/C.

PRT Monitors

Primary Radiator PRT	PT500
Stand-By Heater PRT	PT500

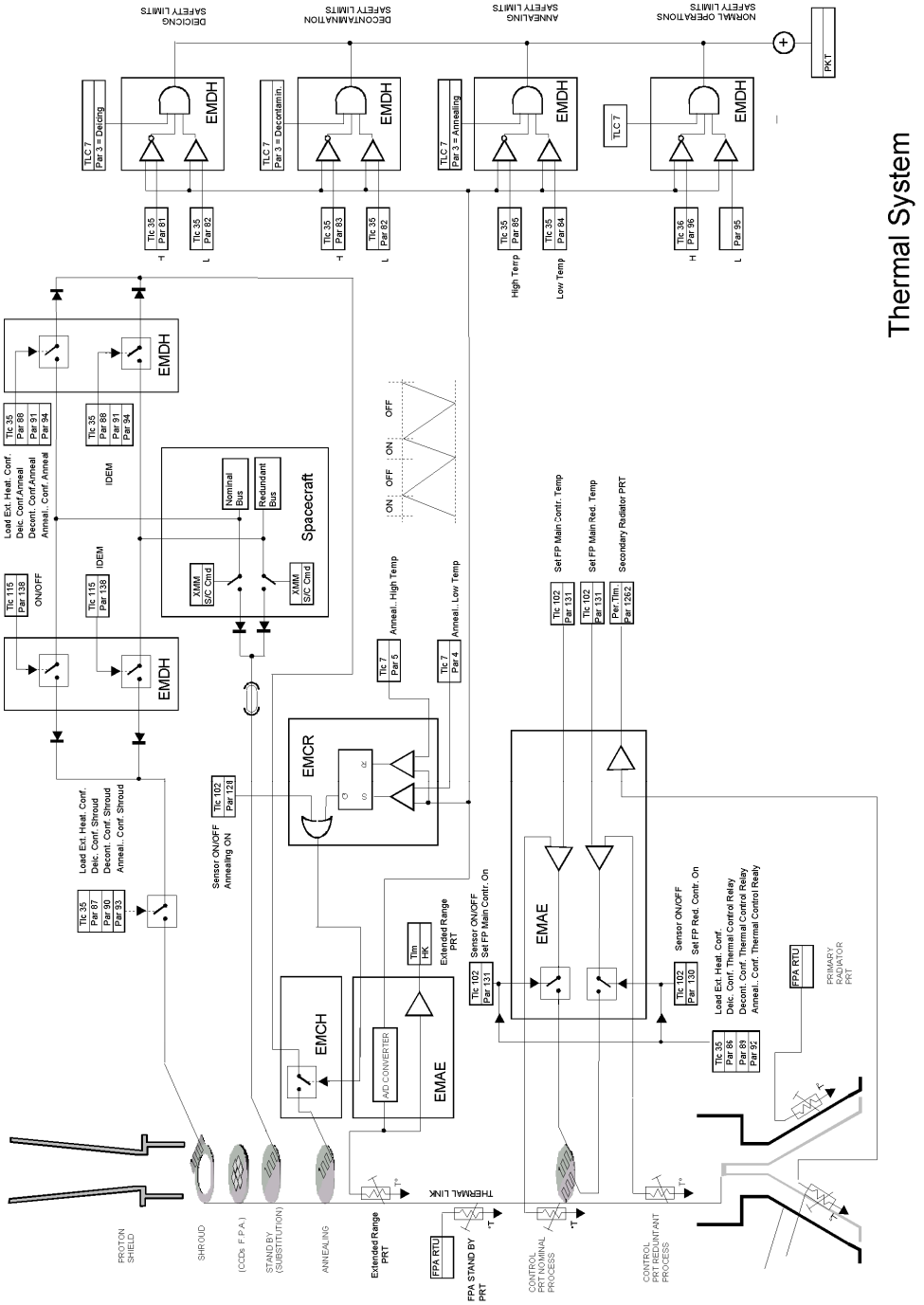


Figure 6.1.4-1: Thermal System Configuration

6.2 INTERNAL INTERFACES

6.2.1 Low Bit Rate I/F between EMDH and EMCR (LBR)

This I/F is used for communication between EMDH and EMCR units, with the exception of the scientific data routed through the HBR I/Fs. The LBR I/F (Nominal and Redundant) is a serial half duplex asynchronous I/F where EMDH is the master unit.
EMDH can send commands (with or without parameters) to the EMCR and depending on the command type it can answer only with an acknowledge or with an additional data block.
Using a dedicated command EMDH can send one or more lower level commands to the EMAE.

The following different types of commands are present:

- Commands without request of a Response Block

These commands generate one or more lower level actions in the EMCR, no request of H/K/Memory status is performed. Only acknowledge is sent back to EMDH.

- Commands with request of a Response Block

These commands are used to request H/K/Memory status from EMCR. Acknowledge and a Response Block are sent back to EMDH.

- Execution status command

This command is used to request the execution status of the last "Command without request of a Response Block" under execution or already executed.
Execution of a "Command with request of a Response Block" will be verified by EMDH waiting the expected or an anomaly Response Block until a suitable timout will expire.

Execution of every command (including lower level commands to EMAE) shall be verified as close as possible to the affected device/memory when new condition/status has been reached. Any available H/K, register, memory location, etc., will be used in order to verify the command execution.

No data block transmission, if not requested, is allowed from EMCR to EMDH.

A command transmission between EMDH and EMCR can be repeated three times in case of errors in the whole data handshake, after that an error indication will be flagged in the TLM format.

Every data packet (Command, Acknowledge and Response Block) exchanged between EMDH and EMCR shall have a 16-bit word multiple format.

EMDH will not send further command until acknowledge and response block, if requested, will be received from EMCR. Timeout shall be implemented to cope with communication problems.

EMCR will not accept any command (with exception of the Execution Status Command) if another command is waiting or under execution.
EMCR shall avoid endless loop and shall grant that execution of every command will take less than 6 seconds from reception.
Every command that will require more than 6 seconds for execution (e.g Turning and synchronization of the Filter Wheel) shall be managed by EMCR in such a way the "H/K Request" command can be accepted and executed.

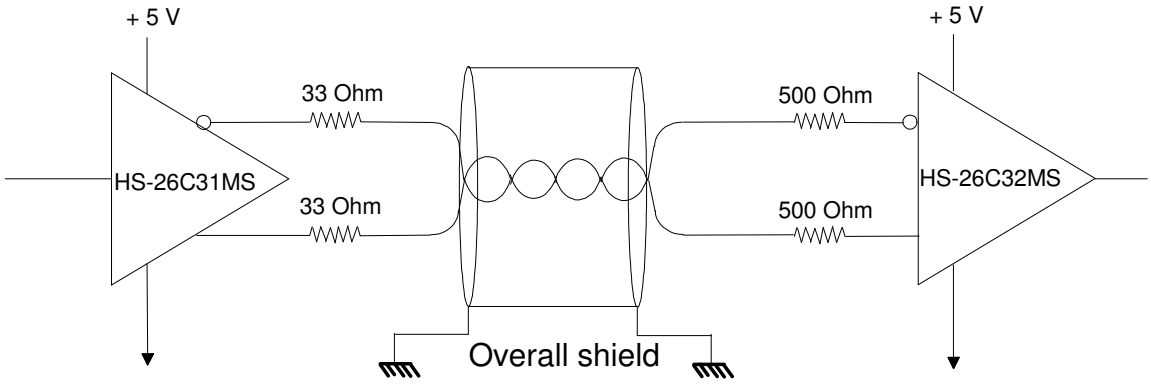
Correct execution or status of the last "Command without request of a Response Block" will be checked by request of execution status.

If a "Command with request of a Response Block" cannot be executed or fails during execution in the EMCR, an Anomaly Response Block is generated, as response, instead of the foreseen Response Block. The Anomaly Response Block will contain reason why the command execution is failed. Furthermore EMDH will provide a suitable timeout to avoid endless waiting loop in case EMCR is not able to transmit the foreseen or the anomaly Response Block.

In the following table the electrical characteristics of the Low Bit Rate I/F are specified:

DH/CR LOW BIT RATE I/F		
Parameter	**Source I/F**	**Receiver I/F**
Protocol	RS-422A	RS-422A
Part Names	HS-26C31MS	HS-26C32MS
Baud Rate	9600	9600
Character Length	8	8
Stop Bit	1	1
Parity Bit	None	None

Herafter the layout of the LBR I/F with shielding philosophy is indicated:



The command format used by EMDH to communicate with the EMCR is the following:

COMMAND FORMAT																	
	Bit	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Word	0	BEGIN IDENTIFIER								COMMAND CODE							
Word	1	COMMAND LENGTH															
Word	...	Parameter ...															
Word	...	Parameter ...															
Word	n-1	Parameter ...															
Word	n	CHECKSUM															

Notes:
Following ESA standard Bit 0 is the most significant bit.
Bit 0 of Word 0 is the first bit transmitted.

BEGIN IDENTIFIER field value is FF Hex and it is used for synchronization purpose in the EMCR.

COMMAND CODE field value identifies the command type and it can assume every value except FF. However FD Hex code is reserved to indicate the Execution status command.

COMMAND LENGTH field value indicates the total number of words included in the command and it is used in the EMCR for integrity test of the received command.

Parameters fields, if present, contain 16-bit data words to be delivered to EMCR unit.

CHECKSUM field value is the result of 16 vertical parity checks over the complete command block.

The Acknowledge (ACK) and Negative Acknowledge (NACK) formats delivered from EMCR to the EMDH are the following:

ACKNOWLEDGE FORMAT																	
	Bit	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Word	0	ACKNOWLEDGE								COMMAND CODE ECHO							

Notes:
Following ESA standard Bit 0 is the most significant bit.
Bit 0 of Word 0 is the first bit transmitted.

ACKNOWLEDGE field value is 11 Hex when it indicates the correct reception of the last command in the EMCR without request of Response block.

ACKNOWLEDGE field value is 22 Hex when it indicates the correct reception of the last command in the EMCR and a Response block has been requested.

ACKNOWLEDGE field value is 44 Hex when it indicates the correct reception of the Execution status command in the EMCR. After the acknowledge an additional word (Execution Report) will be sent to the EMDH.

Hereafter the Execution Report layout:

EXECUTION REPORT																
	Bit	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Word	0	COMMAND CODE								EXECUTION STATUS							

COMMAND CODE field value indicates the last "Command without request of a Response Block" sent to the EMCR.

EXECUTION STATUS field value indicates the execution status of the last "Command without request of a Response Block" sent to the EMCR. It can assume the following values:

- 11 Hex Command waiting for execution
- 22 Hex Command under execution
- 33 Hex Command correctly executed
- 44 Hex Command not executed due to boot program active
- 55 Hex Command not executed due to main program active
- 66 Hex Command not executed due to command code not foreseen
- 77 Hex Command not executed due to CTR current operating mode
- 88 Hex Command not executed due to parameters out of limits
- 99 Hex Command not correctly executed due to wrong verification

COMMAND CODE ECHO field includes the command code related to the acknowledge.

NEGATIVE ACKNOWLEDGE FORMAT																
	Bit	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Word	0	NEGATIVE ACKNOWLEDGE								ERROR CODE							

Notes:
Following ESA standard Bit 0 is the most significant bit.
Bit 0 of Word 0 is the first bit transmitted.

NEGATIVE ACKNOWLEDGE field value is 33 Hex and it indicates the last command was not correctly received in the EMCR or the received command is correct but it cannot be executed being another command under execution.

ERROR CODE field value indicates the reason for command rejection by EMCR. It can assume the following values:

- 11 Hex Received command rejected due to wrong checksum
- 22 Hex Received command rejected due to length overflow
- 33 Hex Received command rejected due to timeout expired during reception
- 44 Hex Received command rejected due to another command under execution

The response block format delivered from EMCR to the EMDH is the following:

RESPONSE BLOCK FORMAT																	
	Bit	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Word	0	BEGIN IDENTIFIER								RESPONSE BLOCK CODE							
Word	1	RESPONSE BLOCK LENGTH															
Word	2	Response Data ...															
Word	...	Response Data ...															
Word	n-1	Response Data ...															
Word	n	CHECKSUM															

Notes:
Following ESA standard Bit 0 is the most significant bit.
Bit 0 of Word 0 is the first bit transmitted.

BEGIN IDENTIFIER field value is FF Hex and it is used for synchronization purpose in the EMDH.

RESPONSE BLOCK CODE field value identifies the response block type (the same value of the command code used to request the involved response block) and it can assume every value except FF Hex. However 00 Hex code is reserved to indicate the Anomaly Response Block Format hereafter detailed.

The anomaly response block format delivered from EMCR to the EMDH is the following:

ANOMALY RESPONSE BLOCK FORMAT																	
	Bit	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Word	0	BEGIN IDENTIFIER								00 Hex							
Word	1	04 Hex															
Word	2	COMMAND CODE								ERROR CODE							
Word	3	CHECKSUM															

Notes:
Following ESA standard Bit 0 is the most significant bit.
Bit 0 of Word 0 is the first bit transmitted.

BEGIN IDENTIFIER field value is FF Hex and it is used for synchronization purpose in the EMDH.

COMMAND CODE field value identifies the "Command with request of a Response Block" failed during execution that has caused the anomaly response block generation.

ERROR CODE field value indicates the reason for command execution failure by EMCR. It can assume the following values:
- 44 Hex Command not executed due to boot program active
- 66 Hex Command not executed due to command code not foreseen
- 77 Hex Command not executed due to CTR current operating mode
- 88 Hex Command not executed due to parameters out of limits

RESPONSE BLOCK LENGTH field value indicates the total number of words included in the response block and it is used in the EMDH for integrity test of the received block.

Response Data fields contain 16-bit data words to be delivered to EMDH unit.

CHECKSUM field value is the result of 16 vertical parity checks over the complete response block.

Hereafter the flow diagrams of the EMDH - EMCR high level communication protocol are shown for commands with and without request of a Response Block:

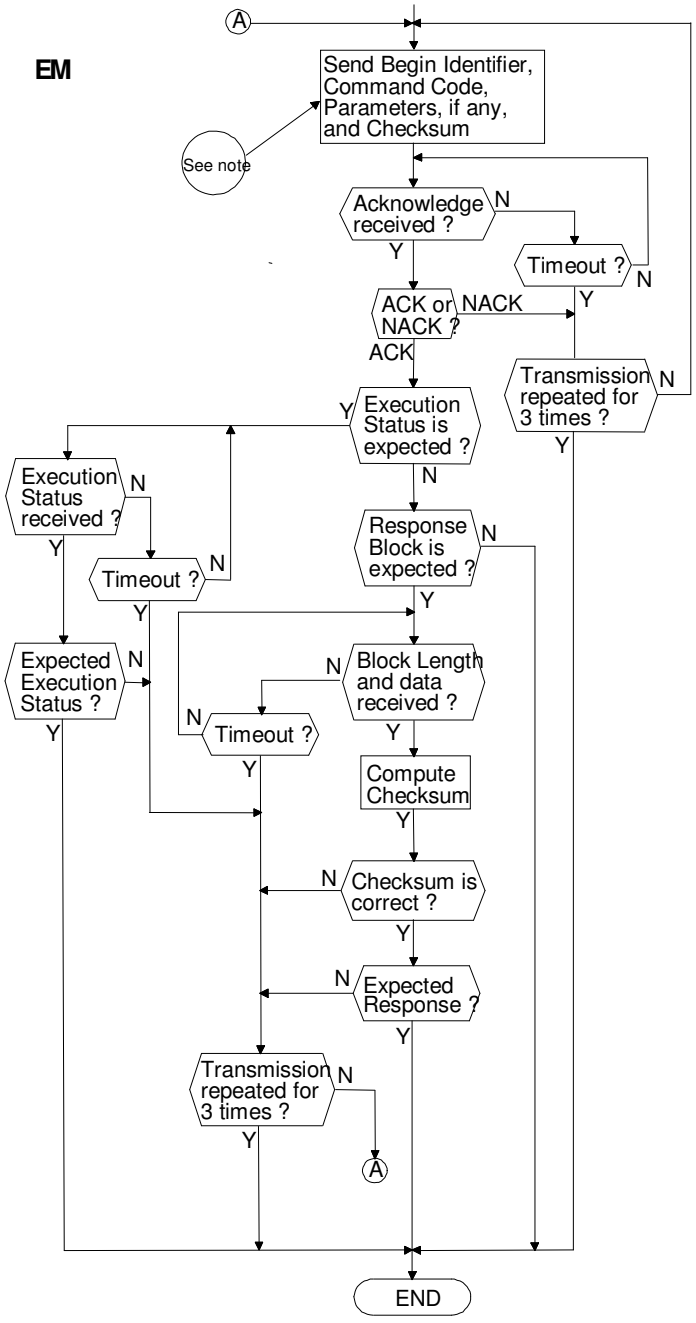


FIGURE 6.2.1-1: EMDH MANAGEMENT FLOW OF CMDs

Note: In case a negative acknowledge is received during command transmission, EMDH will immediately interrupt sending of data to EMCR and it will manage the NACK as received at the end of the command transmission

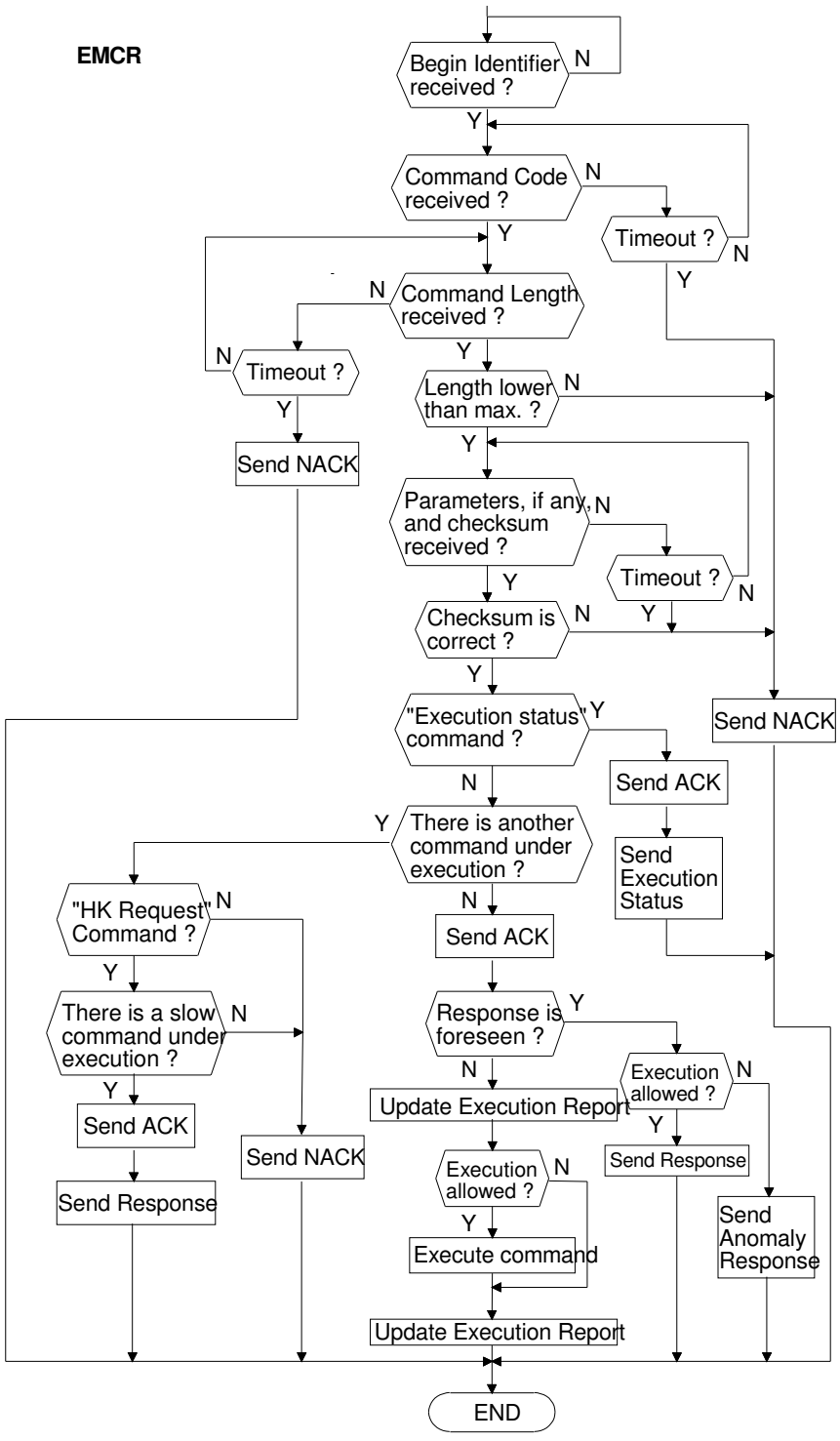
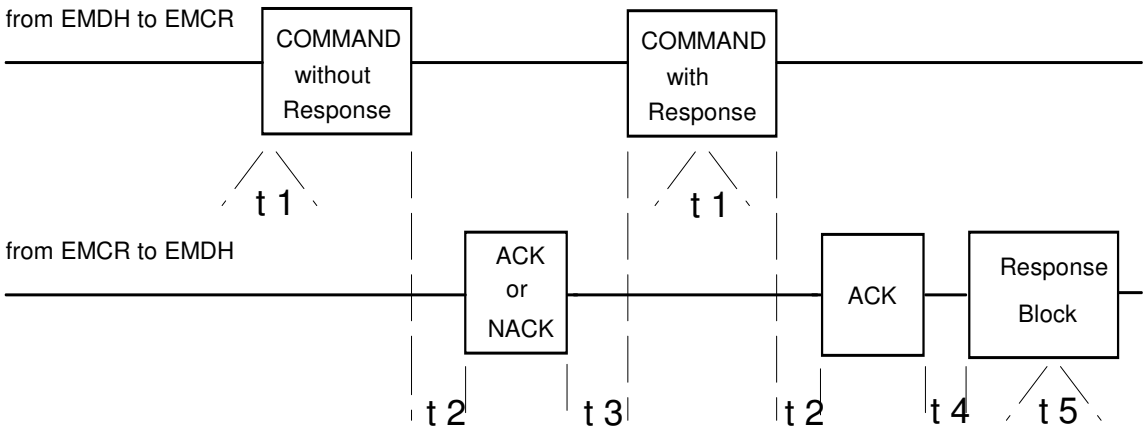


FIGURE 6.2.1-2: EMCR MANAGEMENT FLOW OF CMDs

Hereafter the high level timing protocol is shown:



Id.	Min Time	Max Time	Description
t 1	100 µs	100 ms	Delay between end of transmission of a 8-bit data and start transmission of the next one included in the same Command format
t 2	200 µs	80 ms	Delay from end of Command reception and ACK or NACK transmission.
t 3	100 µs	N/A	Delay from end of ACK or NACK transmission and next Command transmission
t 4	200 µs	6 s	Delay between end of ACK transmission and start of Response block transmission
t 5	100 µs	100 ms	Delay between end of transmission of a 8-bit data and start transmission of the next one included in the same Response block format

6.2.2 Low Bit Rate I/F between EMAE and EMCR (A-C_LBR)

This I/F is used for communication between EMAE and EMCR units, with the exception of the scientific data routed through the SDD I/Fs.
This interface is devoted to send commands to the EMAE and to receive data from it.

The LBR AE/CR I/F (Nominal and Redundant) is a serial half duplex synchronous I/F, where EMCR is the master unit.

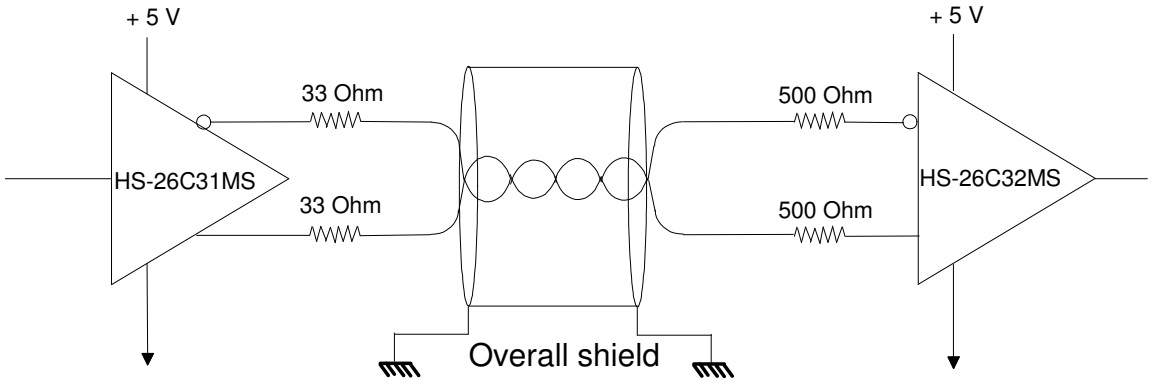
Each interface is constituted by four differential twisted lines:

- Clock: driven by EMCR (active on rising edge and only when transmission is in progress)
- Data Receive: driven by EMAE
- Data Transmit: driven by EMCR
- Transfer: driven by EMCR

The AE/CR I/F shall have the following electrical characteristics:

AE/CR LOW BIT RATE I/F		
Parameter	**Source I/F**	**Receiver I/F**
Protocol	RS-422A	RS-422A
Part Names	HS-26C31MS	HS-26C32MS
Clock Frequency	20 kHz ±2 kHz	20 kHz ±2 kHz
Character Length	16	16

Herafter the layout of the LBR I/F with shielding philosophy is indicated:



As far as the data protocol and I/F timing is concerned, they are specified in RD02 and RD03.

6.2.3 High Bit Rate I/F (HBR)

This kind of I/F is used for scientific data transferring from the EMCR unit to the EMDH unit.

The HBR I/F is a synchronous serial unidirectional I/F where EMCR is the transmitter unit.

The scientific data transfer is performed by means of 8 identical HBR I/F channels.

Each HBR interface consists of four differential twisted lines:

- Clock (active on rising edge);
- Sample;
- Data;
- End Of Frame Pulse

Each HBR I/F can work in three different transmission modes:

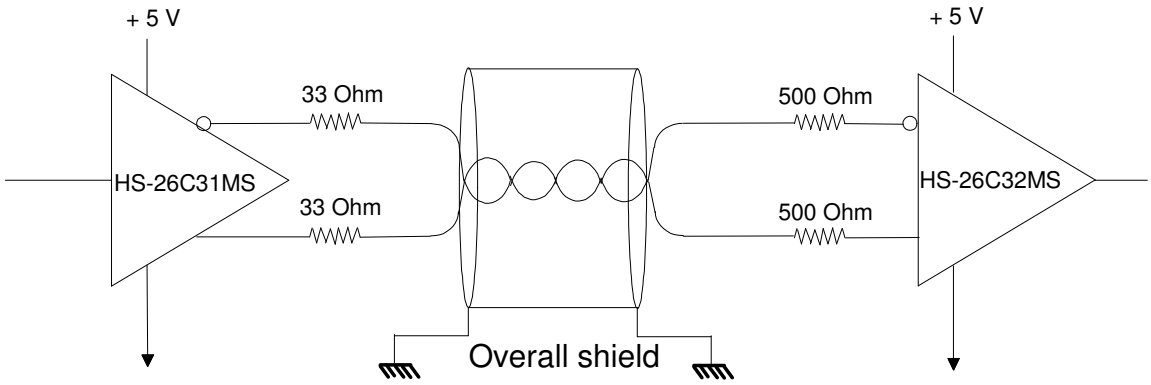
- Imaging/Threshold Mode
- Timing Mode
- Transparent Mode

6.2.3.1 Electrical Characteristics

In the following table the electrical characteristics of the High Bit Rate I/F are specified:

HIGH BIT RATE I/F		
Parameter	**Source I/F**	**Receiver I/F**
Protocol	RS-422A	RS-422A
Part Names	HS-26C31MS	HS-26C32MS
Clock Frequency	Either 500 KHz or 5 MHz (selectable)	Either 500 KHz or 5 MHz (selectable)
Max. Bit Rate	See AD 02	See AD 02
Character Length	16	16

Herafter the layout of the HBR I/F with shielding philosophy is indicated:



6.2.3.2 HBR Data Sequences & Timings

Here below the data transmission sequences and the timing diagrams of the HBR I/F for the different transmission modes are shown:

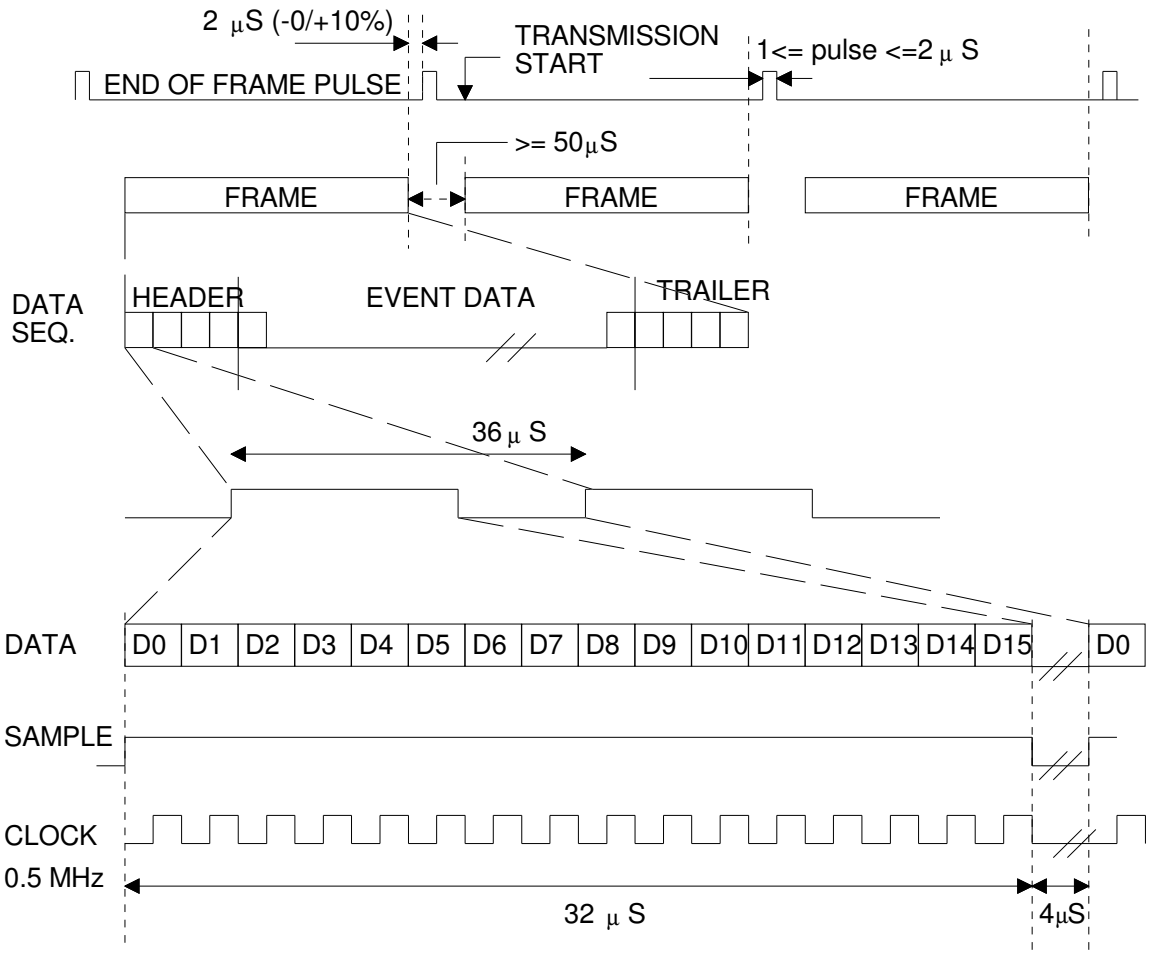
Imaging/Threshold Channel Mode Timings

For each frame, on the data line, there shall be the following data sequence:

I-HEADER
I-EVENT 1
I-EVENT 2
.....
I-EVENT N
I-TRAILER

A frame is defined as the interval between two consecutive pulses of the Frame Line of the HBR channel (except the first frame due to the fact that pulse on the Frame Line is generated only after the first frame transmission).
The maximum number of events in a frame (or in a second) is defined in AD 02.
The following timing diagram shall be considered at the EMCR ouput.
Clock, sample, data and EOF (except the pulse after frame transmission) lines are low (true output low, inverted output high) when there is no data transmission.
Taking into account EMCR will change data on the falling edge of the clock, EMDH shall sample data on the following rising edge of the clock. Falling edge of the sample shall be used by EMDH to store the last 16 bits sampled.

Note that the last Trailer will not be generated at the end of the last frame, but immediately after EMCR has received the Stop Observation command.



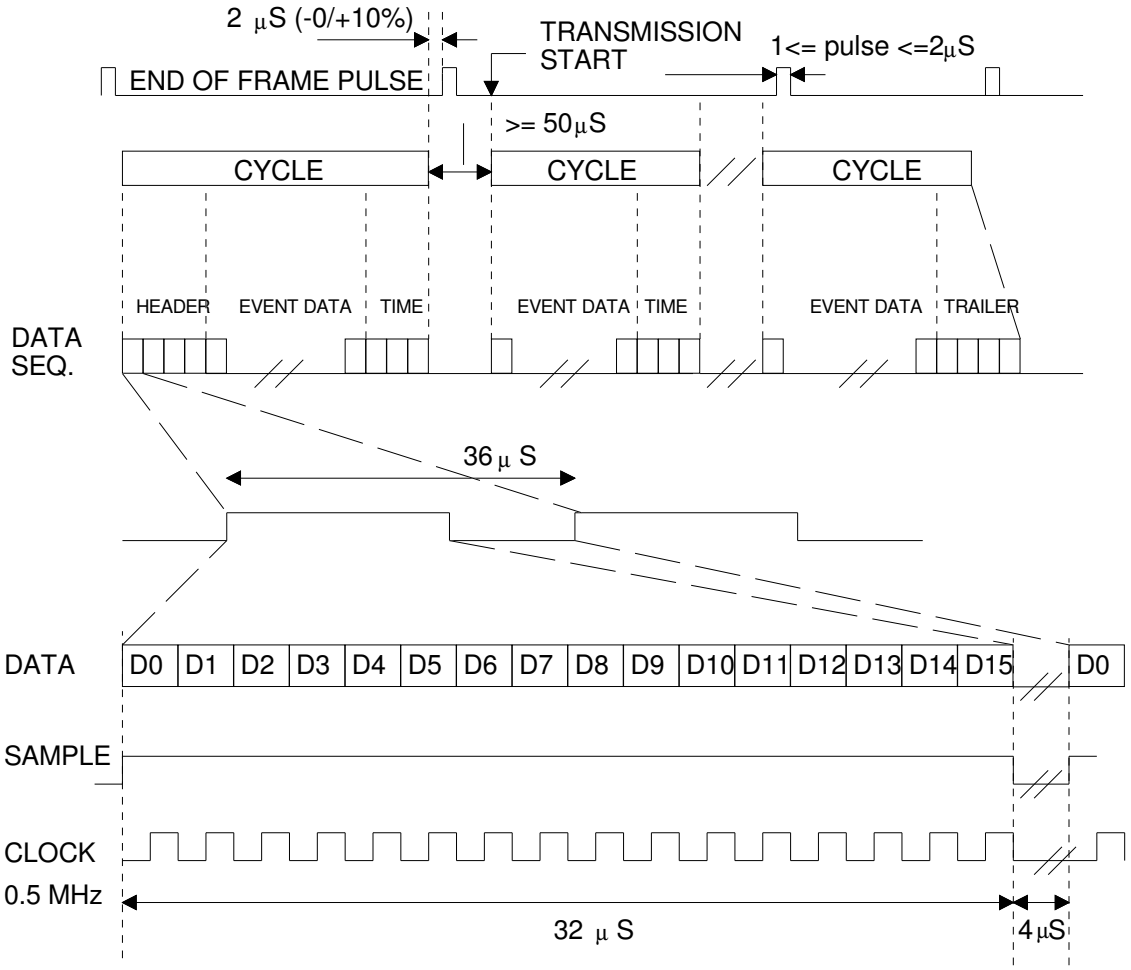
Timing Channel Mode Timings

For the entire exposure period, on the data line, there shall be the following data sequence:

EXPOSURE PERIOD	First Cycle	T-HEADER
		T-EVENT 1
		T-EVENT 2
		.....
		T-EVENT N1
		TIME INFO
	Cycles	T-EVENT 1
		T-EVENT 2
		.....
		TIME INFO
	Last Cycle	T-EVENT 1
		.....
		T-EVENT Nlast
		T-TRAILER

The observation period will be divided in cycles (as shown above).

A cycle is defined as the interval between two consecutive pulses of the Frame Line of the HBR channel (except the first cycle due to the fact that pulse on the Frame Line is generated only after the first frame transmission).
A cycle is also defined as the interval in which 1024 binned rows are readout.
The maximum number of events in a cycle (or in a frame) is defined in AD 02.
The following timing diagram shall be considered at the EMCR ouput.
Clock, sample, data and EOF (except the pulse after frame transmission) lines are low (true output low, inverted output high) when there is no data transmission.
Taking into account EMCR will change data on the falling edge of the clock, EMDH shall sample data on the following rising edge of the clock. Falling edge of the sample shall be used by EMDH to store the last 16 bits sampled.
Note that the Trailer will not be generated at the end of the last cycle, but immediately after EMCR has received the Stop Observation command.



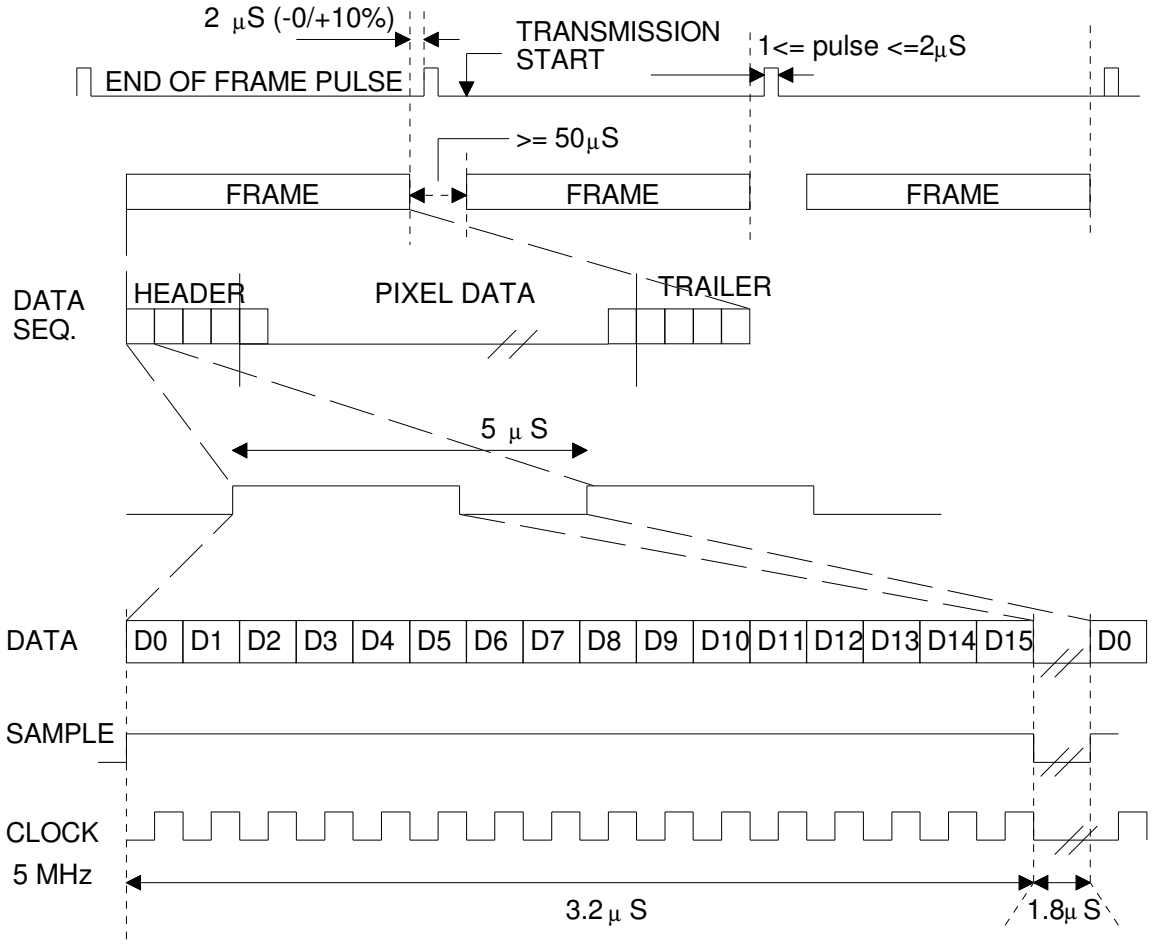
Transparent Channel Mode Timings

For the entire exposure period, on the data line, there shall be the following data sequence:

TR-HEADER
PIXEL 1
PIXEL 2
.....
PIXEL n (367220 for FF & Timing)
TR-TRAILER

A frame is defined as the interval between two consecutive pulses of the Frame Line of the HBR channel (except the first frame due to the fact that pulse on the Frame Line is generated only after the first frame transmission).
The number of pixels in a frame is fixed depending on the window selected (367220 in case the Imaging full frame or the Timing mode is selected).

The following timing diagram shall be considered at the EMCR ouput.
Clock, sample, data and EOF (except the pulse after frame transmission) lines are low (true output low, inverted output high) when there is no data transmission.
Taking into account EMCR will change data on the falling edge of the clock, EMDH shall sample data on the following rising edge of the clock. Falling edge of the sample shall be used by EMDH to store the last 16 bits sampled.



6.2.3.3 Formats of Data Exchanged on HBR Channel

Fields Description

Here below the description of the fields contained in the data structure is given:

Format Identifier: This 2-bits field identifies which kind of data structure will follow:

Format ID.	Format Type
00	Time Info
01	Scientific Data
10	Header
11	Trailer

Gatti Flag: This 1-bit field indicates when the Gatti number used for the DNL correction is set to 0 (starting of the ramp).

Gatti Flag	Gatti Number
0	Different from 0
1	Equal to 0

In Timing mode content of this field is meaningless.

CCD Identifier: This 3-bits field identifies which CCD the data belong to.

CCD Ident.	Active CCD
000	N/A
001	1
010	2
011	3
100	4
101	5
110	6
111	7

CCD Node: This 1-bit field identifies from which read-out node of the CCD the data are read-out.

CCD Node	Active Node
0	0 (Nominal)
1	1 (Redundant)

EDU Threshold: This 12-bits field indicates the current threshold value used by the EDU (range 0÷4095).

EDU Mode: This 2-bits field indicates which is the current operating mode of the EDU:

EDU Mode	Active EDU Mode
00	Transparent
11	Imaging
01	Timing
10	Threshold

EDU ID. This 3-bits field indicates the EDU that has managed the involved HBR channel data (range 0÷7).

Frame/Cycle Number: This 4-bits field reflects the position of a modulo 16 counter incremented after each frame or pseudo-frame transmission (range 0 ÷15). The counter assumes a random value after each EMCR Start Observation.

Window X0-Position: This 10-bits field indicates the X-coordinate of the bottom corner of the current selected read-out window close to the selected output node (range 0÷609).
Note that this value shall be correctly set together with Window ΔX field in order to stay inside the real CCD X dimension of 610 pixels

Window Y0-Position: This 10-bits field indicates the Y-coordinate of the bottom corner of the current selected read-out window close to the selected output node (range 0÷601).
Note that this value shall be correctly set together with Window ΔY field in order to stay inside the real CCD Y dimension of 602 pixels

Window ΔX: This 10-bits field indicates the size, along the X axis and starting from the Window X0-Position, of the current selected read-out window (range 0÷610).
Note that this value shall be correctly set together with Window X0-Position field in order to stay inside the real CCD X dimension of 610 pixels

Window ΔY: This 10-bits field indicates the size, along the Y axis and starting from the Window Y0-Position, of the current selected read-out window (range 0÷602).
Note that this value shall be correctly set together with Window Y0-Position field in order to stay inside the real CCD Y dimension of 602 pixels

Integration Time: This 10-bits field indicates, with a resolution of 100 ms, the integration time of the frame (range 0÷1023).
If the integration time is set to 0, it means the CCD is readout in free running mode (the integration time is EMAE sequence dependent).

Peripheral Pixels Above Threshold Counter: This 3-bits field indicates the number of pixels, belonging to the peripheral ring of the 5x5 matrix, whose energy is above the EDU threshold (range 0÷7).

Event X Position: This 10-bits field indicates the position of the pattern far-top corner (along the X axis and starting from the first pixel read from the selected node) from the selected output node (range 0÷1023). Note that it is expected to find position values inside the real CCD X dimension of 610 pixels

Event Y Position: This 10-bits field indicates the position of the pattern far-top corner (along the Y axis and starting from the first pixel read from the selected node), from the selected output node (range 0÷1023). For the T-Event the Y position indicates the time coordinate of the top-line of the event (range 0÷1023). Note that it is expected to find position values inside the real CCD Y dimension of 602 pixels

Pattern Number: This 5-bits field indicates the pattern type of the recognized event. For I-Event the range is 0÷31, for T-Event the range is 0÷4, for TH-Event pattern number will indicate always a pattern with only the central pixel valid.
The pattern identifier shall be related with the Pattern & Mask Table loaded in the involved EDU.

Event Energy (E1): This 12-bits field indicates the energy of the central pixel of the event (range 0÷4095).

Event Energy (E2): For I-Event this 15-bits field indicates the sum of the energy of the pixels, except the central one, above EDU threshold in the 3x3 matrix (range 0 ÷ 32767), for T-Event this 15-bits field indicates the energy of the pixel that lie beside the brightest pixel (range 0 ÷ 32767).

Event Energy (E3): For I-Event this 15-bits field indicates the signed sum energy of the pixels below EDU threshold in the 3x3 matrix (range -16384 ÷ +16383).

Event Energy (E4): For I-Event this 15-bits field indicates the sum of the energy of the peripehral pixels in the 5x5 matrix (range -16384 ÷ 16383).

FIFO OVF: This 1-bit field indicates when a FIFO overflow as occured during the frame (or pseudo-frame). This flag, when set, indicates that some events in the frame (or pseudo frame) are lost. However the transmitted events are correct.

FIFO OVF	FIFO Overflow
0	Not occured
1	Occured

Pixel Count: This 20-bits field indicates the total number of pixels above threshold belonging to the frame.

Coarse Time: For I-Trailer, TR-Trailer and TH-Trailer this 15-bits field indicates the time (expressed in seconds) at which the integration time finished (range 0 ÷ 32767).
For Time Info and T-Trailer this field indicates the time at which the format is transmitted.

Fine Time: For I-Trailer, TR-Trailer and TH-Trailer this 15-bits field indicates the time, expressed in fraction of second (resolution of 40 μs), at which the integration time finished (range 0 ÷ 32767).
For Time Info and T-Trailer this field indicates the time at which the format is transmitted.

Cycle Number: This 4-bits field indicates the ordinal number of the cycle (range 0 ÷ 15). The counter assumes a random value at EMCR power-on.

Pixel Energy: This 12-bits field indicates the raw energy of the pixel (range 0÷4095).

EOL: This 1-bit field indicates if the transmitted pixel is the last of a line.

EOL	Pixel Number
0	Not last of a line
1	Last pixel of a line

Imaging Transmission Mode Data Formats

I-HEADER

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
MSB															LSB

1	Format ID. 10	Gatti Flag	CCD ID.	CCD Node	EDU Mode	EDU THRES. MSBits	Frame Number
0	EDU Threshold		Window X0-Position				
0	EDU Threshold LSBits		Window Y0-Position				
0	INTEGRAT. TIME MSBits		Window ΔX				
0	INTEGRAT. TIME LSBits		Window ΔY				

I-EVENT

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
MSB															LSB

1	Format ID. 01		Periph. Pixels Above Thresh. Counter		Event Y Position										
0	Event X Position										Pattern Number				
0	0				Event Energy (E1)										
0	Event Energy (E2)														
0	Event Energy (E3)														
0	Event Energy (E4)														

I-TRAILER

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
MSB															LSB

1	Format ID. 11	0	EDU ID.	FIFO OVF	0		Frame Number
0	0					Pixel Count MSBits	
0	Pixel Count LSBits						
0	Coarse Time						
0	Fine Time						

Note: The Most Significant Bit (MSB) is always transmitted first.

Timing Transmission Mode Data Formats

T-HEADER

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
MSB															LSB

1	Format ID. 10	Gatti Flag	CCD ID.	CCD Node	EDU Mode	EDU THRES. MSBits	Frame Number
0	EDU Threshold		Window X0-Position				
0	EDU Threshold LSBits		Window Y0-Position				
0	INTEGRAT. TIME MSBits		Window ΔX				
0	INTEGRAT. TIME LSBits		Window ΔY				

T-EVENT

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
MSB															LSB

1	Format ID. 01	Periph. Pixels Above Thresh. Counter	Event Y Position		
0	Event X Position			Pattern Number	
0	0	Event Energy (E1)			
0	Event Energy (E2)				
0	Meaningless bits				
0	Meaningless bits				

TIME INFO

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
MSB															LSB

1	Format ID. 00	0	EDU ID.	FIFO OVF	0	Cycle (Pseudo Frame) Number
0	0				Pixel Count MSBits	
0	Pixel Count LSBits					
0	Coarse Time					
0	Fine Time					

T-TRAILER

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
MSB															LSB

1	Format ID. 11	0	EDU ID.	FIFO OVF	0	Cycle (Pseudo Frame) Number
0	0				Pixel Count MSbits	
0	Pixel Count LSBits					
0	Coarse Time					
0	Fine Time					

Note: The Most Significant Bit (MSB) is always transmitted first.

Transparent Transmission Mode Data Formats

TR-HEADER

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
MSB															LSB

1	Format ID. 10	Gatti Flag	CCD ID.		CCD Node	EDU Mode	EDU THRES. MSBits	Frame Number
0	EDU Threshold		Window X0-Position					
0	EDU Threshold LSBits		Window Y0-Position					
0	INTEGRAT. TIME MSBits		Window ΔX					
0	INTEGRAT. TIME LSBits		Window ΔY					

TR-EVENT

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
MSB															LSB

1	Format ID. 01	EOL	Pixel Energy

TR-TRAILER

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
MSB															LSB

1	Format ID. 11	0	EDU ID.	FIFO OVF	0	Frame Number
0	0				Pixel Count MSBits	
0	Pixel Count LSBits					
0	Coarse Time					
0	Fine Time					

Note: The Most Significant Bit (MSB) is always transmitted first.

Threshold Transmission Mode Data Formats

TH-HEADER

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
MSB															LSB

1	Format ID. 10	Gatti Flag	CCD ID.	CCD Node	EDU Mode	EDU THRES. MSBits	Frame Number
0	EDU Threshold		Window X0-Position				
0	EDU Threshold LSBits		Window Y0-Position				
0	INTEGRAT. TIME MSBits		Window ΔX				
0	INTEGRAT. TIME LSBits		Window ΔY				

TH-EVENT

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
MSB															LSB

1	Format ID. 01	Periph. Pixels Above Thresh. Counter	Event Y Position												
0	Event X Position										Pattern Number				
0	0		Event Energy (E1)												
0	Meaningless bits														
0	Meaningless bits														
0	Meaningless bits														

TH-TRAILER

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
MSB															LSB

1	Format ID. 11	0	EDU ID.	FIFO OVF	0		Frame Number
0	0					Pixel Count MSBits	
0	Pixel Count LSBits						
0	Coarse Time						
0	Fine Time						

Note: The Most Significant Bit (MSB) is always transmitted first.

6.2.4 Time Reference Clock Interface (TIM_CLK)

This I/F is used to allow the units downstream the EMDH to clock their internal timers.

The signals of this I/F shall be generarated by the EMDH and routed to the EMCR unit.
At the reception of this signal EMCR will reset its internal fine time counter and increment of one its internal course time counter.

The time reference clock interface shall consists of a nominal and redundant differential twisted lines. Time Reference line is normally set to low (true output low and inverted output high). Time Reference line will go high generating a pulse with a frequency of 1 Hz.

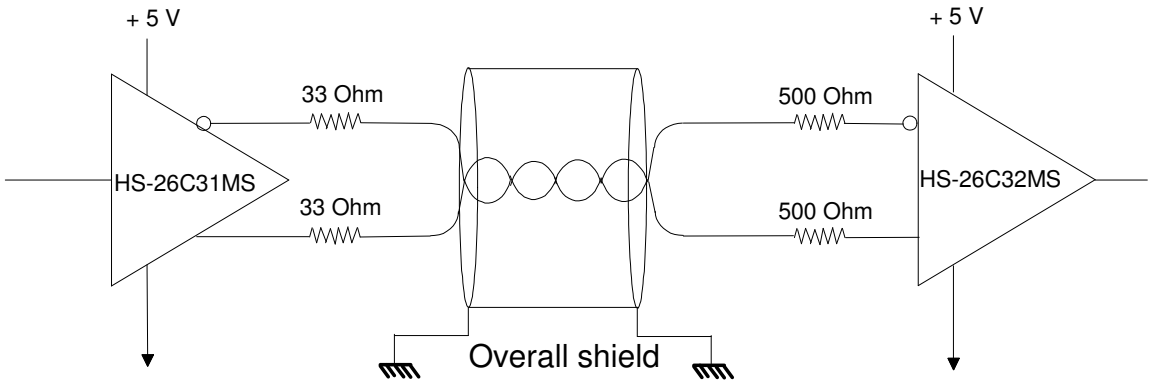
This signal shall be synchronized with the OBDH bus clock and shall be derived from OBDH BCP2 signal.

6.2.4.1 Electrical Characteristics

In the following table the electrical characteristics of the Time Reference Clock I/F are specified:

Time Reference Clock I/F		
Parameter	**Source I/F**	**Receiver I/F**
Protocol	RS-422A	RS-422A
Part Names	HS-26C31MS	HS-26C32MS
Pulse Frequency	1 Hz	1 Hz
Pulse Duration	1.9 µs	1.9 µs
Active edge	Rising	Rising

Herafter the layout of the Time Reference Clock I/F with shielding philosophy is indicated:



6.2.5 Time Reference Synchronization Interface (TIM_RST)

This I/F is used to allow the units downstream the EMDH to keep their internal time synchronized with the satellite time.

The signals of this I/F shall be generated by the EMDH and routed to the EMCR unit.
At the reception of this signal EMCR will reset its internal course time counter.

The time reference clock interface shall consists of a nominal and redundant differential twisted lines. Time Reference line is normally set to low (true output low and inverted output high). Time Reference line will go high generating a pulse before starting of every new exposure period, however at least every 9 hours (this time shall be selectable) when the exposure period is in progress.

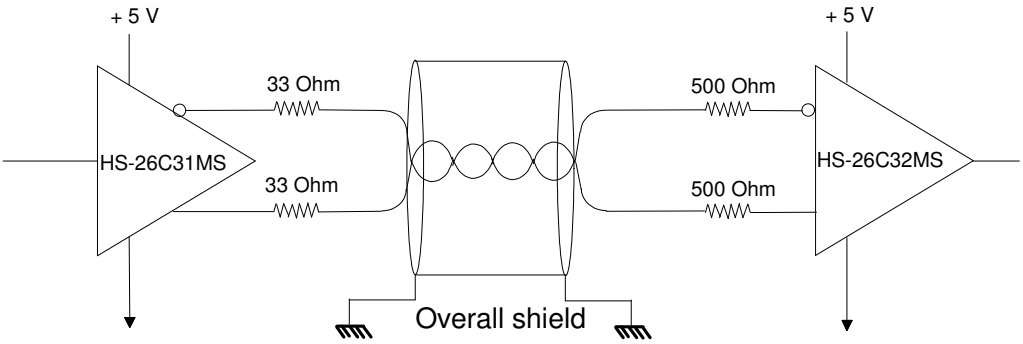
This signal shall be synchronized with the Time Reference Clock Signal and thus with OBDH bus clock.

6.2.5.1 Electrical Characteristics

In the following table the electrical characteristics of the Time Reference Synchronization I/F are specified:

Time Reference Synchronization I/F		
Parameter	**Source I/F**	**Receiver I/F**
Protocol	RS-422A	RS-422A
Part Names	HS-26C31MS	HS-26C32MS
Pulse Frequency	A pulse before starting a new exposure period, however at least every 9 hours when exposure is in progress	A pulse before starting a new exposure period, however at least every 9 hours when exposure is in progress
Pulse Duration	1.9 µs	1.9 µs
Active edge	Rising	Rising

Herafter the layout of the Time Reference Synchronization I/F with shielding philosophy is indicated:



6.2.6 Scientific Digital Data I/F (SDD)

This interface is used for scientific data transfer from the EMAE to the the EMCR.
The SDD I/F is a unidirectional synchronous serial high speed I/F where the EMAE is the master unit.

The scientific data transfer is performed by 8 identical SDD I/Fs.

Each SDD I/F consists of three differential twisted lines:

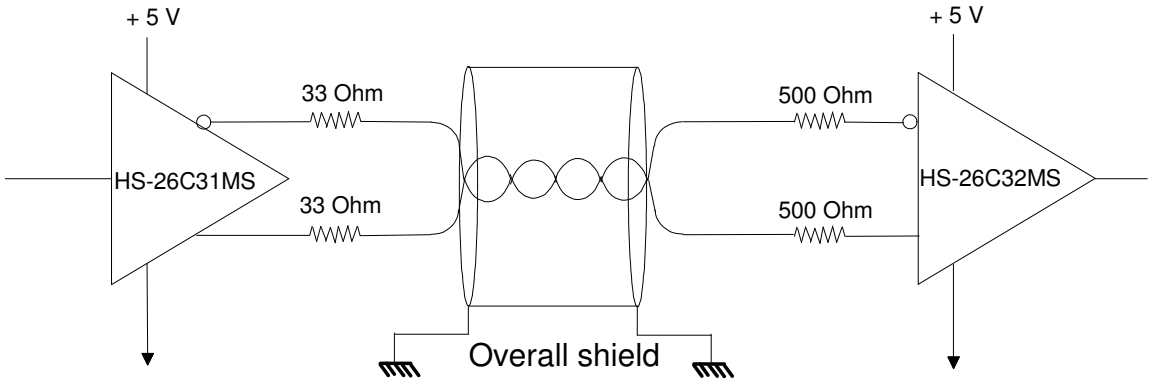
- Clock (active on rising edge);
- Sample;
- Data;

In the following table the electrical characteristics of the SDD I/F are specified:

SDD I/F		
Parameter	**Source I/F**	**Receiver I/F**
Protocol	RS-422A	RS-422A
Part Names	HS-26C31MS	HS-26C32MS
Clock Frequency *	4 MHz	4 MHz
Max. bit rate	3.2 Mbps	3.2 Mbps
Character Length	16	16

* = active on rising edge, active only during data transmission.

Herafter the layout of the SDD I/F with shielding philosophy is indicated:



The transmitted 16 bits data words shall have the following format

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
MSB															LSB
EOI	EOF	EOL	DATA INV.	Pixel Energy											

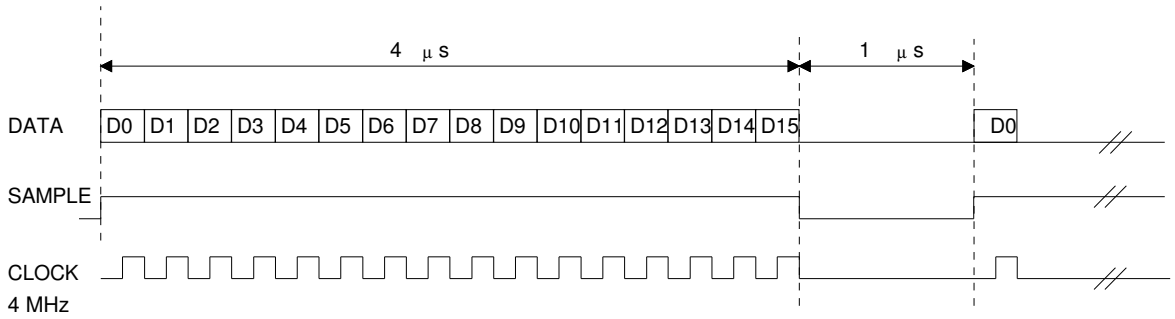
Fields description

EOI: End Of Integration.
EOF: End Of Frame
EOL: END Of Line
Pixel Energy: Converted Energy of the pixel

Synchronization bits ➲ *Meaning* ⓫	*EOI*	*EOF*	*EOL*	Data Invalid
First pixel of new frame is being transmitted	1	0	0	0*
Last Pixel of the line is being transmitted	0	0	1	0*
Last pixel of the frame is being transmitted	0	1	X	0*

* when Data Invalid flag is set the pixel energy value contained in the data word shall be discarded but the information provided by sysncronization bits (if set) shall be used.

Here below the timing diagram for the SDD I/F is presented.



6.2.7 DBI I/F (DBI)

This interface allows the telecommand transmission from the OBDH bus, through the DBU, to the EMDH Unit and the telemetry source packets transmission from the EMDH Unit, through the DBU, to the OBDH bus.

The EMCS shall provide a nominal and a redundant DBI I/F (via DBU) to:

the OBDH Interrogation Bus, and
- RIR_DATA
- RIR_VAL
- RIR_SYNC
- RIR_CLK

the OBDH Response Bus.
- RRT_DATA
- RRT_EN

6.3 DESCRIPTION OF ENGINEERING MODES (RD 12, §3.)

6.3.1 OFF Mode

In off mode, no primary power is supplied to EMCS and all the units are off.

In off mode, the filter wheel shall be in closed position, in order to protect the CCD's. (Provisions have been made so that the filter wheel is turned to the closed position before disconnecting the primary power: see nominal transition from safe stand-by mode to the off mode).
The off mode shall be characterised by the following conditions:

a) The Door Mechanism and the Venting Valve shall be in open position during SMP (in closed position during LEOP) under S/C control;
b) The Calibration Source Mechanism shall be in off position;
c) The S/C-controlled stand-by heaters shall be on;
d) The temperature is monitored by two thermistors (placed on focal plane and primary radiator) powered by S/C.

The S/C shall control the temperature of the CCD's. This temperature shall be kept in the range between –150 °C and 50 °C.

In case of emergency transition to the off mode, CDMS shall include the telecommand to turn the filter wheel to the closed position in the telecommand packet. (It must be noted that the filter wheel is already in the closed position in the safe stand-by mode).
If the transition to the off mode is done via Safe Stand-by Mode, the closing of the filter wheel is done automatically, provided that the sequence, for driving the filter wheel stepper motor was previously uploaded.

The transition OFF - INITIALISATION mode is under S/C control and it consists in applying primary power to the experiment.

6.3.2 INITIALISATION Mode

This mode of operation shall be entered from the off mode and when primary power is applied to EMCS only.
This mode of operation is not a steady state condition but transition between the Off Mode and the Safe Stand-by Mode.

Each EMCS unit shall initialise itself. At the end of each unit initialisation procedure, the master unit shall collect HK telemetry related to the initialisation results from the other units as well its internal data.

An HK telemetry packet containing all the initialisation data report shall be prepared by EMCS and put in the output queue for the transmission via TLM.

The status of all the HW devices shall not be changed from that of the off mode, during both SMP and LEOP (It must be noted that the difference between LEOP and SMP lies in the status of the Door Device which is in open status.).

EMCS shall activate the thermal control of the CCD's.

Focal plane temperature control by S/C will not be active.

At the end of all the previous operations, EMCS shall enter the safe stand-by mode by default, during both SMP and LEOP.

The transition INITIALIZATION - SAFE STAND-BY is automatic after all the EMCS units have finished their initialization. The following actions will be automatically performed (they are the same performed when a SAFE STAND-BY Mode Transition TLC is received):

- H/K telemetry will be activated
- Annealing heater, Secondary Shroud heater and HOPs heaters will be off
- CCDs thermal control will be activated with a default temperature of –100°C. (EMDH will pass this temperature value to EMCR)
- EMDH will monitor that focal plane temperature does not exceed a default temperature range (this range can be modified by "Load Thermal Monitoring Limits" TLC)
- the Filter Wheel will not be active since the relevant sequence, for stepper motor driving, is not automatically loaded in the EMAE sequencer.

6.3.3 SAFE STAND-BY Mode K1

This mode of operation shall be entered from the IDLE mode upon reception of the "Enter EMCS Safe Stand-by Mode" TLC. When the instrument is in any other mode, except OFF and INITIALIZATION, this transition can be performed, using the same TLC, only for emergency reasons. The following actions will be automatically performed:

- Interruption of Observation sending the "Stop Observation" command to EMCR, if EMCS was in one of the Observation modes;
- Interruption, in safe way, of any EMDH or EMCR test in progress, if EMCS was in IN-FLIGHT TEST mode with some EMDH or EMCR test active;
- Annealing heater, Secondary Shroud heater and HOPs heaters will be switched off;
- The CCDs thermal control will be operated with a default temperature of –100°C. (EMDH will send to EMCR a command with the default temperature setting value).
- The Filter Wheel will be activated as follows:
  - ♦ if the Filter Wheel is already in the closed position, there is no action
  - ♦ if the Filter Wheel is in open position, it is turned in the closed position
  - ♦ if the Filter Wheel is in one other position, it is turned in the closed position only when the focal plane temperature has cooled to less than + 60°C.

It is assumed that the Filter Wheel can turn only if the relevant stepper motor sequence has been previoulsy loaded.

The Heaters and HOPs controlled by EMDH will be off.

By default, the generation of all the HK telemetry packets is enabled: by telecommand, it is possible to enable/disable the generation of all or of specific telemetry packets.

During LEOP, it shall be possible to change the status of the door mechanism and the venting valve only in this mode of operation. Upon reception of appropriate telecommands, EMCS shall operate the door mechanism and the venting valve to the open position. Once these operations are performed, the transition to the SMP safe stand-by mode shall occur (see Sect. 3.6).

During SMP, it shall be possible to load, patch and dump SW to/from EMCS.

No TLCs from Ground are accepted, with the following exceptions:

- Enter EMDH S/W Maintenance K9
- Load EMDH Memory K11
- Exit EMDH S/W Maintenance K10

- Stop EMCR RAM Program K69
- Load EMCR Memory K70
- Start EMCR RAM Program K71

- Dump EMDH Memory K51

- Dump EMCR Memory K64

- Calculate EMCR Memory Checksum K65

- Calculate EMDH Memory Checksum K52

- Enter EMCS IDLE Mode K2

- Report TM Packet Generation Status K55

- Enable Generation All TM Packets K56
- Disable Generation All TM Packets K57
- Enable Generation Specific TM Packets K58
- Disable Generation Specific TM Packets K59

- Enable OBT Synchronisation K60
- Enable OBT Verification K62
- Add Time Code K61
- Preset Time Counter K63

Loading of the EMDH memory can be performed only entering the EMDH S/W Maintenance mode by “Enter EMDH S/W Maintenance” TLC. When EMDH is in this mode, H/K telemetry data are not available. EMDH returns to main SAFE STAND-BY mode by “Exit EMDH S/W Maintenance” TLC. Exit from EMDH S/W Maintenance causes a EMDH warm restart.

Loading of EMCR memory can be performed only entering the EMCR Boot Program mode by "Stop EMCR RAM Program" TLC. When EMCR is in this mode, EMCR/EMAE/EMCH H/K telemetry data are not available. EMCR exits this mode by "Start EMCR RAM Program" TLC, which causes EMCR to start the execution of S/W in RAM or by "Stop EMCR RAM Program" which causes EMCR to re-boot the S/W as a power-on.

EMCS shall exit this mode to enter either the off mode or the idle mode upon reception of OBDH telecommands.

In the transition to the off mode, EMCS is not commanding to turn the filter wheel to the closed position autonomously (It must be noted that the filter wheel is already in the closed position in this [safe stand-by] mode).

6.3.4 IDLE Mode K2

This mode of operation shall be entered from any mode of operation with the exception of the off mode, the initialisation mode, and the on-ground test mode.

The status of the Filter Wheel, CCDs, thermal control temperature, calibration source, HOPs, etc. will depend on experiment configuration performed by Telecommands that in this mode are immediately executed.

The EMCS master unit shall acquire its own HK data as well as the HK data from the other EMCS electronic units periodically and forward them to OBDH bus for the transmission via TLM.

In this mode all the Telecommands, with the exception of those listed in the SAFE STAND-BY and IN-FLIGHT TEST modes, are accepted. However, Dump EMDH and EMCR Memory TLCs are accepted and executed also in this mode.

EMCS shall perform the thermal control of the CCD's. The temperature of the CCD's shall be kept between -140 °C and -30 °C.

In this mode Shroud and Annealing heaters will be off.

EMCS shall exit this mode upon reception of telecommands from the OBDH bus in order to enter one of the following modes:

a) Safe Stand-by;
b) Prime;
c) Fast;
d) Offset/Variance;
e) CCD Diagnostics;
f) Annealing;
g) De-icing;
h) Decontamination
i) In-Flight Test.

It is not allowed to remove primary power in this mode.

6.3.5 OFFSET / VARIANCE Mode K5

This mode of operation shall be entered from the IDLE mode upon reception of the "Enter EMCS Offset & Variance Mode" TLC from the OBDH bus. The following actions will be performed during the execution:

- The EMDH shall initialise itself to receive data from one HBR I/F and store them in memory;
- The "Start Observation" command will be sent to EMCR;
- A commanded number of frames, will be received and discarded;
- The last frame sent from EMCR will be stored in the EMDH;
- Offset and Variance of the complete stored frame will be calculated;
- The Offset table and Variance will be sent to Ground by TLM (one shot).
- The Offset table will be stored in the EMDH ready to be uploaded in the EMCR tables

The algorithms for the Offset and Variance calculations are described in the relevant paragraph.

One CCD at the time shall be read in imaging/timing read-out mode with full/partial window option and one-node reading.

One frame shall be read. The energy of all the pixel shall be stored temporarily in the EMDH and then the offset and the variance shall be calculated on-board.

At the end of the transmission of all the data, EMCS shall made automatic transition to the Idle Mode.

No Telecommands will be accepted in this mode with the exception of "Enter EMCS IDLE Mode".

The status of the Filter Wheel, CCDs, thermal control temperature, calibration source, etc. will depend on experiment configuration performed in IDLE mode.

EMCS shall perform the thermal control of the CCD's. The temperature of the CCD's shall be kept between -140 °C and -30 °C.

In this mode Shroud, Annealing and HOPs heaters will be off.

It is not allowed to remove primary power in this mode.

EMCS shall exit this mode in the following conditions:

1) To enter automatically the IDLE mode when Offset/Variance calculation has been performed, Offset/Variance has been sent to ground and Offset table has been loaded in the EMCR. In this case:
   - the HBR I/Fs will be disabled.
   - the scientific TLM will be disabled.
   - the capability to manage all the TLC will be activated
2) To enter the IDLE mode, interrupting the Offset/Variance calculation or transmission to Ground/EMCR, by using the Ground TLC "Enter EMCS IDLE Mode". In this case:
   - "Stop Observation" command will be sent to EMCR
   - the HBR I/Fs will be disabled
   - Offset and Variance calculation will be stopped

- all the scientific information already in the EMDH memory will be sent to Ground
- the scientific TLM will be disabled
- the capability to manage all the TLC will be activated

3) To enter the SAFE STAND-BY mode, by Telecommand, only in emergency case.

6.3.6 CCD DIAGNOSTIC Mode K6

This mode of operation shall be entered from the IDLE mode upon reception of the "Enter EMCS CCD Diagnostic Mode" TLC from the OBDH bus. The following actions will be performed during the execution:

- The EMDH shall initialize itself to receive data from one HBR I/F and store them in memory;
- The "Start Observation" command will be sent to EMCR;
- A commanded number of frames will be received and discarded;
- The last frame sent from EMCR will be stored in the EMDH;
- The data relevant to pixel energy of a complete frame will be sent to Ground by TLM (one shot).

One CCD at the time shall be read in imaging/timing read-out mode with full/partial window option and one-node reading.

One frame shall be read. EMCS shall be capable to store the energy values of all the pixels of the selected CCD in RAM.

Data from the other CCD's shall be ignored.

The energy of each pixel (relevant to one frame only) and the H/K data shall be transmitted at the appropriate rate to the OBDH bus without processing.

No Telecommands will be accepted in this mode with the exception of "Enter EMCS IDLE Mode".

The status of the Filter Wheel, CCDs, thermal control temperature, calibration source, etc. will depend on experiment configuration performed in IDLE mode.

At the end of the transmission of all the data, EMCS shall made automatic transition to the Idle Mode.

EMCS shall perform the thermal control of the CCD's. The temperature of the CCD's shall be kept between –140 °C and +40°C.

In this mode Shroud, Annealing and HOPs heaters will be off.

It is not allowed to remove primary power in this mode.

EMCS shall exit this mode in the following conditions:

1) To enter automatically the IDLE mode when Diagnostic data have been sent to ground. In this case:
   - the HBR I/Fs will be disabled to receive data

- the scientific TLM will be disabled
- the capability to manage all the TLC will be activated

2) To enter the IDLE mode, interrupting the Diagnostic data collection and transmission to Ground, by using the Ground TLC “Enter EMCS IDLE Mode”. In this case:
   - “Stop Observation” command will be sent to EMCR
   - the HBR I/Fs will be disabled to receive data
   - Diagnostic data collection and transmission to Ground will be stopped
   - all the scientific information already in the EMDH memory will be sent to Ground
   - the scientific TLM will be disabled
   - the capability to manage all the TLC will be activated
3) To enter the SAFE STAND-BY mode, by Telecommand, only in emergency case.

6.3.7 EXTRA-HEATING - ANNEALING Mode K7

This mode of operation shall be entered from the idle mode upon reception, with the appropriate parameters, of the “Enter EMCS Extra-heating Mode” TLC from the OBDH bus. The heater configuration to be used is the one programmed by the “Load Extra-heating Configuration” TLC (K35)

- The filter wheel shall be turned to the open position if it were in a different position before entering this mode.
- The Door shall be open.
- The temperature of the CCD's shall be kept at 130 °C (fine setting can be performed by Telecommand).

If the transition can be executed the following actions will be performed:

- to apply primary power to the Annealing and the Secondary Shroud heaters by switch in the EMDH;
- to activate the Annealing heater control with the requested temperature (EMDH will send to EMCR the appropriate command).

If deactivation of the nominal temperature control of the focal plane is requested, the setting temperature of the nominal temperature control is saved and the nominal temperature control is disabled.

The CCD's shall be kept at that temperature for about 36 hours. The EMDH will monitor that it is not exceeded: if this happens, all the Extraheating heaters will be automatically switched off and the nominal temperature control with the original setting value will be activated.

In this mode CCD and HOPs heaters will be off.

No Telecommands will be accepted in this mode with the exception of “Enter EMCS IDLE Mode”.

An appropriate HK telemetry shall be sent to the OBDH bus.

EMCS shall exit this mode in the following conditions:

1) to enter the IDLE mode, interrupting the Annealing process, by using the Ground TLC "Enter EMCS IDLE Mode". In this case:
   - the EMDH switch used to power the Annealing heater will be switched off
   - the EMDH switch used to power the Shroud heater will be switched off
   - the focal plane temperature setting value before extra-heating will be passed to EMCR to be used for the standard focal plane temperature control
   - the EMDH will monitor that focal plane temperature does not exceed the temperature range programmed by "Load Thermal Monitoring Limits" TLC
   - the capability to manage all the TLC will be activated
2) to enter the SAFE STAND-BY mode, by Telecommand, only in emergency case.

It is not allowed to remove primary power in this mode.

6.3.8 EXTRA-HEATING - DE-ICING Mode K7

This mode of operation shall be entered from the idle mode upon reception, with the appropriate parameters, of the "Enter EMCS Extra-heating Mode" TLC from the OBDH bus. The heater configuration to be used is the one programmed by the "Load Extra-heating Configuration" TLC (K35)

- The filter wheel shall be turned to the open position if it were in a different position before entering this mode.
- The Door shall be open.
- The temperature of the CCD's shall be kept at -70 °C (fine setting can be performed by Telecommand).

If the transition can be executed the following actions will be performed:

- to apply primary power to the the Secondary Shroud heaters by switch in the EMDH;
- to activate the CCD Thermal heater control with the requested temperature (EMDH will send to EMCR/EMAE the appropriate command).

If deactivation of the nominal temperature control of the focal plane is requested, the setting temperature of the nominal temperature control is saved and the nominal temperature control is disabled.

The CCD's shall be kept at that temperature for about 36 hours. The EMDH will monitor that it is not exceeded: if this happens, all the Extra-heating heaters will be automatically switched off and the nominal temperature control with the original setting value will be activated.

In this mode HOPs heaters will be off.

The temperature of the secondary shroud shall be kept at the necessary temperature using the EMCS controlled secondary shroud heaters only. The temperature shall be monitored from ground in an open loop manner via HK telemetry .

No Telecommands will be accepted in this mode with the exception of "Enter EMCS IDLE Mode".

An appropriate HK telemetry shall be sent to the OBDH bus. The secondary shroud temperature shall be included in the HK telemetry.

EMCS shall exit this mode in the following conditions:

1) to enter the IDLE mode, interrupting the Secondary Shroud/De-icing process, by using the Ground TLC "Enter EMCS IDLE Mode". In this case:
   - the EMDH switch used to power the Shroud heater will be switched off
   - the focal plane temperature setting value before extra-heating will be passed to EMCR to be used for the standard focal plane temperature control
   - the EMDH will monitor that focal plane temperature does not exceed the temperature range programmed by "Load Thermal Monitoring Limits" TLC
   - the capability to manage all the TLC will be activated
2) to enter the SAFE STAND-BY mode, by Telecommand, only in emergency case.

It is not allowed to remove primary power in this mode.

6.3.9 EXTRA-HEATING - DECONTAMINATION Mode K7

This mode of operation shall be entered from the idle mode upon reception, with the appropriate parameters, of the "Enter EMCS Extra-heating Mode" TLC from the OBDH bus. The heater configuration to be used is the one programmed by the "Load Extra-heating Configuration" TLC (K35)

- The filter wheel shall be turned to the open position if it were in a different position before entering this mode.
- The Door shall be open.
- The temperature of the CCD's shall be kept at -20 °C (fine setting can be performed by Telecommand).

If the transition can be executed the following actions will be performed:

- to apply primary power to the Annealing and Shroud heaters by switch in the EMDH;
- to activate the Annealing and Shroud heater control with the requested temperature (EMDH will send to EMCR the appropriate command).

If deactivation of the nominal temperature control of the focal plane is requested, the setting temperature of the nominal temperature control is saved and the nominal temperature control is disabled.

The CCD's shall be kept at that temperature for about 36 hours. The EMDH will monitor that it is not exceeded: if this happens, the Annealing heater will be automatically switched off and the nominal temperature control with the original setting value will be activated.

The CCD's shall be kept at that temperature for about 3 hours.

An appropriate HK telemetry shall be sent periodically to the OBDH bus.

No Telecommands will be accepted in this mode with the exception of "Enter EMCS IDLE Mode".

EMCS shall exit this mode in the following conditions:

1) to enter the IDLE mode, interrupting the Decontamination process, by using the Ground TLC "Enter EMCS IDLE Mode". In this case:
   - the EMDH switch used to power the Annealing and Shroud heaters will be switched off
   - the focal plane temperature setting value before extra-heating will be passed to EMCR to be used for the standard focal plane temperature control
   - the EMDH will monitor that focal plane temperature does not exceed the temperature range programmed by "Load Thermal Monitoring Limits" TLC
   - the capability to manage all the TLC will be activated
2) to enter the SAFE STAND-BY mode, by Telecommand, only in emergency case.

It is not allowed to remove primary power in this mode.

6.3.10 OVERALL THERMAL SYSTEM DESCRIPTION

The purpose of the Thermal Control System is to control the operating temperature of the CCD focal plane, and to restore good operating conditions after degradation due to contamination, radiation or failure of the nominal system.

In order to meet the above requirements, the Thermal Control System has flexibility both in terms of control temperature, and heater configuration.

A simplified schematic of the system is shown in Fig.6.9.10-1.

The different temperature range are achieved with four heaters which are:

- Control Heaters (nominal and redundant) to control the temperature of the CCDs during normal operation and DeIcing Extrahetaing Mode.
- Annealing Heater to control the temperature during Decontaminationa and Annealing Extraheating Modes
- Shroud Heater to warm up the Shroud during during all Extraheating Modes to allow higher temperature at the CCD focal plane, and to remove ice build-up.
- Standby Heater to maintain an acceptable CCD operating temperature when EPIC is OFF.

To control the heaters of the Thermal System there are two closed loop control systems, and two open loop switches:

The first closed loop controller is hardware within the EMAE, and consists of a Nominal or Redundant system having a PRT input conditioning circuit, comparator and power switch which drives the selected 5 Watt control heater in the CCD focal plane to maintain the CCD temperature at the commanded set point of -150C to +50C.

The second closed loop controller is software within the EMCR which monitors the extended range PRT in the camera head via the EMAE, and commands the 28 Watt Annealing Heater ON/OFF via the EMAE. The temperature is controlled between two commandable limits.

The two open loop switches are the ON/OFF power to the 10 Watt Shroud Heater controlled by the EMDH, and the 4 Watt CCD standby heater controlled by the spacecraft.

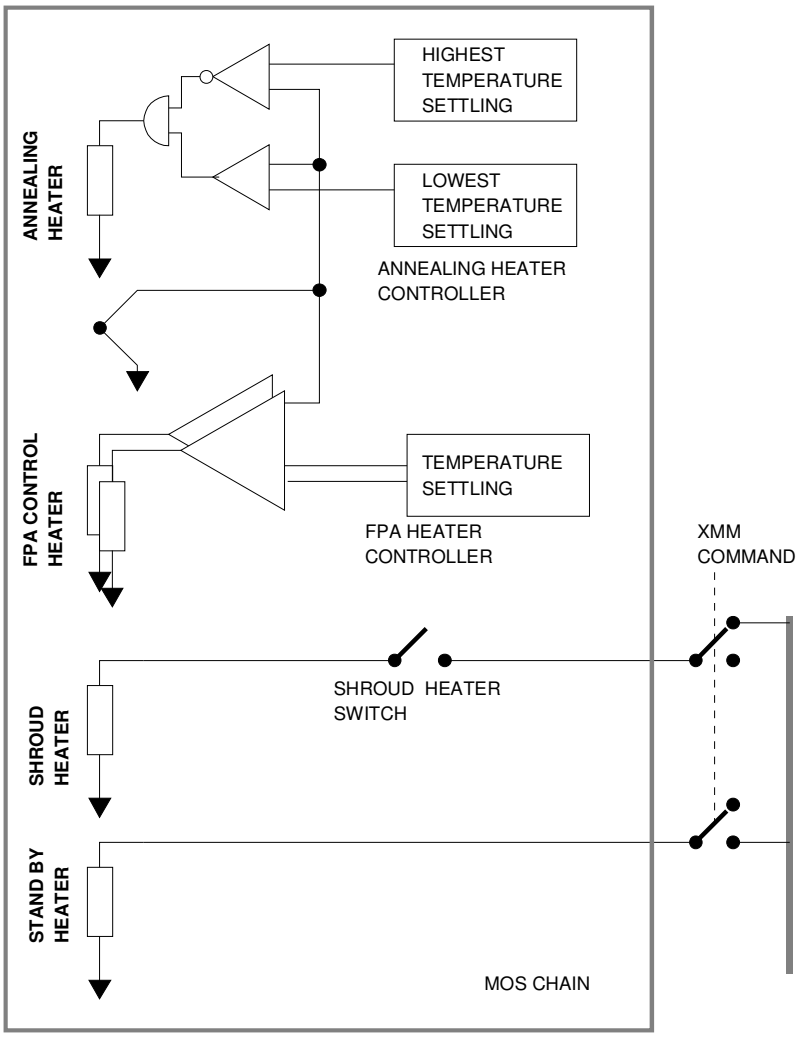


Figure 6.3.10-1: Thermal System overview

A detailed description of the Thermal System is given in Fig. 6.1.4-1.

6.3.11 IN-FLIGHT TEST Mode K8

This mode of operation shall be entered from the IDLE mode upon reception of the "Enter EMCS In-Flight Test Mode" TLC from the OBDH bus. The following actions will be performed during the execution:

- the EMDH initialise itself to receive data on the HBR I/Fs and process them as required;
- the "Start Observation" command will be sent to EMCR;
- the Scientific telemetry will be activated.

The status of the Filter Wheel, CCDs, thermal control temperature, etc. will depend on experiment configuration performed in IDLE mode.

In tests using simulated sources all the experiment works as in observation: the data are not readout from the CCDs but they are generated at the EMAE or EMCR level.

In tests dedicated to specific H/W and S/W functions are grouped different EMDH and EMCR tests (memory area test, H/W test, etc.) which can be individually triggered: during test execution some of the standard functions performed by the unit under test could be suspended.

Predefined digital patterns shall be generated at the beginning of the digital part of the electronic chain in order to test the functions of the electronic chain related to the elaboration of the scientific data.

The above mentioned patterns shall be stored permanently in EMCR or EMAE and used to simulate events.
EMCS H/K data will be available via TLM, if not interrupted due to execution of particular tests.

No telecommands are accepted in this mode, with the following exceptions:
- Enter EMCS IDLE Mode
- Perform EMDH Memory Check
- TBD

EMCS shall perform the thermal control of the CCD's.

In this mode Secondary Shroud, Annealing and HOPs heaters will be off.

In this mode the Calibration Source will not be active.

Besides, provisions shall be made to test some specific functions at unit level.

EMCS shall exit this mode in the following conditions:
1) To enter the IDLE mode, interrupting the in-flight test process, by using the Ground TLC “Enter EMCS IDLE Mode”. If instrument test using simulated sources (EMAE or EMCR) is in course, the following actions will be performed during the execution:
   - “Stop Observation” command will be sent to EMCR;
   - HBR I/Fs will be disabled to receive data;
   - All the scientific information already in the EMDH memory will be sent to Ground;
   - Scientific TLM will be disabled;
   - The capability to manage all the TLCs will be activated.

   If some H/W or S/W specific tests are under execution in the EMCR or EMDH, they will be safely suspended and the capability to manage all the TLCs will be activated.
2) To enter the SAFE STAND-BY mode, by Telecommand, only in emergency case.

It is not allowed to remove primary power in this mode.

6.4 DESCRIPTION OF OBSERVATION MODES (RD 12, §3.)

6.4.1 PRIME Mode K3

EMCS shall enter this mode from the IDLE mode upon reception of the "Enter EMCS Prime Observation Mode" from the OBDH bus. The following actions will be performed during the execution:

- the EMDH will initialise itself to receive data on the HBR I/Fs and process them as required;
- the "Start Observation" command will be sent to EMCR;
- the Scientific TLM will be activated.

EMCS units shall be reconfigured according to the parameters of the telecommand under the supervision of the master unit.

After reconfiguration, the master unit shall command the other units to start the operations of this mode.

CCD1 through CCD7 shall be read in imaging mode from one node. CCD2 through CCD7 shall be read only with the full window option, i.e.:

$$x_0 = y_0 = 1, \Delta x = 610 \text{ and } \Delta y = 602$$

and with the minimum T_{int} greater than T_0.

The nodes of CCD2 through CCD7 shall be read approximately at the same time (no synchronisation is required).

The Prime mode shall be divided into two submodes:

a) Full Window; and
b) Partial Window.

In the Full Window submode, CCD1 shall operate with the full window option and with the minimum T_{int} greater than T_0 for this option.

In the Full Window submode, there shall be an overall time unit corresponding to a macroframe. This time unit shall be less than 2.4 s ± 20%.

In the Partial Window submode, CCD1 shall operate with the partial window option and with the minimum T_{int} greater than T_0 for this option.

The EMCS shall:

a) determine the photon energy;
b) reject the cosmic rays;
c) reject the contribution from bright pixels;

on a **frame by frame** basis on the output coming from the seven CCD's.

Since the output from the EMCS detector is made of eight channels (two from CCD1 and six form CCD2 through CCD7), then the two half-frames from the two channels of CCD1 (if active) shall need special processing on ground.

The implementation of the requirements on the photon energy determination and the cosmic rays rejection shall occur in three steps:

a) An event recognition algorithm shall be used (Appendix B);
b) An upper threshold shall be applied;
c) A lower threshold shall be applied.

Science report packets shall be prepared.

A science report packet shall be put in the EMCS output queue as soon as it is prepared.
The data storage area shall be allocated to the different CCD channels in a suitable manner.

In case the rate of the incoming scientific events is greater than the transmission rate on the OBDH bus, EMCS shall send a warning message to the CDMS. This message shall be sent when the storage area is about 50% filled.

In case the scientific data storage area is about being filled, the new incoming data shall be rejected on a frame by frame basis. The number of events rejected shall be counted and included in an HK source packet together with the start time and the end time of this overflow condition. The ending of the overflow condition is set when the related storage area is less than about 25% filled.

HK source packets shall be sent to the OBDH bus at least every 8 s.

No Telecommands will be accepted in this mode with the exception of “Enter EMCS IDLE Mode”.

The EMCS shall control the temperature of the CCD's at the settled level, which is, in default conditions, -100°C. This temperature is currently considered optimal for scientific purposes but it may be changed during the SMP.

The status of the Filter Wheel, CCDs, thermal control temperature, calibration source, etc. will depend on experiment configuration performed in IDLE mode.

In this mode Shroud, Annealing and HOPs heaters will be off.

EMCS can exit this mode in the following conditions:

1) To enter the IDLE mode, interrupting the Observation phase, by using the Ground TLC “Enter EMCS IDLE Mode”. The following actions will be performed during the execution:
   - “Stop Observation” command will be sent to EMCR;
   - HBR I/F will be disabled to receive data;
   - All the scientific information already in the EMDH memory will be sent to Ground;
   - Scientific TLM will be disabled;
   - Capability to manage all the TLC will be activated.
2) To enter the SAFE STAND-BY mode, by Telecommand, only in emergency case.

It is not allowed to remove primary power in this mode.

6.4.2 FAST Mode K4

EMCS shall enter this mode from the IDLE mode upon reception of the "Enter EMCS Fast Observation Mode" from the OBDH bus. The following actions will be performed during the execution:

- the EMDH will initialise itself to receive data on the HBR I/Fs and process them as required;
- the "Start Observation" command will be sent to EMCR;
- the Scientific TLM will be activated.

EMCS units shall be reconfigured according to the parameters of the telecommand under the supervision of the master unit.

After reconfiguration, the master unit shall command the other units to start the operations of this mode.

CCD1 shall be read in timing read-out from either one of the two nodes.

On the output of CCD1, EMCS shall:

a) determine the photon energy;
b) reject the cosmic rays

on a line by line basis (bright pixel rejection is not required).

The implementation of the requirements on the photon energy determination and the cosmic rays rejection shall occur in two steps:

a) An event recognition algorithm shall be used (Appendix B);
b) An upper threshold shall be applied.

CCD2 through CCD7 shall be read in imaging mode from one node with the full window option, i.e., $x_0 = y_0 = 1$, $\Delta x = 610$, $\Delta y = 602$ and with the minimum T_{int} greater than T_0.

The nodes of CCD2 through CCD7 shall be read simultaneously (but no synchronization is required).

For the output coming from the six peripheral CCD's, EMCS shall:

a) determine the photon energy;
b) reject the cosmic rays;
c) reject the contribution from bad pixels;

on a frame by frame basis .

For the output of the six peripheral CCD's, the implementation of the requirements on the photon energy determination and the cosmic rays rejection shall occur in three steps:

a) An event recognition algorithm shall be used (Appendix A);
b) An upper threshold shall be applied;
c) A lower threshold shall be applied.

Science report packets shall be prepared.

A science report packet shall be put in the EMCS output queue as soon as it is prepared.

The data storage area shall be allocated to the different CCD channels in a suitable manner.

In case the rate of the incoming scientific events is greater than the transmission rate on the OBDH bus, EMCS shall send a warning message to the CDMS. This message shall be sent when the storage area is about 50% filled.

For the scientific data coming from CCD1, in case the related storage area is about being filled, the new incoming data shall be rejected on a cycle by cycle basis. The number of (16 bit) words rejected shall be counted and included in an HK source packet together with the start time and the end time of this overflow condition. The ending of the overflow condition is set when the related storage area becomes less than about 25% filled.

For the scientific data coming from CCD2 through CCD7, in case the related storage area is abuot being filled, the new incoming data shall be rejected on a frame by frame basis. The number of events rejected shall be counted and included in an HK source packet together with the start time and the end time of this overflow condition. The ending of the overflow condition is set when the related storage area becomes less than about 25% filled.

HK source packets shall be sent to the OBDH bus at least every 8 s.

No Telecommands will be accepted in this mode with the exception of “Enter EMCS IDLE Mode”.

The EMCS shall control the temperature of the CCD's at the settled level, which is, in default conditions, -100°C. This temperature is currently considered optimal for scientific purposes but it may be changed during the SMP.

The status of the Filter Wheel, CCDs, thermal control temperature, calibration source, etc. will depend on experiment configuration performed in IDLE mode.

In this mode Shroud, Annealing and HOPs heaters will be off.

EMCS can exit this mode in the following conditions:

1) To enter the IDLE mode, interrupting the Observation phase, by using the Ground TLC “Enter EMCS IDLE Mode”. The following actions will be performed during the execution:
   - “Stop Observation” command will be sent to EMCR;
   - HBR I/F will be disabled to receive data;
   - All the scientific information already in the EMDH memory will be sent to Ground;
   - Scientific TLM will be disabled;
   - Capability to manage all the TLC will be activated.
2) To enter the SAFE STAND-BY mode, by Telecommand, only in emergency case.

It is not allowed to remove the primary power in this mode.

7. EXPERIMENT ON BOARD SOFTWARE

7.1 EMDH SW

7.1.1 Code description

Code is fully described in the Baseline Document for SW Requirements of the EPIC MOS Data Handling (EMDH) Unit (part a) and Baseline Document for SW Requirements of the EPIC MOS Data Handling (EMDH) Unit (part b) and in the SW Detailed Design Document (DDD) for the EMDH unit.
This section is manly intended to provide an handbook for the item of the code to address easily them.

7.1.1.1 Main Functions

EMDH SW implements the following functions:
- Collect Housekeeping data
- Collect Scientific Data coming from CCD control boxes
- Process Scientific Data with reference to the active operating mode
- Prepare Source Packet containing Scientific Data and Housekeeping
- Receive, decode and execute of Telecommands sent from Ground
- Dispatch telecommands to the addressed units
- Provide patch & dump capabilities for data resident on EMDH
- Manage EMDH Software uploading and Memory dumping
- Dispatch Uploaded software for the other electronic boxes (EMCR)
- Address software patches for the other electronic boxes (EMCR)
- Packet memory dumps coming from the other electronic boxes (EMCR)
- Manage On Board Time (OBT)

7.1.1.2 Function breakdown

The system is decomposed in the following main functions
- OBDH Bus I/F composed by:
  - RBI I/F Rx Handler for reception of the Telecommand Packets
  - RBI I/F Tx Handler for transmission of the Source Packets
  - OnBoard Time Management
- Basic Loader to upload new software and to interact with Ground without activation of Ada Real Time System
- Initialization of any loaded software either from PROM or Ground
- Bootstrap Loader, a PROM Monitor for handling bootstrap and restart operations
- Telecommand Manager
- Kernel for tasks supervision and scheduling
- Interrupt Handler to react to Interrupt Request Signals calling the related Interrupt Service Routine
- Data Housekeeper, composed by:

- Data I/O, for upgrading of the working parameters or configuration tables
- HK Data Collection
- Memory Dump Formatter
- On Board Time management

- Data Processing, devoted to Scientific processing as thresholdings, bright pixel rejections, offset and variance calculation
- Telemetry Manager, composed by:
  - Source Packets Preparation (HK & Scientific Data)
  - Source Packet Store
- an Hardware Software Interface layer providing application layer with a set of services able to manage memory locations and I/O ports by direct call
- HBR & LBR I/F for reception of HK and Scientific Data and transmission of telecommands addressed to other electronic boxes

Fig. 7.1.1.2-1 shows the higher and lower level of the software functions.

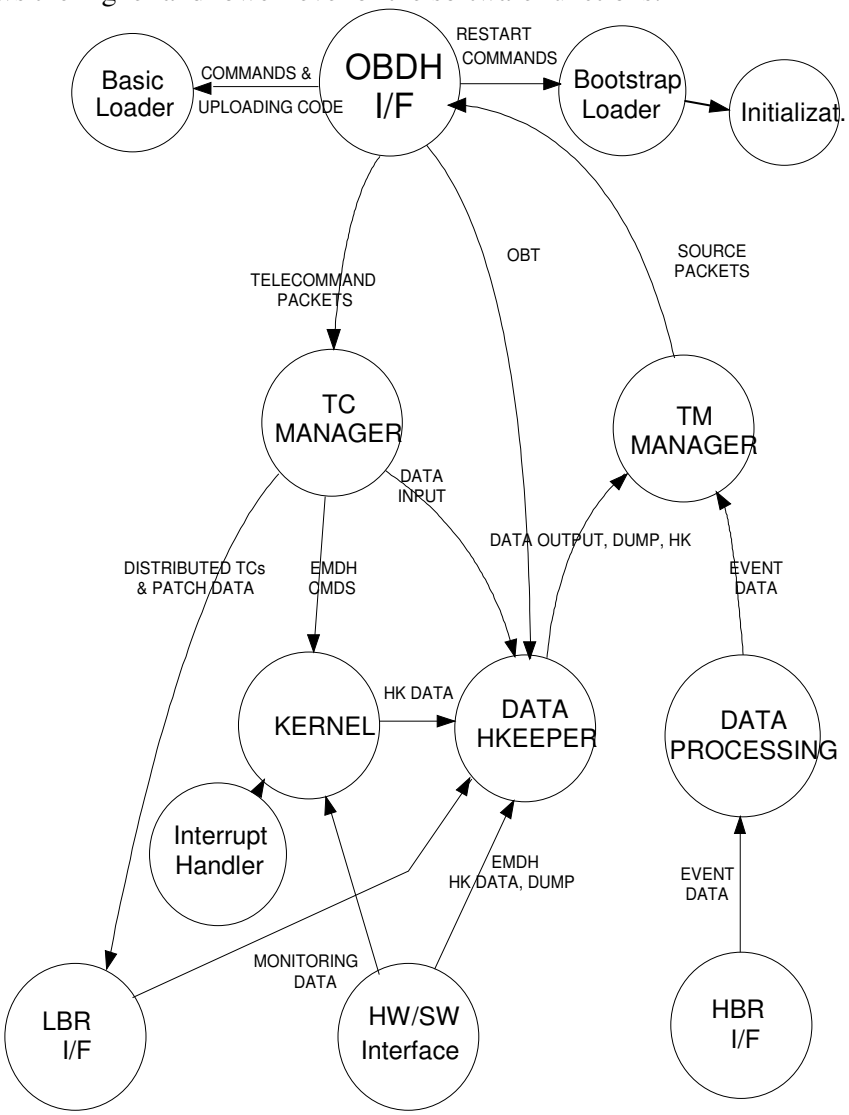


Figure 7.1.1.2-1

7.1.1.3 Environmental considerations

The software embedded in the EMDH unit *interfaces* with:

- the EMCR Unit, that sends Scientific CCD Data to EMDH through 8 High Bit Rate (HBR) channels coming from the Control and Recognition unit (EMCR);
- the OBDH bus of the spacecraft through a RBI chip and a DBU unit

The EMDH software runs on the hardware platform where:

- a master HPM 31750 processor for the Digital Data Handling; that microprocessor manages:
  - 2 Low Bit Rate channel (LBR), a low speed serial link for receiving HK data from EMCR and for distributing commands and data to EMCR. One LBR is for test purpose, and only one serial link at time is active.
  - a Remote Bus Interface RBI for DBI handling toward the OBDH bus
- a slave HPM 31750 processor devoted to process scientific data coming from 8 High Bit Rate channels (HBR), the high speed serial link for incoming Scientific Data from EMCR

Following the EMDH design, the embedded software system is structured in:

- the *data handling* section, executed by the master HPM-31750 processor and composed by:
  - an *Ada Periodic Executive* for run time support inclusive of standard libraries and run time features of a typical kernel;
  - an *Application Layer* inclusive of TC/TM manager and data housekeeper functions
  - an *HW/SW interface* layer for management of all the input/output channels.
- a *computing intensive* section executed by the slave HPM-31750 processor and composed by:
  - a *Data Processing* part, dealing with the scientific data processing, able to filter valid event and to reject noise as cosmic-rays or bright pixel,
  - a *HBR handler* interfacing with FIFOs for each HBR channel
  - a *simple handler* of the Inter Processor Communication (IPC) with a shared memory area visible to the master HPM 31750 through the system bus SBUS90.

As far as the interaction with H/W, the software shall control a given number of devices whose control is allocated to EMDH unit:

Two Heaters switches: - Annealing heater
- Shroud heater

Current Limiters
HOP's
Filter Wheel Power

7.1.1.4 Relation to other systems

The two MOS Data Handling systems do not interact to each other and act as slaves of the S/C Central Data Mgmt. Unit (CDMS) and are linked to the S/C OBDH sub-system bus through a RBI component. The EMDH complies with the operating modes of the whole EPIC MOS Camera System (EMCS), where the following states are foreseen for:

1. Launch and Early Orbit Phase (LEOP)
   - OFF; no power at all
   - INITIALIZATION: where the CCDs are Off

- SAFE STAND-BY: where the CCDs are Off
- IDLE: where CCDs are On and the filter is open and the HOP are activated once to enter the SMP phase

2. Scientific Mission Phase (SMP)
   - OFF; no power at all
   - INITIALIZATION: where the CCDs are Off
   - SAFE STAND-BY: where the CCDs are Off
   - IDLE: where CCDs are On and the filter is open
   - OPS; it stands for OPerationS that for the EMCS are:
     - Prime Mode
     - Fast Mode
     - Offset & Variance Mode
     - CCD Diagnostic Mode
     - Extraheating (Annealing, Sec.Shroud De-Icing, CCD Decontamination) Mode
     - In-Flight Test Mode

The following table 7.1.1.4-1 maps the EMCS operating mode with the EMDH Operating mode. The related Software modes are here reported.

Table 7.1.1.4-1

EMCS	EMDH	SW
LEOP Off	Off	=
LEOP Initialize.	Initialization	Initialization
LEOP Safe/St-by	Stand-By	Stand-By
		Maintenance
LEOP Idle	Idle	Idle
SMP Off	Off	=
SMP Initialize.	Initialization	Initialization
SMP Safe/St-by	Stand-By	Stand-By
		Maintenance
SMP Idle	Idle	Idle
OPS – Prime	Prime	Prime
OPS – Fast	Fast	Fast
Offset / Variance	Offset / Variance	Offset & Variance
CCD Diagnostic	CCD Diagnostic	Diagnostic
EXTRA-HEATING□Annealing□Shroud De-Icing□CCD Decontaminat	Extra-Heating	Extra-Heating
Test	Test	In Flight Test
		OnGround Test

7.1.1.5 Computer Software Configuration Item Identification

The processors for the Digital Data Handling Unit is the HPM 31750 implementing the MIL-STD-1750A instruction set, where:

- the used language is the Ada MIL-STD-1815 (Ada 83); and
- the Ada intrinsic tasking mechanism has been not used, because of better code efficiency. A periodic scheduling policy, managed by a scheduler called APEX (Ada Periodic Executive) has been used to schedule Ada procedures according to priority levels and time period constraints..

The software components of the EMDH units have beeen submitted to the following general constraints:

- OBDH bus bandwidth constraints
- Time constraints
- Memory constraints

as described in chapter 3.5 of SRD.

Furthermore constraints on the software are set by the interfacing requirement to the S/C TM/TC capabilities, as listed in RS-PX-0032 XMM - Packet Structure Definition.

The software is driven by:

- power-on signal
- RBI Commands
- Interrupt Requests
- Event Occurrences
- Telecommands from OBDH
- Test Cable Plugged-In condition

The foreseen software functions are allocated to software components as shown in the following table 7.1.1.5-1:

Table 7.1.1.5-1

Software Configuration	Software Component	Function	Processor	Language
CSCI1	Ada Periodic Executive	Kernel	MASTER	Ada 90% ASM 10%
CSCI2	Application Layer	TC Manager TM Manager Data Hkeeper	MASTER	Ada
CSCI3	HW/SW Interface	OBDH Bus I/F LBR Handler Interrupt Handler	MASTER	Ada 40% ASM 60%
CSCI4	Computing Intensive SW	Data Processing HBR Handler	SLAVE	Ada 40% ASM 60%
CSCI5	PROMed Monitor	Bootstrap Loader	MASTER	ASM
CSCI6	Basic SW	Initialization Basic Loader	MASTER	ASM

Therefore the EMDH software shall be composed by:

- CSCI1: APEX: Ada Periodic Executive inclusive of Basic System Services for Task Management and Ada Run Time Support
- CSCI2: Application Software
- CSCI3: HW/SW Interfaces Control Drivers
- CSCI4: Computing Intensive part
- CSCI5: PROMed Monitor
- CSCI6: Basic SW

CSCI1: APEX: Ada Periodic Scheduler

Activities: the CSCI1 is devoted to schedule the application processes following the scheduling descriptions inserted in a Periodic Process Table (PPT) and an Aperiodic Process Table (APT).
The CSCI1 is inclusive also of basic system services for locking/unlocking suspending and resuming periodic processes on request by the application software (task management)

Inputs: no-one

Outputs: O2: **end basic service** - return to the caller
O3: **process calls** to parameterless application procedures

Controls: C1: Periodic Real Time Clock (**rtc**)
C2: bootstrapping signal of "**software loaded**"
C3: **end process** of application procedure - return to scheduler
C4: **Basic Service Request** to Apex

Mechanism: M1: call from **Interrupt Service Routine (ISR)** triggered by an Interrupt request (for details see Fig 2-7.2.1-1 of SRD)

The components of the Ada Periodic Executive are : (for details see chapter 3.1.2 of SRD)

- **APEX - Initialization**

The Initialization is activated by a "software loaded" event signaled by the PROM Monitor after a **cold restart**.
In case of **warm restart** such control signals that software already loaded is ready for initialization; the initialization shall handle the elaboration of the Ada packages declarative parts. At the end, control is passed to scheduling part for activation of the defined processes.

- **APEX - Process Tables**

Two tables shall record the scheduling characteristics of both periodic and aperiodic processes, by means of descriptors.
Descriptors are not static and a pull of basic system services is supplied to the application software for changing the scheduling features of the described processes according to the processing needs.
The software is set in a defined operational mode by definition of the related process tables.

- **APEX - System Services**

A pool of basic system services allows application software to modify or inquiry the process tables. Therefore, an aperiodic (sporadic) process can be waked up and a periodic process can be suspended for a given time period (the time unit is the real time clock tick).

- **APEX - Scheduling and Process Execution**

When a process is eligible for running it is activated by means of an usual call procedure (no Ada Tasking System is used).
Each application process is therefore seen as a parameterless procedure, that may interact with other process, by means of the supplied basic system services.
Each process shall terminate at the end of its own program flow; no pre-emption is allowed, unless an interrupt occurs. In that case the related Interrupt Service Routine (ISR) is activated, the interrupt is serviced immediately and the scheduling is updated.

CSCI2: Application Software

Activities: the CSCI2 is containing all the application processes for data housekeeping, packetisation and Telecommand handling.

Inputs:
I1: **Memory Service Results**
I2: **Bootstrap Report**
I3: **Valid Event** Data
I4: **Time** information
I5: **Chain HK** data

Outputs:
O1: **Basic Service Request** to Apex
O2: **end process** of application procedure - return to scheduler
O3: call to low-level memory services (**Memory Services Request**)
O4: call to procedures for HW **Interfaces handling** drivers
O5: Formatted **Source Packets**
O6: **Dispatched TCs**

Controls:
C1: Periodic **Process Calls**
C2: **End basic services** - return to the caller
C3: **Buffered TCs** from OBDH

(for details see Fig 2-7.2.2-1 of SRD)

For details on components of the Application Software see chapter 3.1.3 of SRD for telecommands, chapter 3.1.4 of SRD and chapter 3.1.5 of SRD for telemetry housekeeping and packetisation.

The components of the Application Software are:

- **TC Manager**

The Telecommand (TC) Manager is charged of reception, validation and request for schedule of the Telecommand received from ground. It is also charged of the dispatching of telecommand addressed to other electronic boxes.
For details of the Commands Management see chapter 3.1.3.1 of SRD for Acquisition, chapter 3.1.3.2 of SRD for Validation, chapter 3.1.3.3 of SRD for Execution and chapter 3.1.3.4 of SRD for Despatching. See also chapter 7.12 of DDD and chapter 7.12.1 of DDD for Validation, chapter 7.12.2 of DDD for Verification and chapter 7.12.3 of DDD for Operation mode acceptance check.

For details about proper commands see chapter 3.1.3.of SRD for Direct RBI Commands; chapter 3.1.3.5 of SRD for Mode Transition, chapter 3.1.3.6 of SRD for Maintenance and Special Commands for EMDH, chapter 3.1.3.7 of SRD for Configuration Commands for EMDH, chapter 3.1.3.8 of SRD for On/Off Commands for EMDH, chapter 3.1.3.9 of SRD for Memory Management Commands for EMDH, chapter 3.1.3.10 of SRD for TM Management Commands for EMDH, chapter 3.1.3.11 of SRD for OBT Management Commands, chapter 3.1.3.12 of SRD for Commands to EMCR with Response, chapter 3.1.3.13 of SRD for commands for EMCR without Response.

- **Data HouseKeeper**

That components shall include all the data collection operations related to:

- Housekeeping data coming from LBR channel
- Housekeeping data extracted by the EMDH monitor and inclusive of Ack of the received TCs
- Memory dumps formatting both for dumps from other electronic boxes (through the LBR channel) and EMDH memory (through the Basic Software)
- Input/Output operations for EMDH working parameters, data and configuration tables (Bright Pixels, Patterns Tables, Periodic and Aperiodic Process Tables, Interfaces configuration and so on)
- On Board Time (OBT) management

For details about the Housekeeping Collection see chapter 3.1.5.2 of SRD and chapter 7.8 of DDD

- **TM Manager**

The Telemetry (TM) Manager is charged of all the operations related to preparation of the Source Packets after the collection made by the Data Handling components from the related data reception channels of:

- HouseKeeping (HK) data
- Scientific Data (events and ancillary info)
- others, as memory dumps, table parameters output

For details about the telemetry see TM details doc for Packet structure and chapter 7.11 of DDD

Beside these in chapter 7.3 of DDD is described how Synchro Object manages synchronization between Objects, in chapter 7.4 of DDD is described how Switch Object manages on/off commands. and in chapter 7.10 of DDD is described how Thermal Object manages temperatures

In chapter 7.6 of DDD is decribed how EMCR Services Object manages *Single command execution, Single command execution and send TM to ground, Wait execution of required command, Command with response block* i.e. the command i/f vs EMCR.
Last two Object in this set are relevant to the internal EMDH behavior (EMDH Services Object, chapter 7.7 of DDD) and its monitoring (Sytem Monitoring Object. chapter 7.9 of DDD).

CSCI3: Hardware Software I/Fs (Control drivers)

Activities: the CSCI3 collects all the software components devoted to drive direct actions on the HW devices through the HW/SW I/Fs.

Inputs: I1: Formatted **Source Packets**
I2: **Dispatched TCs** to be forwarded
I3: **RBI Instructions**

I4: **XMM OBT**
I5: Chain HK on the LBR Channel (**LBR Housekeeping**)
I6: **TM(6) Packets** from Basic Software

Outputs: O1: **Buffered TC** coming from OBDH
O2: **Telemetry** Source **Packets** to OBDH
O3: **Dispatched Commands** to EMCR
O4: **TC to Basic Software**
O5: **RBI** command of **'Start ICU'** to come on initilaization 2nd phase
O6: **RBI** command of **reset** (warm restart)
O7: call to **Interrupt Service Routine**
O8: **Time** information
O9: **Chain HK** data

Controls: C1: call to procedures for HW **Interfaces handling** drivers
C2: **Interrupt Request** signals
C3: interrupts due to **RBI Commands** (from OBDH Bus)
C4: **Telecommand** from OBDH

(for details see Fig 2-7.2.3-1 of SRD)

The Software/Software are described in chapter 3.3.1 of SRD
For details on Hardware/Software Interfaces see chapter 3.3.2.1 of SRD for general aspects, chapter 3.3.2.2 of SRD for I/O mapped interfaces and chapter 3.3.2.3 of SRD for interrupt handlers.

The components of the Hardware/Software Interfaces are:

- **Interrupt Handler**

According to [AD.5], the following interrupt handlers shall be provided by the software on the master 31750:
General Interrupts (**Interrupt Requests**), as

- Synch Pulse Interrupt handler
- HBR 31750 Slave I/F Attention Interrupt
- LBR UART RX Interrupt handler
- LBR UART TX Interrupt handler
- Monitor Interrupt handler

Interrupts from RBI (**RBI Commands**) as:

- Instruction to RBI Interrupt handler - IT1n
- Instruction to USER Interrupt handler -IT2n

To each interrupt the software reacts with a defined ISR that interacts with the scheduling made by APEX.
As far as the **RTC interrupt** is concerned, it is dealt differently as its own ISR is the APEX scheduler itself.

The slave 31750 shall be provided by the following interrupt handlers:

- HBR End of Frame (EOF)
- HBR FIFO FULL (FF)
- Instruction to Slave - IT1n
- Monitor Interrupt handler

- **OBDH Bus I/F**

The interface for the OBDH bus shall handle the memory buffer filled by RBI with transmitted data through an OBDH Bus Telecommand.
It shall be provided also with the software part of the OnBoard Time Management in order to provide the Source packets with the required time information.
For details concerning OBDH Communication see chapter 3.3.6 of SRD (in chapter 3.3.6.1 of SRD listing of TC whilst in chapter 3.3.6.2 of SRD listing of TM) and chapter 3.3.7 of SRD for Scientific Packets description.
Communication at RBI level is described in chapter 3.3.8 of SRD (in particular see chapter 3.3.8.1 of SRD for RBI chip details and chapter 3.3.8.2 of SRD for RBI chip management)

- **LBR Handler**

That component shall handle the Low Bit Rate Channel receiving the Housekeeping data of the other electronic boxes as well as memory dumps and command acknowledges.
For details concerning EMCR Commands see chapter 3.3.3 of SRD and for details concerning EMCR Housekeeping see chapter 3.3.5 of SRD. For the protocol see chapter 7.5 of DDD.

CSCI4: Computing Intensive Software I/Fs

Activities: the CSCI4 collects the software components devoted to Data Processing functions to be applied to event data coming from HBR channels.
Inputs: I1: **Scientific Data** on **HBR** Channels
Outputs: O1: **Valid Event** data to be formatted
Controls: C1: call to procedures for **handling** HBR **Interfaces**
C2: **Event Occurrence** on HBR Channels
(for details see Fig 2-7.2.4-1 of SRD)
The components of the Computing Intensive Software Interfaces are: (for details see chapter 3.1.6 of SRD)

- **HBR Handler**

That component shall handle the High Bit Rate Channel receiving the scientific data (event-data). It may be provided with a simplified buffer management for the incoming data in the different Observation modes.
The protocol with EMCR for what concerns Scientific Data is in chapter 3.3.4 of SRD

- **Data Processing**

That component is related to all scientific processing to be applied to the scientific data (event-data and ancillary).
Scientific processing mainly deals with additional event rejections, according to the scientific requirements and time constraints imposed by the event rates, but limited by the processing time constraints imposed by processor speed and allowed data throughput.
Details of Observation Data Processing are in chapter 3.1.6.1 of SRD whilst Offset and Variance Management is described in chapter 3.1.6.2 of SRD (in particular chapter 3.1.6.2.2 of SRD, chapter 3.1.6.2.3 of SRD and chapter 3.1.6.2.4 of SRD are related to Data Acquisition in Full Frame, Window and Timing mode; chapter 3.1.6.2.5 of SRD is relevant to averaging sub-process; chapter 3.1.6.2.6 of SRD and chapter 3.1.6.2.7 of SRD deal with filtering sub-process and chapter 3.1.6.3 of

SRD and chapter 3.1.6.4 of SRD describes how to get Offset and Variance value plus the algotithm commandability).

See also chapter 7.13 of DDD and chapter 7.13.3 of DDD for Communication Data interfaces description, chapter 7.13.4 of DDD for Prime/Fast processing description, chapter 7.13.5 of DDD for Transparent processing description, chapter 7.13.6 of DDD for Offset and Variance processing description.

That component shall handle the Interprocessor communications between 31750 Master and Slave, by polling the communication area reserved to the master's messages and putting flags or messages to be polled by the 31750 Master.

CSCI5: PROM Monitor

Activities: the CSCI5 collects the software component devoted to all the bootstrapping operations activated whenever either a cold restart (power on) or a warm restart (RBI reset) occurs.
As such Monitor is resident on a different on-board PROM, is configured as separated C.I.

Inputs: no one

Outputs: O1: bootstrap signal of "**software loaded**"
O2: **Bootstrap Report** data

Controls: C1: **RBI Reset** trigger
C2: **RBI 'Start ICU'** command to come on initialization (2nd phase)
C3: **Exit from Basic SW**
C4: **Power- on** signal (from HW devices)
C5: **Test Cable** plugged-in condition

(for details see Fig 3.1.1-1 of SRD)

A monitor resident on PROM is foreseen for all the bootstrap operations after the execution of the microprocessor Built-In tests (BIT)

a. PROM checksum
b. RAM check and clean-up for both MASTER AND SLAVE
c. Software loading from PROM to RAM on MASTER 31750
d. Software loading from PROM to RAM on SLAVE 31750

Whenever a software reconfiguration has been performed after a complete uplinking of the code, the PROM monitor can be called by an RBI instruction of warm restart that holds the RAM contents.
For details see chapter 3.1.1 of SRD
The Boot procedure is described starting from chapter 7.1 of DDD (in particular chapter 7.1.3 of DDD addresses the bootstrap of the Master Processor, chapter 7.1.4 of DDD addresses the bootstrap of the Slave Processor, chapter 7.1.5 of DDD their synchronisation and chapter 7.1.6 of DDD the execution steps) and chapter 7.1.7 of DDD where involved items are detailed.

CSCI6: Basic SW

Activities: the CSCI6 collects the software component devoted to the memory services and maintenance.

Inputs: no one

Outputs: O1: **Exit** command to come back to restart (warm) operations

O2: **TM(6) Packets** from basic software
O3: **Memory Services Results**

Controls: C1: **Enter to Basic Software** triggered by either test cable plugged condition or Start ICU RBI command
C2: call to low-level memory services (**Memory Service Requests**)
C3: **Telecommand to Basic SW**

The Monitor resident on RAM shall provide a component able to deal with elementary SW maintenance operations like memory dumps, checksum calculation and software up loading. (for details see chapter 3.1.5.1 of SRD and see chapter 3.4.2 of SRD)
The activation of the basic software sets the software in Maintenance mode and can be triggered in two different ways:
a. when the software is in Stand-By mode, by reception of a suitable TC(5,1) - Start task Telecommand;
b. after a warm restart, when the system is in RESET state, by reception of a Start ICU Instruction-to-RBI with no zero parameter.
The basic software can be exit by reception of a reset ICU Instruction to RBI with no zero parameter that triggers a warm restart initializing the software without cleaning the RAM contents or by reception of a TC(5,2) - Exit Basic Software.

When a test cable is plugged in the test connector, the basic software shall be able to handle operations of the On Ground Test Mode inclusive of communications protocol through external ports instead of through RBI registers.

The Mantenance procedure is described starting from chapter 7.2 of DDD (in particular chapter 7.2.3.1 of DDD addresses BSW, chapter 7.2.3.2 of DDD addresses EV, chapter 7.2.3.3 of DDD addresses PKT, chapter 7.2.3.4 of DDD addresses INTR, chapter 7.2.3.5 of DDD addresses RBI, chapter 7.2.3.6 of DDD addresses UART, chapter 7.2.3.7 of DDD addresses MEM, chapter 7.2.3.8 of DDD addresses MEMORY, chapter 7.2.3.9 of DDD addresses CRC, chapter 7.2.3.10 of DDD addresses MODE and chapter 7.2.3.11 of DDD addresses EVEF).
Then a very simple protocol, to be used to let the basic software exchange messages via the UART device attached to the test cable is in chapter 7.2.4 of DDD

7.1.1.6 Hood Objects

The following table 7.1.1.6-1 lists in bottom-up order:
- Hood Object names that are link to the relevant section in the Hood Description Skeleton part of the DDD.
- Files that store the ralevant source code
- The Object provided operations

Table 7.1.1.6-1

HOOD Object	Files	Provided Operations
Calcmcd	ov/calcmcd.asm	Get_increment
Ccdff	ov/ccdff.asm	compute_ff_ov
Ccdwin	ov/ccdwnd.asm	compute_tm_ov compute_w_ov

Corona	ov/corona.asm	get_tm_corona get_corona
Dbllong	ov/dbllong.asm	vl_div vl_add
Ov	ov/ov.asm	update_ca_col update_ca_row set_window_limits update_wnd_row compute_rows_av compute_cols_av compute_variance update_av init_variables
Pixels	ov/pixels.asm	put_pixel get_pixel
Smooth	ov/smooth.asm	smooth_change_row smooth_pixel smooth_init
Sort	ov/sort.asm	simmetric_sort sort
Board_s	Boot_slave/board_s.asm	bit_check board_regs_init board_regs_warm_init mbx_read mbx_write
Boot_s	Boot_slave/boot_s.asm	warm_restart cold_restart
Bootmem_s	Boot_slave/bootmem_s.asm	ram_prg_checksum startprom_checksum startprom_load
Crc	bsw/crc.asm	crc_boot crc_compute crc_byte
Edac_s	Boot_slave/edac_s.asm	edac_check_and_enable
Fltrep	Boot_slave/fltrep_s.asm	fltrep_store fltrep_ram_to_regs
Hbr	Boot_slave/hbr_mos.asm	hbr_disable hbr_init
HBR_primefast	slave/hp_.ada slave/hp.ada	proc_HBR set_processing reset_hbrstate
HBR_transparent	slave/ht_.ada slave/ht.ada	compute_w_ov compute_tm_ov eof_ih compute_ov get_transparent_data
Main_sci	slave/main.ada slave/ms_.ada slave/ms.ada	main
Sci	slave/sci.asm	read4k maskit getenergy ggetmbxms fid slaveattn hbrinit readword readfast fifoenable resetfifoeof resetfifofull resetfifo

		fifoeof fifofull fifohfull fifoempty
Scientific_computing	slave/sc_.ada	start
Shwsw_if	slave/shwsw_if_.ada slave/shwsw_if.ada	get_lpaddr raise_attn_it FIFOempty FIFOfull FIFOhalffull FIFOeof ResetFIFO ResetFIFOfull ResetFIFOeof FIFOenable set_IV HBR_init
Sih	slave/sih_.ada slave/sih.ada	FIFOfull_ih mastermbx_ih unused13_ih unused11_ih unused10_ih unused08_ih unused02_ih unused00_ih FIFOeof_ih
Ca Ca1	common/ca_.ada common/ca.ada	get_ov_skip set_ov_skip set_sw get_sw get_hbr_th set_hbr_th get_go_cmd set_hbr_bpt get_hbr_bpt get_ov_info set_ov_info set_go_cmd get_hbr_control set_hbr_control set_pattern_id get_pattern_id set_offset_r get_offset_r set_offset_c get_offset_c set_variance get_variance get_scientific_init_report init set_ov_window get_ov_window get_ov_window_ada set_ov_smooth_thresholds get_ov_smooth_thresholds set_ov_factors get_ov_factors set_ov_mode get_ov_mode set_ov_ccd_id get_ov_ccd_id set_ov_ccd_node get_ov_ccd_node

		set_ov_instances get_ov_instances set_ov_ccd_geometry get_ov_ccd_geometry
Hbrb Hbrb1	common/hbrb_.ada common/hbrb.ada common/hbr.asm	set_sizes get_status read_events write_events init
Data_Collector	master/HK/d_colle/d_colle_.ada master/HK/d_colle/d_colle.ada master/HK/d_colle/d_get.ada	Get_Current_Mode Set_Current_Mode Get_Task_Pid Set_Task_Pid init Set_Analog_Channel SetSwitch SetSwitch_Alert SetSwitch_Commanded Set_Events Set_Buffer_Occupation Set_Buffer_Configuration Set_OBT_Reset_Time Set_Filter_Wheel Set_Counting_Time SetArming_Status Set_Refreh_Status Set_HK_Request Get_HK_Data GetData SendData
EMCR_Services	master/HK/emcr_se/emcr_se_.ada master/HK/emcr_se/emcr_se.ada master/HK/emcr_se/er_exec.ada master/HK/emcr_se/er_perio.ada master/HK/emcr_se/er_resp.ada master/HK/emcr_se/er_si_tm.ada master/HK/emcr_se/er_simpl.ada	EMCR_SendQueue Init EMCR_ServicePeriodic EMCR_GetResponse EMCR_HK_GetData EMCR_HK_SendReq EMCR_StopServicies
EMDH_Services	master/HK/emdh_se/emdh_se_.ada master/HK/emdh_se/emdh_se.ada master/HK/emdh_se/eh_perio.ada	Init EMDH_Periodic DumpEMCR ChecksumEMCR DownloadEMCR_Table loadEMDH_table checksumEMDH dumpEMDH dumpEMDH_table UploadEMCR complex_periodic send_complex_FW get_complex_FW
LBR_Protocol	master/HK/lbr_prt/lbr_prt_.ada master/HK/lbr_prt/lbr_prt.ada master/HK/lbr_prt/checksum.ada master/HK/lbr_prt/l_getfr.ada master/HK/lbr_prt/l_init.ada master/HK/lbr_prt/l_period.ada master/HK/lbr_prt/l_sendfr.ada	LBR_SendFrame LBR_GetFrame LBR_Periodic Get_Protocol_Status Init
Switch	master/HK/switch/switch_.ada master/HK/switch/switch.ada	Init Arm Fire Remove On Off

		OnOff Reset ReadSwitch
Synchro	master/HK/synchro/synchro_.ada master/HK/synchro/synchro.ada	Init Wait_synchro Put_synchro Check_synchro
System_Monitoring	master/HK/sys_mon/sys_mon_.ada master/HK/sys_mon/sys_mon.ada	Sys_Mon_Periodic time_verif Set_basic_sw Init
Thermal_Control	master/HK/thr_cnt/thr_cnt_.ada master/HK/thr_cnt/thr_cnt.ada master/HK/thr_cnt/t_perio.ada	init therm_mon_periodic set_thermal_limit get_thermal_limit Set_Thermal_Mode Set_Extraheating_config_Table Get_Extraheating_Config_Table EMCR_Set_Point
TC_CircBuff	master/TC/tc_circ/tccirb_.ada master/TC/tc_circ/tccirb.ada master/TC/tc_circ/getpck.ada master/TC/tc_circ/init_cb.ada master/TC/tc_circ/putpck.ada	Init GetPck PutPck
TC_mng	master/TC/tc_mng/tc_mng_.ada master/TC/tc_mng/tc_mng.ada master/TC/tc_mng/c_apid.ada master/TC/tc_mng/c_checks.ada master/TC/tc_mng/c_header.ada master/TC/tc_mng/c_lenght.ada master/TC/tc_mng/c_verify.ada master/TC/tc_mng/init.ada master/TC/tc_mng/newtc_pr.ada master/TC/tc_mng/tc_p_mng.ada master/TC/tc_mng/tc_valid.ada master/TC/tc_mng/xqt_conf.ada master/TC/tc_mng/xqt_emae.ada master/TC/tc_mng/xqt_mem.ada master/TC/tc_mng/xqt_mode.ada master/TC/tc_mng/xqt_onof.ada master/TC/tc_mng/xqt_resp.ada master/TC/tc_mng/xqt_simp.ada master/TC/tc_mng/xqt_task.ada master/TC/tc_mng/xqt_time.ada master/TC/tc_mng/xqt_tm.ada	Init Periodic_mng newTC_processing
Cast	master/cast/cast_.ada master/cast/cast.ada	i_to_addr PID_to_i i_to_PID b_getbit b_setbit lw_to_w w_to_lw b_to_w w_to_b
Op_modes	master/om_.ada master/om.ada master/oma.asm	get_ift_param slave_attn get_extrah_param set_ift_param set_extrah_param firstssb_start change_mode get_current_mode expected_pixels

TM	master/tm_.ada master/tm.ada master/tma.asm	init read_enable_sid enable_all_sid enable_sid report_all_telemetry_status eotm_processing schedule_pck get_tm_bufstat send_hk send_np send_tcverif send_mem send_sc
Bsw	bsw/bsw.asm	enter_ground_test enter_basic_sw
Crc_bsw	bsw/crc.asm	crc_compute crc_boot crc_byte
Ev	bsw/ev.asm	ev_getnext ev_process ev_init
Exdef	bsw/evdef.inc	
Intr	bsw/intr_mos.asm	intr_init_sel intr_setcallback intr_init
Mem	bsw/mem.asm	mem_checksum mem_check_addressable mem_dump mem_check_loadable mem_load
Memory	bsw/memory.asm	memory_checksum memory_dump memory_load
Mode	bsw/mode.asm	mode_set mode_get
Pkt	bsw/pkt.asm	pkt_init pkt_receive pkt_send
Rbi	bsw/rbi_mos.asm	rbi_get_status rbi_set_running rbi_getitrcmd rbi_hw_init i_to_rbi_isr i_to_user_isr rbi_send_packet rbi_newpackets rbi_init
Uart	bsw/uart.asm	uart_isr uart_send_packet uart_newpackets uart_init
Board_m	Boot_master/board_m.asm	bit_check board_regs_init board_regs_warm_init mbx_read mbx_write usart_init testcable_check
Boot_m	Boot_master/boot_m.asm	cold_restart warm_restart
Bootmem_m	Boot_master/bootmem_m.asm	ram_prg_checksum startprom_checksum

		startprom_load prom_load prom_checksum ram_check ram_clean
Edac_m	Boot_master/edac_m.asm	edac_check_and_enable
Fltrep	Boot_master/fltrep_m.asm	fltrep_store fltrep_regs_to_ram fltrep_ram_to_regs
APEX2	master/p_table_.ada master/p_table.ada master/p_executive.ada master/getctx.asm master/retctx.asm	change_timing get_info suspend request_aperiodic_execution unlock lock set_overrun_attributes unload_aperiodic unload_periodic load_aperiodic load_periodic canc_susp executive
HWSW_IF	master/hwsw_if_.ada master/hwsw_if.ada master/hwsw_ifa.asm	testcablein OBDHstatus resetcurlim setswitch readalert readswitch write resetwrite newchar storechar getchar putchar lbr_charcnt read resetread add_time get_time read_FR1 read_FR2 enable_BCP4 enable_synchro preset_time force_synch_pulse RBI_send_TM set_IV get_lpaddr load_counter enable_counter maskit set_TC_receipt set_OTR watchdog_reset read_TC raise_attn_it read_analog init watchdog_disable
Ih	master/ih_.ada master/ih.ada	LBR_rx_ih LBR_tx_ih syncpls_ih RBI_toRBI_ih

		RBI_touser_ih rtc_ih slave_attn_ih unused00_ih unused14_ih
Main_master	master/main_master.ada	main_master

7.1.2 Memory map

EMDH unit has two microprocessor boards, so the S/W engineers have to take into account that two memory maps are used. Furthermore since the two boards communicate between them by means of the SBUS90 and since the are both visible by the RBI board, a System Memory Map are used.

The memory map of each uProcessor board is arranged as shown by next table (Tab. 7.1.2.-1) and figure (Fig. 7.1.2-1).

Table 7.1.2-1: HPM 31750 General Memory Map

Area	Start Addr.	Size (word)	Notes
START-UP PROM	0	8 or 32 K	Read Only. May be on board or external. Must be enabled by the CPU. May not be present.
High PROM	FE000hex F8000hex	8K 32K	Gives access to the on-board PROM. Read-Write. May not be present. Writing may be inhibited.
RAM	0	32K to 256K in 32K chunks or 128K to 1M in 128K chunks	May be divided in two sub-areas
Expansion	Always after RAM end	64K	May not be present
External	Always after RAM end or Expansion memory end	1M in 1750A mode, 2M in 1750B mode, minus the size of the other areas	From 1 to 2M gives access to the full system bus memory space.

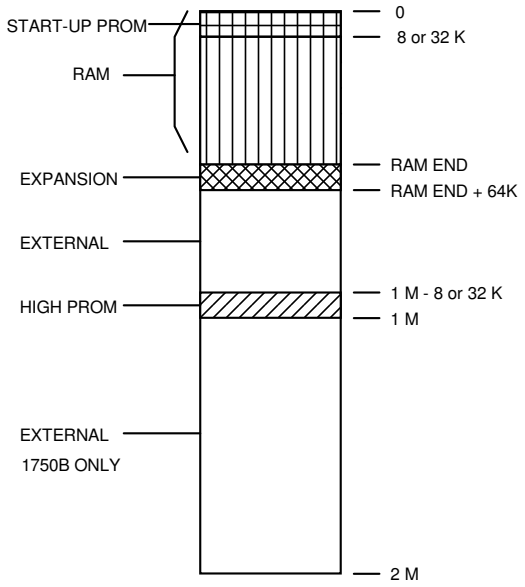


Figure 7.1.2-1: HPM 31750 General Memory Map

As far the physical arrangement of the RAM and PROM memory is concerned, the following figure (Fig. 7.1.2-2) illustrates how the RAM an PROM chips are arranged on EMDH boards.

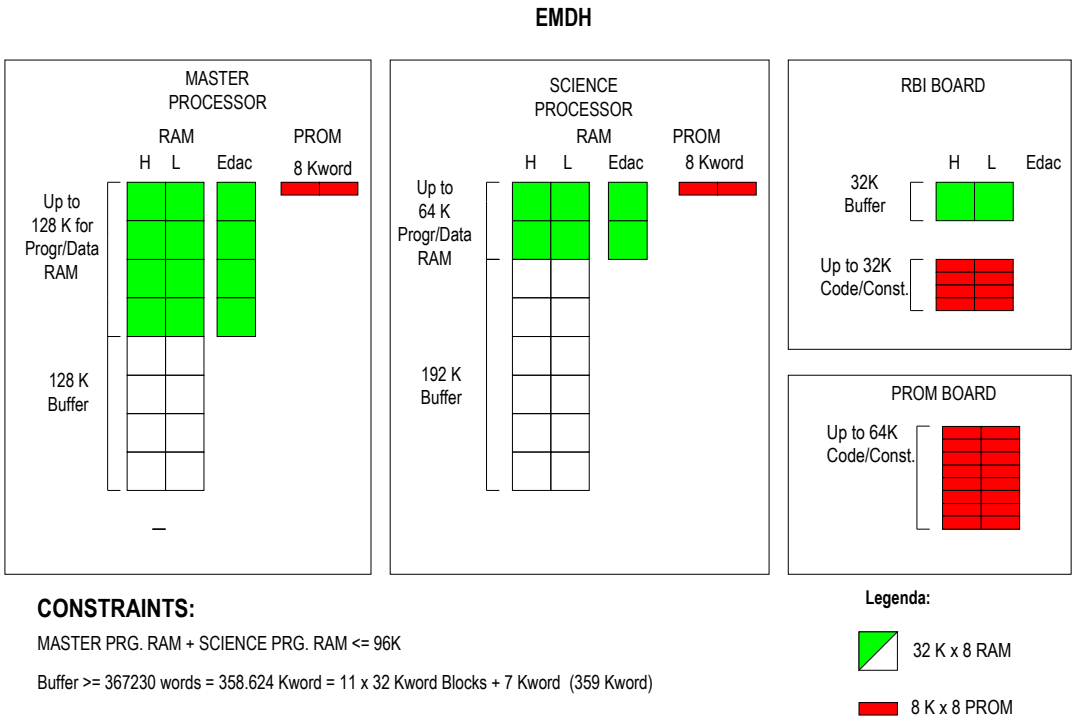


Figure 7.1.2-2 EMDH Physical Memory Arrangement

According to the memory mapping rules stated in EMDH HW/SW Interface document, and reported at the beginning of the chapter, the memory maps for each uProcessor board as well as the System Memory Map are here below shown:

Table 7.1.2-2 Master uProcessor Memory Map

Area	Addr. Range	Size (word)	Notes
START-UP PROM	0 – 02000hex	8K	Read Only.
On Board Memory	0 - 3FFFFhex	256 Kword in chunks of 32K word	Includes: program RAM, Data RAM, RBI I/O Buffers and Science Data Buffer 2
External Memory	4000hex – 8FFFFhex	320K	**Not Addressable Area**. The S/W of this board shall never read or write in this addresses range.
External Memory	90000hex – CFFFFhex	256K	In this range the Master UProc. boards can read-write from/to the Science uProc. Board RAM.
External Memory	D0000hex – DFFFFhex	64K	In this range the Master uProc. board can access the FIFOs of the HBR Board. **Even if this operation is outside the scope of the EMDH architecture**
External Memory	E0000hex – EFFFFhex	64K	In this range the Master uProc. Board can access in read-only mode, the PROM Board.
External Memory	*F0000hex – FDFFFhex*	*56k*	***Not Addressable Area**. The S/W of this board shall never read or write in this addresses range.*
HIGH PROM	*FE000hex – FFFFFhex*	*8k*	*In this range the S/W can asses, in read mode, the content of the Start-Up PROM, regardless the status (Enabled/Disabled) of the Start-Up PROM itself (see relevant CPU I/O commands*
External Memory	*100000hex – 11FFFFhex*	*128K*	***Not Addressable Area**. The S/W of this board shall never read or write in this addresses range.*
External Memory	*120000hex – 127FFFhex*	*32K*	*In this range the Master uProc. board can access the PROM chips housed in the RBI board*
External Memory	*128000hex – 12FFFFhex*	*32K*	*In this range the Master uProc. board can access the RAM chips housed in the RBI board*
External Memory	*130000hex - 1FFFFFhex*	*832K*	***Not Addressable Area**. The S/W of this board shall never read or write in this addresses range.*

Table 7.1.2-3 Science uProcessor Memory Map

Area	Start Addr.	Size (word)	Notes
START-UP PROM	0	8K	Read Only.
On Board RAM	0 - 3FFFFhex	256 Kword in chunks of 32K word	Includes: program RAM, Data RAM and Science Data Buffer 1
Expansion Memory	40000hex - 4FFFFhex	64K	In this range the S/W of the Science uProc. Board can access the **8 HBR FIFOs** in read-only mode. See tab. 4-4a
External Memory	50000hex - 8FFFFhex	256K	In this range the Science uProc. boards can read-write from/to the Master uProc. Board.
External Memory	90000hex – DFFFFhex	320K	**Not Addressable Area.** The S/W of this board shall never read or write in this addresses range.
External Memory	E0000hex – EFFFFhex	64K	In this range the Science uProc. Board can access in read-only mode, the PROM Board.
External Memory	*F0000hex – FDFFFhex*	*56k*	***Not Addressable Area**. The S/W of this board shall never read or write in this addresses range.*
HIGH PROM	*FE000hex – FFFFFhex*	*8k*	*In this range the S/W can asses, in read mode, the content of the Start-Up PROM, regardless the status (Enabled/Disabled) of the Start-Up PROM itself (see relevant CPU I/O commands*
External Memory	*100000hex - 11FFFFhex*	*128K*	***Not Addressable Area**. The S/W of this board shall never read or write in this addresses range.*
External Memory	*120000hex - 127FFFhex*	*32K*	*In this range the Sciebce uProc. board can access the PROM chips housed in the RBI board*
External Memory	*128000hex - 12FFFFhex*	*32K*	*In this range the Science uProc. board can access the RAM chips housed in the RBI board*
External Memory	*130000hex - 1FFFFFhex*	*832K*	***Not Addressable Area**. The S/W of this board shall never read or write in this addresses range.*

Table 7.1.2-4: HBR FIFO Memory Map

Expansion Memory	48000hex - 49FFFhex	8K	Any address in this range address the HBR 1 FIFO
	4A000hex - 4BFFFhex	8K	As above per HBR 2 FIFO
	4C000hex - 4DFFFhex	8K	As above per HBR 3 FIFO
	4E000hex - 4FFFFhex	8K	As above per HBR 4 FIFO
	40000hex - 41FFFhex	8K	As above per HBR 5 FIFO
	42000hex - 43FFFhex	8K	As above per HBR 6 FIFO
	44000hex - 45FFFhex	8K	As above per HBR 7 FIFO
	46000hex - 47FFFhex	8K	As above per HBR 8 FIFO

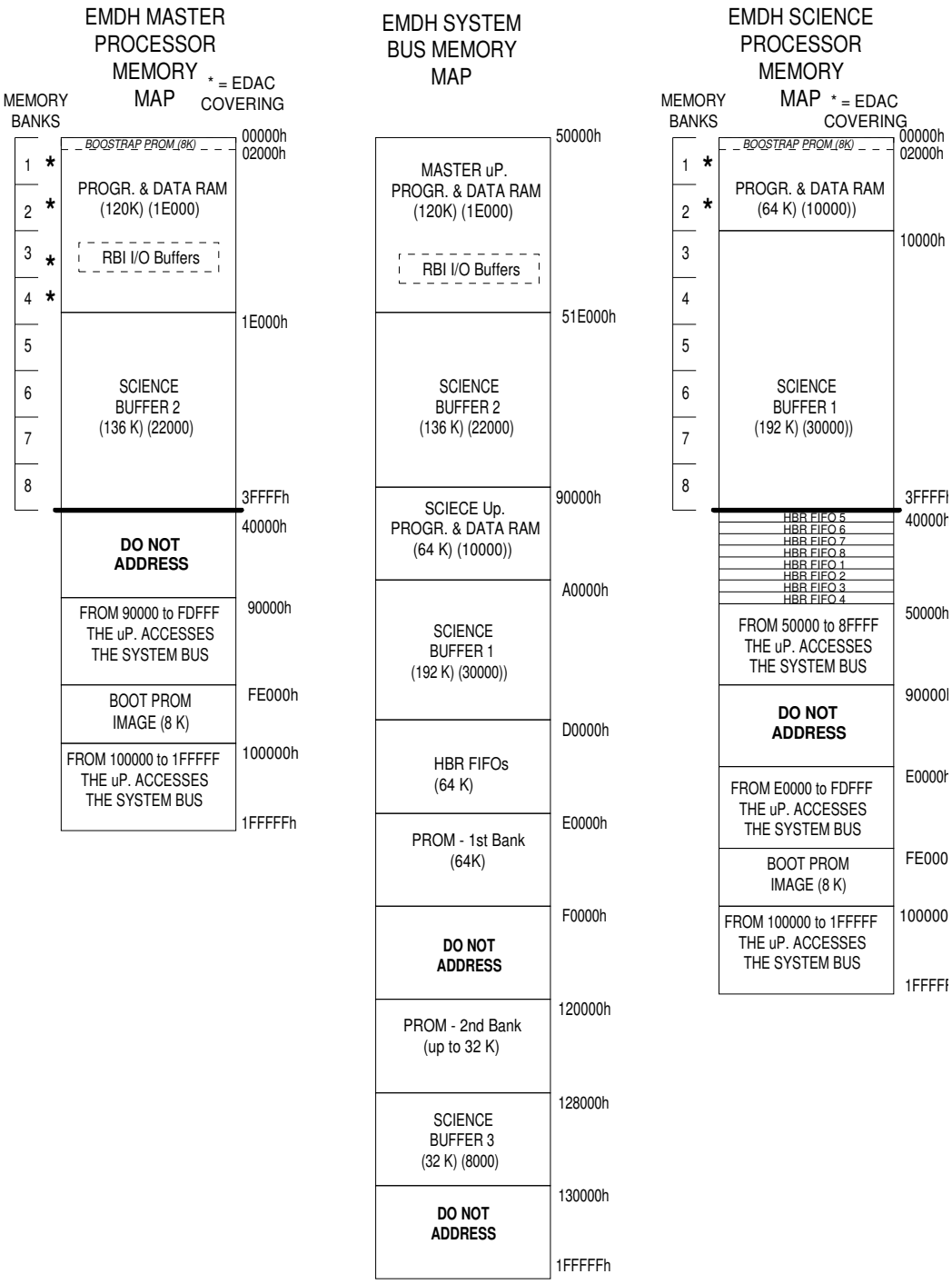


Figure 7.1.2-3: Master uProc, Science uProc. and System Memory Addresses

Details of I/O registers are in EMDH HW/SW Interface document.
For what concerns I/O maps you can find details about Master uProcessor Board, Scientific uProcessor Board, Miscellaneous Board and RBI Board.
Finally details about Interrupts.

7.1.3 Compile, link and load procedures

Code and compile, link, load procedures are organised in a directory tree.
This is the final baseline of the software package SW-A-634 for the EPIC MOS Data Handling Unit (EMDH).

The root contains:

- REVH_baseline list of all files configurated for REV.H with the modifciation from former REV.G
- EQM2FM.delta compared lists of the REV.B delivered with EQM and REV.H delivered with FM
- compile scripts, as used for rebuilding the memory image submitted and validated by system tests:
  - **PreMakeHK PreMakeTC makeHK makeTC makeMaster makeAllmaster** which calls the right sequence of the above scripts to compile the MASTER S/W;
  - **makeFast makeOv** to be used to compile the SLAVE S/W inclusive of the new Offset & Variance algorithm;
  - **makeBoot_m makeBoot_s makeBSW** to be used to assembly the bootstrap PROM code (bootstrap and basic software for master; bootstrap for slave)

  (BEWARE to the working directory which must be ~/baseline/MOS)

- linking directives **main_master.link main_sci.link**
- memory maps; the original ones from working baseline eprom.v10 used for formal acceptance of EMCS: **main_master.map main_sci.map**

SUB-Directories contain:

- *ABS*: contains the *.high *.low to be referenced as master for PROM (master image files contain SW_REVISION=2F00 at D03E) (scient image files contain SW_REVISION=2F00 at 5020) Then it contains the reference files (.high .low .ldm .trb .dbg) as rebuilded and cross-checked with the software in EPROM submitted to EMCS acceptance Moreover they are joined with: *.raw files: to be used for upload software in binary format through TC(6,1) and * eprom.cks.master & slave reporting the SUMCHECKS to be matched during load of EPROM_high and EPROM_low.
- *ABS SUB-Dirs*; bootobj.prom 21 .obj files as used for Start-Up PROM flight
- *eprom.v10.OCT7* contains the reference files (.high .low .ldm .link .map .trb .dbg) of the software in EPROM submitted to acceptance (SW_REVISION=1F06 at D03E for master) (SW_REVISION=1F06 at 5020 for slave)

Note: the commands files start with

```
cd ~/MOS.deliv.H
```

that is current release. If source files are put in other directory, this instruction has to be changed.

7.1.3.1 Compile and link procedure

To compile (from scracth),
Create an Ada Library 1750A/

```
> alm new
```

Check in your work directory the file master/ioaddr.inc

```
> cp -p master/ioaddr.inc
```

For the Master execute the following scripts in this order:

- > makeBoot_m to assembly the bootsrap
- > makeAllMaster to recompile from scratch Ada sources and assembly files. This script uses
  PreMakeHK | tee premakehk.log
  PreMakeTC | tee premaketc.log
  makeHK | tee makehk.log
  makeTC | tee maketc.log
  makeMaster | tee makemaster.log

that handle subparts and poduce the listed log files. Due to relationship among the modules it is a good practice to use makeAllMaster vs. the single steps.

Check no compilation errors by means of the follwing unix command.

```
> grep Error *.log
```

Check the Ada library consistency by means of the command:

```
> alk main_master -no_link -no_map
```

this step is not necessary if no new ada file has been introduced.

Check if the following directory is present in your work-directory (containing *.asm *.obj):./bootobj.prom

Link the obj to produce a *.ldm using the script

```
> lnktld -debug -map -dir=main_master.link
```

where main_master.link contains the linking direcives

Then compile Scientific S/W by executing the following script:

- makeBoot_s to assembly the bootsrap
- makeFast to recompile from scratch Ada sources and assembly files. This script does not use any second level script.

Check no compilation errors by means of the following unix command.

```
> grep Error *.log
```

Check the Ada library consistency by means of the command:

```
> alk main  -no_link -no_map
```

this step is not necessary if no new ada file has been introduced.

Link the obj to produce a *.ldm using the script

```
> lnktld -debug -map -dir=main_sci.link
```

where main_sci.link contains the linking direcives

Produce the prom images like that:

```
> tld2hex
enter filename *.ldm:   main_master.ldm
enter file name: master
enter offset:  0
> tld2hex
enter filename *.ldm:   main_sci.ldm
enter file name: scient
enter offset:  0
```

Note:

the two script that prepare the boot sections assembly *.asm files to be copied in bootobj.prom by using the command

```
tldasm -debug <nomefile>.asm
```

for each one of the asm included in the subdirectory ./Boot_master ./Boot_slave ./bsw. then put output to the bootobj.prom directory by using the command

```
cp  -p *.obj   ../bootobj.prom/
```

7.1.3.2 Loading Software

To load EMDH SW procede as follows:

A. if the EMDH is running.

1. enter Safe Stand.By
2. enter Basic Software
3. load software (master or slave) by using TC(6,1) MID=0 and physical address (32 bit).The BSW will check you do not address RAM where it runs (if this happens, no problems: request a Restart Cold and nothing is lost but changes already done)
4. Restart Warm
5. start ICU with zero
6. good luck

Note: restart ri-inizialise all variables in the Ada sections $DATA$! then anly CONSTANTS are patchable items.

B. if the EMDH is Suspended

By using RBI memory load as usual

Code to be used for patch is to be extracted from LDM file obtained from the TLD linker,cleaning from initial words in every records that are used to lead the loading function as it is carried out by the emulator.The load format description is in the TLD. manuals

Check:

- dump EMDH SW from address 16#1000# (RTX_START) then
- check vs the LDM file

you will get a record with the address plus some side info.

7.2 EMCR SW

7.2.1 Code description

EMCR SW is partitioned in two modules:
- *Boot* and
- *Program*

Boot runs in PROM while *Program* is copied to RAM where it runs. Control is shared between them.(i.e. the first step of command verification, according to SW Status is done by *Boot*)
Boot and *Program* allocate the sw resources according the memory map in Section 4.2 and they share some variables/buffers as common area and some interaction constraints as relationship.
A Functional Diagram summarizes the interconnection of the main tasks.
Beside this to get a complete control of the SW the implemented Interrupt Controller and the mamagement of the Interval Timer must be taken into account.

7.2.1.1 Functions

In the following the set of the SW functions extracted from the code is listed. You can follow the link bound to the name to get:
- a *call tree index* where the structure of the addressed function is detailed with respect to the called functions (i.e.all the dependencies of the current function are listed). Each called function has an entry in the *cross-reference index* (see below) and in the *source index* (see below).
- a *cross refernce index* where all the callers and called funcions bound to the addressed one are listed (i.e. all the interfaced functions are listed). Each addressed function has an entry in the *source index* (see below) and each caller/called has an entry in the *cross refernce index* itself.
- a *source index* where the functions are grouped as source code. Each addressed function has an entry in the *cross refernce index*.
- All these view have a goto section at the top where the others can be selected. An ancillary listing of the functions called *name index*, where the addressed function has an entry in the *source index* and an entry in the *cross refernce index*, has been introduced to avoid to come back to this root index.

EMCR Boot Functions Alphabetical index

Code/source file Relationships	Description	Public Label Global data	Local data
Allow_it_boot			
Background_boot	(add $ 2.1.6)		
Check_stat_uart	(add $ 2.5)		
Checksum	(add $ 2.4.7)		
Crc			
Error_block	(add $ 2.4.6)		
Exec_tc_boot	(add $ 2.4.3)	(add $ 2.4.2)	
Goto_ram	(add $ 2.1.5)		
Init_it_boot	(add $ 2.5)		
Init_timer	(add $ 2.5)		
Init_uart	(add $ 2.5)		
it_parasite	(add $ 2.5)		
it_receive	(add $ 2.2.4)	(add $ 2.2.2)	(add $ 2.2.3)
it_time_out	(add $ 2.2.5)		
it_transmit	(add $ 2.3.5)		

Load_ctr_ram	(add $ 2.4.4)		
Main	(add $ 2.1.5)	(add $ 2.1.2) (add $ 2.1.3)	
Nothing			
Read_ctr_mem	(add $ 2.4.5)		
Read_uart	(add $ 2.5)		
Reset_wdog	(add $ 2.5)		
Start_boot (name)	(add $ 2.1.4)		
Start_to	(add $ 2.5)		
Stop_to	(add $ 2.5)		
Transmit	(add $ 2.3.4)	(add $ 2.3.2)	(add $ 2.3.3)
Write_uart	(add $ 2.5)		

EMCR Program Functions Alphabetical index

Code/source file Relationships	Description	Public Labels Global data	Local data
add_2048			
Allow_it_boot			
Alternate_manage	(add $ 3.2.7)		
Background_boot	(add $ 2.1.6)		
Build_5_lines	(add $ 3.5.3)		
Build_image	(add $ 3.5.3)		
cad_read	(add $ 3.8)		
Check_stat_uart			
Checksum			
Checksum_calc			
Command_emae			
Common_28_29	(add $ 3.3.5)		
Conf_edu			
Conf_seq_mode			
Edge			
edu_fifo	(add $ 3.8)		
edu_read	(add $ 3.8)		
edu_win			
edu_write	(add $ 3.8)		
edu_write_read	(add $ 3.8)		
Emae_er	(add $ 3.8)		
Emae_fifo	(add $ 3.8)		
Error_block			
Exec_tc_ram	(add $ 3.6.1)	(add $ 3.6.1)	(add $ 3.6.1)
Gatti_manage	(add $ 3.2.8)		
HS			
Init_ccd_header	(add $ 3.8)		
init_dma	(add $ 3.8)		
init_header	(add $ 3.8)		
init_tables	(add $ 3.8)		
it_allow	(add $ 3.8)		
it_dma	(add $ 3.8)		
it_dma_disable	(add $ 3.8)		
it_dma_enable	(add $ 3.8)		
it_frame	(add $ 3.8)		
it_frame_0	(add $ 3.8)		
it_frame_1	(add $ 3.8)		

it_frame_2	(add $ 3.8)		
it_frame_3	(add $ 3.8)		
it_frame_4	(add $ 3.8)		
it_frame_5	(add $ 3.8)		
it_frame_6	(add $ 3.8)		
it_frame_7	(add $ 3.8)		
it_frame_disable	(add $ 3.8)		
it_frame_enable	(add $ 3.8)		
it_tic	(add $ 3.2.6)		
it_tic_disable	(add $ 3.8)		
it_tic_enable	(add $ 3.8)		
load_header	(add $ 3.2.3)		
load_offset_edu	(add $ 3.6.6)	(add $ 3.6.6)	(add $ 3.6.6)
load_pattern_edu	(add $ 3.6.7)	(add $ 3.6.7)	(add $ 3.6.7)
load_seq_par	(add $ 3.6.5)	(add $ 3.6.5)	(add $ 3.6.5)
load_threshold_edu			
main_ram	(add $ 3.1.3)	(add $ 3.1.2)	
manage_header	(add $ 3.2.4)		
manage_heating	(add $ 3.4.2)		
manage_hk	(add $ 3.1.4)		
manage_stat_edu	(add $ 3.8)		
manage_tc	(add $ 3.3.6)		
OK			
position_filter_wheel	(add $ 3.3.4)		
read_ctr_mem			
read_offset_edu	(add $ 3.6.3)	(add $ 3.6.3)	(add $ 3.6.3)
read_pattern_edu	(add $ 3.6.2)	(add $ 3.6.2)	(add $ 3.6.2)
read_pattern_ram			
read_seq_emae	(add $ 3.6.4)	(add $ 3.6.4)	(add $ 3.6.4)
reset_wdog			
send_edu_writings	(add $ 3.7.2)		
send_emae_cdes	(add $ 3.7.1)		
send_hsk			
send_runstep			
start_dma	(add $ 3.8)		
start_observation	(add $ 3.2.2)	(add $ 3.2.1)	
start_temp_control	(add $ 3.8)		
start_test_image	(add $ 3.5.2)		
Stop_dma	(add $ 3.8)		
Stop_observation	(add $ 3.2.9)		
Stop_temp_control	(add $ 3.8)		
Stop_test_image	(add $ 3.8)		
Switch_mux_emae			
Sync_filter_wheel	(add $ 3.3.3)	(add $ 3.3.2)	
Transmit			
Unmask			
_ass1			

7.2.1.2 Structures

As we have seen in the function case, for what concerns Structures we have a *call tree index,* a *cross reference index*, a *source index* and a *name index*

EMCR Boot Structures Alphabetical index

In the folowing the set of EMCR Boot structure is listed .Each Item is an entry to Code/source file Relationships.

struct NONAME_1	struct NONAME_2	struct NONAME_3
struct NONAME_4	struct NONAME_5	uchar
Uint	union BUF_DEF	union BUF_DEF Buf
union NONAME_6	union PTR_ADD	union PTR_ADD ptr_boot
union PTR_ADD ptr_ram	union PTR_ADD ptr_rom	union PTR_ADD ptrd
union WB	union WB ack	union WB Exec_report
union WB nb_waited	unsigned char	unsigned int

EMCR Program Structures Alphabetical index

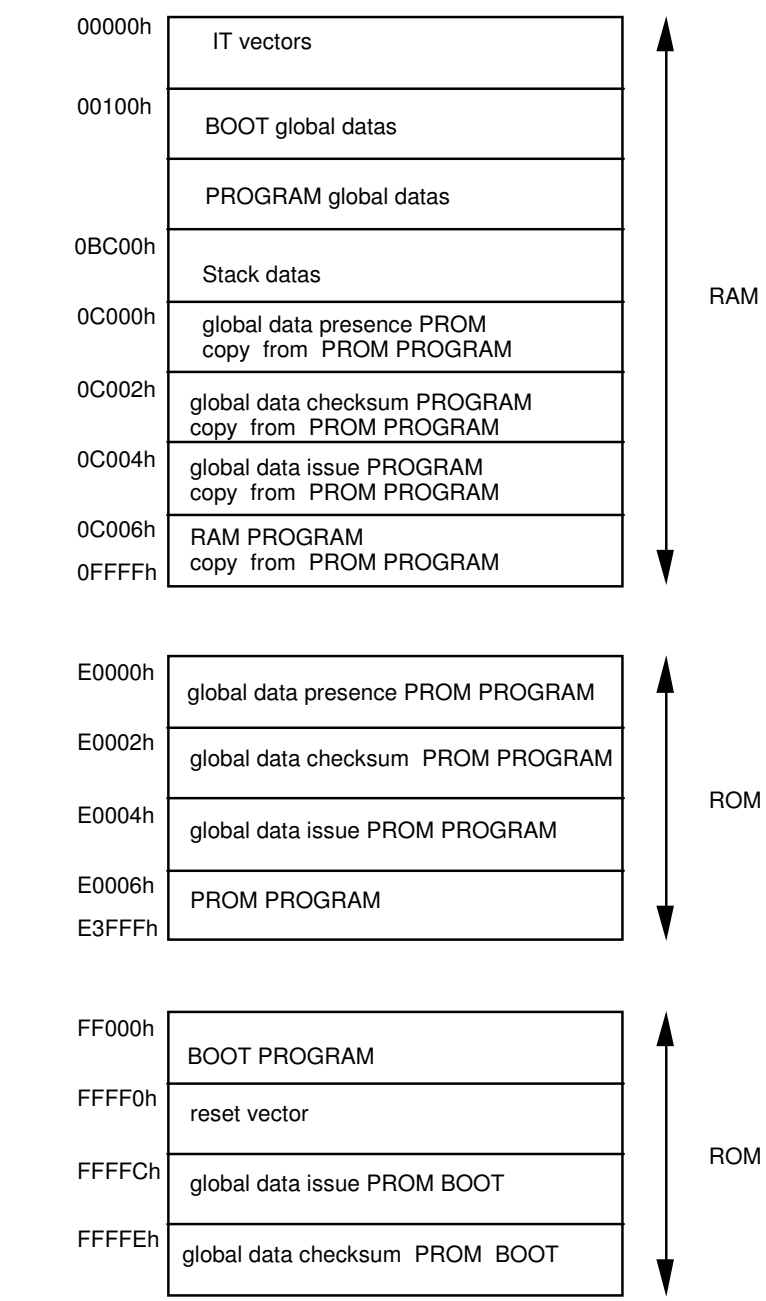
In the following the set of EMCR Program structure is listed .Each Item is an entry to Code/source file Relationships.

struct NONAME_1	struct NONAME_10	struct NONAME_11
struct NONAME_12	struct NONAME_13	struct NONAME_14
struct NONAME_15	struct NONAME_16	struct NONAME_17
struct NONAME_18	struct NONAME_19	struct NONAME_2
struct NONAME_20	struct NONAME_21	struct NONAME_22
struct NONAME_23	struct NONAME_24	struct NONAME_25
struct NONAME_26	struct NONAME_27	struct NONAME_28
struct NONAME_29	struct NONAME_3	struct NONAME_30
struct NONAME_31	struct NONAME_32	struct NONAME_33
struct NONAME_34	struct NONAME_35	struct NONAME_36
struct NONAME_37	struct NONAME_38	struct NONAME_39
struct NONAME_4	struct NONAME_40	struct NONAME_41
struct NONAME_43	struct NONAME_45	struct NONAME_46
struct NONAME_47	struct NONAME_48	struct NONAME_49
struct NONAME_5	struct NONAME_50	struct NONAME_51
struct NONAME_54	struct NONAME_55	struct NONAME_57
struct NONAME_58	struct NONAME_59	struct NONAME_6
struct NONAME_60	struct NONAME_61	struct NONAME_62
struct NONAME_63	struct NONAME_64	struct NONAME_66
struct NONAME_68	struct NONAME_7	struct NONAME_70
struct NONAME_73	struct NONAME_74	struct NONAME_76
struct NONAME_77	struct NONAME_78	struct NONAME_79
struct NONAME_8	struct NONAME_80	struct NONAME_81
struct NONAME_82	struct NONAME_83	struct NONAME_85
struct NONAME_86	struct NONAME_87	struct NONAME_88
struct NONAME_89	struct NONAME_9	struct NONAME_90
struct NONAME_92	struct NONAME_93	struct NONAME_94
uchar	uint	union BUF_DEF
union BUF_HK	union BUF_HK Bhk	union BUF_TC
union NONAME_42	union NONAME_44	union NONAME_52
union NONAME_53	union NONAME_56	union NONAME_65
union NONAME_67	union NONAME_69	union NONAME_71
union NONAME_72	union NONAME_75	union NONAME_84
union NONAME_91	union NONAME_95	union PTR_ADD

union PTR_ADD pbdma	union WB	union WB cde_lsb
union WB cde_msb	union WB cde_r	union WB cde_w
union WB Emae_command	union WB emae_response	union WB load_ad
union WB n_seq	union WB r	unsigned char
unsigned int		

7.2.2 Memory map

EMCR sw memory is used as follows:



7.2.3 Compile, link and load procedure

Files of EMCR SW are organised as fully decribed in chapter 1.3 of UM: see
section 1.3.2 of UM for the Boot Files and
section 1.3.3 of UM for Program files.

The load procedure is in chapter 5 of UM.

In chapter 6 of UM the PROM programmation procedure is shown. It provides:
section 6.2 of UM for the Boot Files and
section 6.3 of UM for Program files.

8. EXPERIMENT TELECOMMANDS AND TELEMETRY

8.1 TELECOMMAND PACKETS LIST AND DESCRIPTION

This paragraph gives the complete list of the telecommand packets available to command the EPCS experiment in all its functions. For each telecommand a detailed description and the list of all the relevant information included in the TLM/TC database are given.

Telecommand Packet List and Description

8.2 TELECOMMANDS PARAMETERS LIST AND DESCRIPTION

This paragraph gives the complete list of the telecommands parameters used in the various telecommand packets. For each telecommand parameter a detailed description and the list of all the relevant information included in the TLM/TC database are given.

Telecommand Parameter List and Description

8.3 TELEMETRY PACKETS LIST AND DESCRIPTION

This paragraph gives the complete list of the telemetry packets available to monitor the EPCS experiment in all its functions. For each telemetry packet a detailed description and the list of all the relevant information included in the TLM/TC database are given.

Telemetry Packet List and Description

8.4 TELEMETRY PARAMETERS LIST AND DESCRIPTION

This paragraph gives the complete list of the telemetry parameters used in the various telemetry packets. For each telemetry parameter a detailed description and the list of all the relevant information included in the TLM/TC database are given.

Telemetry Parameters List and Description

8.5 CONDITIONS LIST AND DESCRIPTION

This paragraph gives the complete list of the conditions used in both telemetry and telecommands definition. For each condition a detailed description and the list of all the relevant information included in the TLM/TC database are given.

Telemetry Parameter Conditions List and Description

8.6 ACRONYMS LIST AND DESCRIPTION

Hereafter the complete list with description of the acronyms used in the above paragraphs to describe the telecommand/telemetry packets and parameters is given:

DATABASE LEGENDA

TC PARAMETERS

PREF	Parameter Reference Number (XOIRD A2.5-3)
NAME	Parameter Name (short)
PTC	Parameter Type Code (XOIRD A2.5-5)
PFC	Parameter Format Code (XOIRD A2.5-5)
WIDTH	Parameter Width in bits
F/V	Flag to show if parameter is fixed or variable: F=FIXED; V=VARIABLE (XOIRD A2.5-8)
UNIT	Parameter engineering unit (XOIRD A2.5-7)
DEFAULT	Default parameter value in engineering units (XOIRD A2.5-9)
MINIMUM	Minimum allowable value in engineering units (XOIRD A2.5-10)
MAXIMUM	Maximum allowable value in engineering units (XOIRD A2.5-10)
MFN	Master Function Number of the TC packets in which the parameter is inserted
ALIAS	Alias Reference Number (A2.5-12)
RAW	Raw value (XOIRD A2.10-4)
MEANING	Text string associated to raw value (XOIRD A2.10-4 and A2.10-5)
CURVE	Calibration Curve Number (XOIRD A2.5-11) and mathematical definition (XOIRD A2.9-4)

TC PACKETS

MF_NO	Master Function Number (XOIRD A2.4-2)
NAME	Packet Name (XOIRD A2.4-5)
TYPE	Packet Type (XOIRD A2.4-8)
STYPE	Packet Subtype (XOIRD A2.4-8)
TID	Task Identifier (XOIRD A2.4-10; PSD sect. 2.3.1, 2.3.2, 2.3.3, 2.3.4)
FID	Function Identifier (XOIRD A2.4-10; PSD sect. 2.3.3, 2.3.4)
MID	Destination Memory (PSD sect. 2.4.1, 2.4.2, 2.4.3,)
MODE	Commanded Mode (PSD sect. 2.3.5)
CATEGORY	Command Category (XOIRD A2.4-7)
CONDITION	Operational Constraints, via Condition Parameter (XOIRD A2.4-13)
CONDITION NAME	Condition Parameter Name (short)
ACC. TIME	Reception Time for TC Acceptance in secs (XOIRD A2.4-15, ICD p.17)
EXEC. TIME	Reception Time for TC Execution in secs (XOIRD A2.4-15, ICD p.17)
VERIF. TIME	Time of Verification of end-effect (ICD p.17)
VERIF. TM PREF	TM Parameter providing end-effect verification (ICD p.17)
TPN	Telemetry packet Number of TM Parameter providing end-effect verification
OFFSET BYTE	Byte Offset in the TM packet of TM Parameter providing end-effect verification (XOIRD A2.6-9)

START BIT	Start bit in the TM packet of TM Parameter providing end-effect verification (XOIRD A2.6-9)
WIDTH	Width in bits of TM Parameter providing end-effect verification (XOIRD A2.6-9)
VERIF. TM VAL.	Value of TM Parameter at end-effect (ICD p.17)
PREC. TC	Preceding Telecommand (XOIRD A2.4-16)
FOLL. TC	Following Telecommand (XOIRD A2.4-16)
ALT. TC	Alternative Telecommand (XOIRD A2.4-16)
RED. TC	Redundant Telecommand (XOIRD A2.4-16)
OPP. TC	Opposite Telecommand (XOIRD A2.4-16)
BYTE	Byte Offset of TC Parameter in the TC Packet (ICD p.16)
BIT	Start Bit of TC Parameter at Byte Offset in the TC Packet (ICD p.17)
W	Parameter Width of Fixed Bit Pattern or Lenght of Variable Parameter
PREF	TC Parameter Reference Number (XOIRD A2.5-3)
NAME	TC Parameter Name (short)
F/V	Flag to show if parameter is fixed or variable: F=FIXED V=VARIABLE (XOIRD A2.5-8)
UNIT	TC Parameter engineering unit (XOIRD A2.5-7)
VALUE	Default TC Parameter Value or Fixed Value (ICD p.17)
MINVAL	Minimum allowed TC Parameter Value (ICD p.17)
MAXVAL	Maximum allowed TC Parameter Value (ICD p.17)
TM VER	TM Verification Parameter of the TC Parameter (ICD p.17)
TPN	Telemetry packet Number of TM Verification Parameter
BYTE	Byte Offset of TM Verification Parameter in packet (XOIRD A2.6-9)
BIT	Start bit of TM Verification Parameter in packet (XOIRD A2.6-9)
WIDTH	TM Verification Parameter width in bits

TM PARAMETERS

PREF	Parameter Reference Number (XOIRD A2.7-3)
NAME	Parameter Name (short)
F/V	Flag to show if parameter is fixed or variable F=FIXED, V=VARIABLE (XOIRD A2.7-8)
UNIT	Parameter engineering unit (XOIRD A2.7-7)
PTC	Parameter Type Code (XOIRD A2.7-6)
PFC	Parameter Format Code (XOIRD A2.7-6)
W	Parameter Width in bits
TC	TC packet (Master Function Number) influencing this parameter (XOIRD A2.7-17)
DEFAULT	Default parameter value in engineering units (XOIRD A2.7-9)
MINIMUM	Minimum allowable value in engineering units (XOIRD A2.7-10)
MAXIMUM	Maximum allowable value in engineering units (XOIRD A2.7-10)
ALT. PAR.	Alternative Parameter (XOIRD A2.7-21)
RED. PAR.	Redundant Parameter (XOIRD A2.7-21)
COND.	Conditioned Parameter Ref.Number which indicates that TM Para is valid or not
TM PKT	Telemetry Packet Number of the TM packets in which the parameter is inserted

CURVE	Calibration Curve Number (XOIRD A2.7-11) and mathematical definition (XOIRD A2.9-4)
ALIAS	Alias Reference Number (XOIRD A2.7-13)
RAW	Raw value (XOIRD A2.10-4)
MEANING	Text string associated to raw value (XOIRD A2.10-4 and A2.10-5)

TM PACKETS

TPN	Telemetry Packet Number (XOIRD A2.6-2)
NAME	Packet Name (XOIRD A2.6-5)
APID	Application ID (XOIRD A2.6-3)
TYPE	Packet Type (XOIRD A2.6-7)
STYPE	Packet Subtype (XOIRD A2.6-7)
TID	Task Identifier (PSD sect. 3.5.1)
FID	Function Identifier (PSD sect. 3.5.1)
MID	Memory Identifier (PSD sect. 3.6.2 and 3.6.3)
SID	Packet Structure Identifier (XOIRD A2.6-8)
TIME FLAG	Time field in Data Field Header. Y=PRESENT, N=ABSENT (XOIRD A2.6-18)
SOURCE	Packet Source (Unit) (XOIRD A2.6-4)
ERROR CODE	Error Code (ICD p.20)
ERROR FLAG	Error Flag (ICD p.20)
PERIODIC PKT CONDITION	Condition Parameter describing the Operational Conditions when periodic packet generation is possible (XOIRD A2.6-11)
APERIODIC PKT CONDITION	Condition Parameter describing the Operational Conditions when non-periodic packet generation is possible (XOIRD A2.6-12)
PERIOD	Packet generation Interval (in ms), for periodic packets only (XOIRD A2.6-10)
BYTE	Byte Offset of the TM parameter in the TM packet (XOIRD A2.6-9)
BIT	Start bit of the TM parameter in the TM packet (XOIRD A2.6-9)
WIDTH	TM Parameter width in bits
PREF	TM Parameter Reference Number (XOIRD A2.6-9)
NAME	TM Parameter Name (short)
F/V	Fix /variable status of TM parameter
UNIT	TM Parameter Unit (XOIRD A2.7-7)
VALUE	Value field for fix bit pattern parameters (as INT, max. 5 long)
MINVAL	Minimum allowable value in engineering units (XOIRD A2.7-10)
MAXVAL	Maximum allowable value in engineering units (XOIRD A2.7-10)
TCMFN	TC packet (Master Function Number) influencing this TM parameter (XOIRD A2.7-17)

9. EXPERIMENT OPERATION PROCEDURES

9.1 General consideration

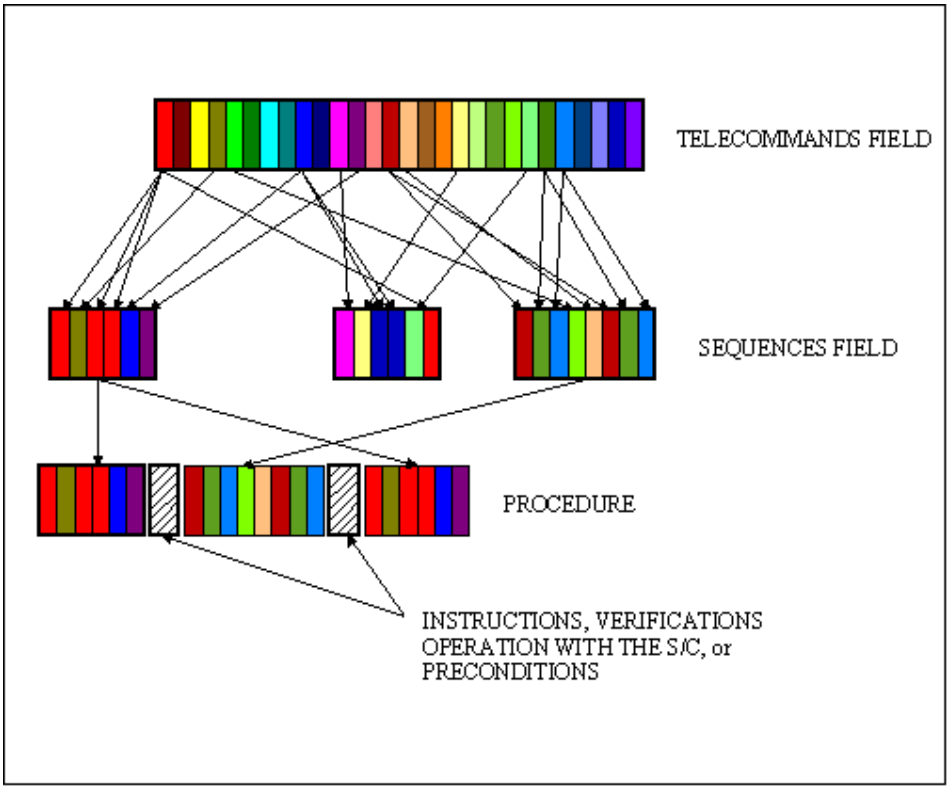
The EMCS is an experiment allowing different modes of operations, as described in the previous paragraph and can be configured, on the same mode, in different configuration.

The Full Window mode can be configured for reading from one node, or from the redunded mode or from both, just as example.

That means that the relatively high flexibility of the system required a relevant high number of telecommands and parameters which allow to built a procedure to be executed during the early phase or during operations.

Each procedure can be built using directly the sequence of telecommands but, considering that the number of procedures to be executed are relatively high, due to the crossing between different options in the modes, an approach which use predefined sequences of telecommands to built the procedures, has been adopted.

Herafter is described the approach used.



The experiment is driven by telecommands which, all togheter, constitutes the Fields of the Telecommands.

A defined list ofTelecommands, extracted by the whole Telecommands Field, consitutes a Sequence which allow for a predefined operation.
Operation which could be, for istance, the opening the venting valve or the configuration of the system for an observation in full frame mode with the main node.

A list of sequences consitute a procedure which define the full set of telecommand to settle the EMCS for an observation or for an engineering task.

9.2 Telecommands list

The list of telecommands is available in the relevant chapter 8.1

9.3 Sequences list

The full list of the available sequences is available in the EMCS command procedures document. Hereafter the main sequences are listed.

9.3.1 Scientific Sequences

9.3.1.1 IMAGING

Full Frame
Offset and Variance Full Frame
Transparent Imaging Full Frame

9.3.1.2 TIMING

Timing
Offset and Variance
Trasparent

9.3.2 Engineering Sequences

Venting Valve Operation
Door Operation
Switch On Nominal Chain
Switch On Redundant Chain
Synchronise the Filter Wheel
Move Filter Wheel in Open Position
Move Filter Wheel in Postions 1,2,3,4,5,0 and Cal
Main Configuration

9.4 COMMISSIONING PROCEDURES

9.4.1 Introduction

In the following sections the activities planned for the XMM Commissioning Phase are outlined. They are identified with the same code used by ESA in the XMM Commissioning Phase Plane. For each activity, the relevant procedure is defined, when possible, with reference to the command sequences and building blocks described in the EMCS command procedures document.
Note that all the activities and database references are relevant to the EMCS1 chain: for the EMCS2 one, the corresponding items must be considered.

9.4.2 EM1COMM01

Description: EPIC-MOS1 initial switch-on, pressure monitoring & venting valve operations and assessment of the door clamping integrity. This activity is also required to be executed during LEOP (TBC) to periodically monitor the clamping bellows pressure. The instrument internal door is closed. A detailed description of the involved steps is provided here below:

- Switch-on the prime section of the experiment.
- Wait for the Initialization Log TM packet (30005)
- Wait for the FW Not Closed Report (30015), with the following parameter status:

TM_PREF	TM_PARA_NAME	VALUE
E1254	H FW NominalStop	0 (In Position)
E1257	H FW Position	0 (Open)
E1258	H FW Redund Stop	0 (In Position)

- In the EMCS Periodic H/K TM packet (30001), check the following parameter status:

TM_PREF	TM_PARA_NAME	VALUE	Switch-on checks
E1001	D Prim PW Consum	0.4 A ± 10 %	0.3 – 0.6
E1004	D +5 V PW Supply	5.2 V ± 5 %	4.7 – 5.3
E1005	D DBU Power +6V	6.1 V ± 5 %	5.4 – 6.6
E1006	D +15V PW Supply	14.7 V ± 5 %	13.5 – 16.5
E1007	D -15V PW Supply	-15.1 V ± 5 %	-16.5 – -13.5
E1008	G EMCS Oper Mode	0 (Safe Stand-by)	0 (Safe Stand-by)
E1009	G EMCS Status	0 (Valid Mode)	0 (Valid Mode)
E1010	D Door HOP Stat.	0 (OFF)	
E1011	D Ven Val HOP St	0 (OFF)	
E1012	D FW Coil 1 Stat	0 (OFF)	
E1013	D FW Coil 2 Stat	0 (OFF)	
E1014	D Ann Heater St.	0 (OFF)	
E1015	D Shr Heater St.	0 (OFF)	
E1076	C EMAE -6 V Line	- 6.1 V ± 5 %	-6.3 – -5.7
E1077	C EMAE +6 V Line	6 V ± 5 %	5.7 – 6.3
E1078	C EMAE -13V Line	- 13.1 V ± 5 %	-13.7 – -12.3
E1079	C EMAE +13V Line	13.1 V ± 5 %	12.3 – 13.7

E1080	C EMAE +28V Line	27.7 V ± 5 %	25.6 – 29.4
E1081	C EMAE +18V Line	17.9 V ± 5 %	17.1 – 18.9
E1082	C Signal Ground	- 0.04 V ± 5 %	-0.1 – 0.1
E1083	C EMAE +32V Line	27 V ± 5 %	24.3 – 29.7
E1086	C EMCR +5 V Line	5.1 V ± 5 %	4.7 – 5.3
E1088	C EMCR -13V Line	- 13.1 V ± 5 %	-13.7 – -12.3
E1089	C EMCR +13V Line	13.1 V ± 5 %	12.3 – 13.7

- Wait until each experiment unit is inside its operational temperature range, by reading the following TM Parameters:

TM_PREF	TM_PARA_NAME
E1002	D P.S. Temp #1
E1003	D P.S. Temp #2
E1084	V EMVC Temp. #1
E1085	C EMCR Temp. #1
E1087	V EMVC Temp. #2
E1090	C EMCR Temp. #2

When this happen switch-off the relevant unit substitution heater.

- Send the TC Enter IDLE Mode.
- Send the TCs included in the EMDH Time Synchronization block.
- Send the TC Sensors On/Off (E102), with the following parameter setting:

PREF	PARA_NAME	VALUE
E128	AnnHeaterRelaySt	0 (OFF)
E129	VacuumSensorStat	1 (ON)
E130	RedThermContrSt	0 (OFF)
E131	NomThermContrSt	1 (ON)

- In the EMCS Periodic H/K TM packet (30001), check the following parameter status:

TM_PREF	TM_PARA_NAME	VALUE
E1255	HDoorBellowState	0 (Retracted)
E1256	H Door Open uSw	1 (closed)
E1261	H Vacuum Monitor	Note 1
E1265	HDoorBellowPress	> 3.5 Bar (Note 2)

Note 1: For MOS1 chain, the vacuum monitor E1261 must be lower than 7000 mV (corresponding to 10 mB); for MOS2 chain, due to the existing vacuum leakage, it is expected to have about 1 B, which cannot be measured by the vacuum monitor K1261.
Note 2: 3.5 Warning limit, 2 Alarm limit and no-go criterium.

- Calculate the EMDH Memory Checksum
- In the TM packet EMDH Memory Checksum (30031), check that the Checksum value is TBD.
- Repeat for 30 times the Venting Valve operation block.
- Switch-off the experiment.

9.4.3 EM1COMM02

Description: EPIC-MOS-1 switch-on (nominal branch) and first part of functional check-out; the instrument internal door is closed. This test is derived from the instrument IST activity and also exercised during SVT's. For the execution of this test the EMCR On Board SW version V11 (in PROM) will be used.
A detailed description of the involved steps is provided here below:

- Switch-on the prime section of the experiment.
- Wait for the Initialization Log TM packet (30005)
- Wait for the FW Not Closed Report (30015), with the following parameter status:

TM_PREF	TM_PARA_NAME	VALUE
E1254	H FW NominalStop	0 (In Position)
E1257	H FW Position	0 (Open)
E1258	H FW Redund Stop	0 (In Position)

- In the EMCS Periodic H/K TM packet (30001), check the following parameter status:

TM_PREF	TM_PARA_NAME	VALUE
E1001	D Prim PW Consum	0.4 A ± 10 %
E1004	D +5 V PW Supply	5.2 V ± 5 %
E1005	D DBU Power +6V	6.1 V ± 5 %
E1006	D +15V PW Supply	14.7 V ± 5 %
E1007	D -15V PW Supply	-15.1 V ± 5 %
E1008	G EMCS Oper Mode	0 (Safe Stand-by)
E1009	G EMCS Status	0 (Valid Mode)
E1010	D Door HOP Stat.	0 (OFF)
E1011	D Ven Val HOP St	0 (OFF)
E1012	D FW Coil 1 Stat	0 (OFF)
E1013	D FW Coil 2 Stat	0 (OFF)
E1014	D Ann Heater St.	0 (OFF)
E1015	D Shr Heater St.	0 (OFF)
E1076	C EMAE -6 V Line	- 6.1 V ± 5 %
E1077	C EMAE +6 V Line	6 V ± 5 %
E1078	C EMAE -13V Line	- 13.1 V ± 5 %
E1079	C EMAE +13V Line	13.1 V ± 5 %
E1080	C EMAE +28V Line	27.7 V ± 5 %
E1081	C EMAE +18V Line	17.9 V ± 5 %
E1082	C Signal Ground	- 0.04 V ± 5 %
E1083	C EMAE +32V Line	27 V ± 5 %
E1086	C EMCR +5 V Line	5.1 V ± 5 %
E1088	C EMCR -13V Line	- 13.1 V ± 5 %
E1089	C EMCR +13V Line	13.1 V ± 5 %

- Wait until each experiment unit is inside its operational temperature range, by reading the following TM Parameters:

TM_PREF	TM_PARA_NAME
E1002	D P.S. Temp #1

E1003	D P.S. Temp #2
E1084	V EMVC Temp. #1
E1085	C EMCR Temp. #1
E1087	V EMVC Temp. #2
E1090	C EMCR Temp. #2

When this happen switch-off the relevant unit substitution heater.

- Execute the Switch-on procedure from step 4 to step 9.
- Turn the FW (MOS1) to Filter A position
- Turn the FW (MOS1) to Filter B position
- Turn the FW (MOS1) to Filter C position
- Turn the FW (MOS1) to Filter D position
- Turn the FW (MOS1) to Open position

9.4.4 EM1COMM03

Description: Second part of EPIC-MOS-1 functional check; the instrument internal door is closed. This test is derived from the instrument IST activity and also partially exercised during SVT's. The CCD's are expected to be at a temperature of -100 °C. For the execution of this test the EMCR On Board SW version V11 (in PROM) will be used.
A detailed description of the involved steps is provided here below:

- Calculate the EMCR Memory Checksum
- In the TM packet EMCR Memory Checksum (30032), check that the Checksum value is TBD.
- Execute the Switch-on procedure from step 10 to step 15.
- Turn the FW to Open Calibration position
- Execute the Full-Frame procedure from step 1 to step 8.
- Execute the HBR1 transparent and the Enter Diagnostic FF blocks
- Execute the HBR3 transparent and the Enter Diagnostic FF blocks
- Execute the HBR4 transparent and the Enter Diagnostic FF blocks
- Execute the HBR5 transparent and the Enter Diagnostic FF blocks
- Execute the HBR6 transparent and the Enter Diagnostic FF blocks
- Execute the HBR7 transparent and the Enter Diagnostic FF blocks
- Execute the HBR8 transparent and the Enter Diagnostic FF blocks
- Execute the Full-Frame procedure from step 9 to step 33.
- Turn the FW (MOS1) to Open position

9.4.5 EM1COMM04

Description: Third part of EPIC-MOS-1 functional check-out; the instrument internal door is closed. The CCD's are expected to be at a temperature of -100 °C. For the execution of this test the EMCR On Board SW version V14 will be uplinked and used.
A detailed description of the involved steps is provided here below:

- Send the TC Enter Safe Stand-by mode (E1).
- Execute the Switch-on procedure from step 2 to step 3.
- Wait that the EMCR Memory Dump is completed and check it.
- Send the TC Enter IDLE Mode.
- Turn the FW (MOS1) to Open Calibration position
- Execute the EDU Peripheral CCDs block.
- Execute the Full-Frame procedure from step 3 to step 33.
- Turn the FW (MOS1) to Open position

9.4.6 EM1COMM05

Description: EPIC-MOS1/2 functional check of all operating modes and measurement/assessment of CCD's functionality. For each mode offset & variance are evaluated and transmitted to ground for comparison with ground test results. The test is executed with the instrument door closed.
A detailed description of the involved steps is provided here below:

- Turn the FW (MOS1) to Open Calibration position
- Execute the Full-Frame procedure from step 3 to step 33, including what reported in note 1 for the Threshold configuration: the observation will take 1 h.
- Repeat the Full-Frame procedure from step 3 to step 33 (now without threshold configuration): the observation will take 1 h.
- Execute the Large Window procedure from step 1 to step 33: the observation will take 1 h.
- Execute the Small Window procedure from step 1 to step 33: the observation will take 1 h.
- Execute the Timing procedure from step 1 to step 33: the observation will take 1 h.
- Execute the Full Frame Double Node procedure from step 1 to step 36: the observation will take 1 h.
- Execute the Large Window Free Run procedure from step 1 to step 33: the observation will take 1 h.
- Execute the Small Window Free Run procedure from step 1 to step 33: the observation will take 1 h.
- Execute the Refreshed Frame Store procedure from step 1 to step 33: the observation will take 1 h.
- Turn the FW (MOS1) to Open position

9.4.7 EM1COMM06

Description: Configure EPIC-MOS1 to safe status (until internal door opening). This activity will be executed at the end of EM1COMM05. Venting valve operations will be executed in parallel on both EPIC-MOS1 & 2.
A detailed description of the involved steps is provided here below:

- Repeat for 30 times the Venting Valve operation block.
- Set the thermal control to 0 °C for 30 minutes.

9.4.8 EM1COMM07

Description: EPIC-MOS1 internal door opening: preparation activity & execution.
A detailed description of the involved steps is provided here below:

- Execute the Enter Idle telecommand.
- In the HK TM packet (30001), check the following status of the FW:

TM_PREF	TM_PARA_NAME	VALUE
E1254	H FW NominalStop	0 (In Position)
E1257	H FW Position	0 (Open)
E1258	H FW Redund Stop	0 (In Position)

If the above check fails, turn the FW (MOS1) to Open position and repeat the check.

- Execute the Door opening block.
- In the HK TM packet (30001), check the following status of the Door:

TM_PREF	TM_PARA_NAME	VALUE
E1255	HDoorBellowState	0 (Retracted)
E1256	H Door Open uSw	0 (Open)
E1261	H Vacuum Monitor	-
E1265	HDoorBellowPress	0 Bar

- Set the thermal control to 30 °C for 30 minutes.

9.4.9 EM1COMM08

Description: EPIC-MOS1 decontamination period (at least 48 h) following internal door internal door opening.
A detailed description of the involved steps is provided here below:

- Stay for 48 hours at +30 °C in Extraheating mode

9.4.10 EM1COMM09

Description: EPIC-MOS1 cool-down following internal door internal door opening and subsequent decontamination period.
A detailed description of the involved steps is provided here below:

- Execute the Enter Idle telecommand.
- Perform the Thermal Control Setting to -100 °C.

9.4.11 EM1COMM10

Description: First part of EPIC-MOS1 operating modes functional check with internal door open. This test also foresees a preliminary estimate of the EPIC-MOS1 bore-sight alignment.
A detailed description of the involved steps is provided here below:

- Slew to the selected target
- Move the Filter Wheel to the required position
- Execute the Fast Diagnostic Setup for all CCDs
- Execute the Full-Frame procedure from step 3 to step 6, including what reported in note 1 for the Threshold configuration
- Execute the EDU all CCDs Fast Diagnostic setup.
- Execute the HBR1 transparent and the Enter Fast Diagnostic FF blocks
- Execute the HBR3 transparent and the Enter Fast Diagnostic FF blocks
- Execute the HBR4 transparent and the Enter Fast Diagnostic FF blocks
- Execute the HBR5 transparent and the Enter Fast Diagnostic FF blocks
- Execute the HBR6 transparent and the Enter Fast Diagnostic FF blocks
- Execute the HBR7 transparent and the Enter Fast Diagnostic FF blocks
- Execute the HBR8 transparent and the Enter Fast Diagnostic FF blocks
- Execute the Switch-on procedure from step 13 to step 15.
- Execute steps 1-2 and 7-33 of the Full-Frame procedure, including what reported in note 1 for the Threshold configuration: the observation will take 1 h.
- Move the Filter Wheel to the required position
- Execute the Fast Diagnostic Setup for all CCDs
- Execute the Full-Frame procedure from step 3 to step 6
- Execute the EDU all CCDs Fast Diagnostic setup.
- Execute the HBR1 transparent and the Enter Fast Diagnostic FF blocks
- Execute the HBR3 transparent and the Enter Fast Diagnostic FF blocks
- Execute the HBR4 transparent and the Enter Fast Diagnostic FF blocks
- Execute the HBR5 transparent and the Enter Fast Diagnostic FF blocks
- Execute the HBR6 transparent and the Enter Fast Diagnostic FF blocks
- Execute the HBR7 transparent and the Enter Fast Diagnostic FF blocks
- Execute the HBR8 transparent and the Enter Fast Diagnostic FF blocks
- Execute the Switch-on procedure from step 13 to step 15.
- Execute steps 1-2 and 7-33 of the Full-Frame procedure: the observation will take 1 h.
- Move the Filter Wheel to the required position
- Execute the Large Window procedure from step 1 to step 33: the observation will take 1 h.
- Move the Filter Wheel to the required position
- Execute the Small Window procedure from step 1 to step 33: the observation will take 1 h.
- Move the Filter Wheel to the required position
- Execute the Timing procedure from step 1 to step 33: the observation will take 1 h.
- Move the Filter Wheel to the required position
- Execute the Fast Diagnostic Setup for all CCDs
- Execute the Full-Frame procedure from step 3 to step 6, including what reported in note 1 for the Threshold configuration.
- Execute the EDU all CCDs Fast Diagnostic setup.
- Execute the HBR1 transparent and the Enter Fast Diagnostic FF blocks

- Execute the HBR3 transparent and the Enter Fast Diagnostic FF blocks
- Execute the HBR4 transparent and the Enter Fast Diagnostic FF blocks
- Execute the HBR5 transparent and the Enter Fast Diagnostic FF blocks
- Execute the HBR6 transparent and the Enter Fast Diagnostic FF blocks
- Execute the HBR7 transparent and the Enter Fast Diagnostic FF blocks
- Execute the HBR8 transparent and the Enter Fast Diagnostic FF blocks
- Execute the Switch-on procedure from step 13 to step 15.
- Execute steps 1-2 and 7-33 of the Full-Frame procedure, including what reported in note 1 for the Threshold configuration: the observation will take 1 h.

9.4.12 EM1COMM11

Description: Second part of EPIC-MOS1 operating modes functional check with internal door open. This test also foresees a preliminary estimate of the MOS/OM bore-sight alignment.
A detailed description of the involved steps is provided here below:

- Slew to the selected target
- Move the Filter Wheel to the required position
- Execute the Fast Diagnostic Setup for all CCDs
- Execute the Full-Frame procedure from step 3 to step 6, including what reported in note 1 for the Threshold configuration
- Execute the EDU all CCDs Fast Diagnostic setup.
- Execute the HBR1 transparent and the Enter Fast Diagnostic FF blocks
- Execute the HBR3 transparent and the Enter Fast Diagnostic FF blocks
- Execute the HBR4 transparent and the Enter Fast Diagnostic FF blocks
- Execute the HBR5 transparent and the Enter Fast Diagnostic FF blocks
- Execute the HBR6 transparent and the Enter Fast Diagnostic FF blocks
- Execute the HBR7 transparent and the Enter Fast Diagnostic FF blocks
- Execute the HBR8 transparent and the Enter Fast Diagnostic FF blocks
- Execute the Switch-on procedure from step 13 to step 15.
- Execute steps 1-2 and 7-33 of the Full-Frame procedure, including what reported in note 1 for the Threshold configuration: the observation will take 1 h.
- Move the Filter Wheel to the required position
- Execute the Fast Diagnostic Setup for all CCDs
- Execute the Full-Frame procedure from step 3 to step 6
- Execute the EDU all CCDs Fast Diagnostic setup.
- Execute the HBR1 transparent and the Enter Fast Diagnostic FF blocks
- Execute the HBR3 transparent and the Enter Fast Diagnostic FF blocks
- Execute the HBR4 transparent and the Enter Fast Diagnostic FF blocks
- Execute the HBR5 transparent and the Enter Fast Diagnostic FF blocks
- Execute the HBR6 transparent and the Enter Fast Diagnostic FF blocks
- Execute the HBR7 transparent and the Enter Fast Diagnostic FF blocks
- Execute the HBR8 transparent and the Enter Fast Diagnostic FF blocks
- Execute the Switch-on procedure from step 13 to step 15.

- Execute steps 1-2 and 7-33 of the Full-Frame procedure: the observation will take 1 h.
- Move the Filter Wheel to the required position
- Execute the Full Frame Double Node procedure from step 1 to step 36: the observation will take 1 h.
- Move the Filter Wheel to the required position
- Execute the Large Window Free Run procedure from step 1 to step 33: the observation will take 1 h.
- Move the Filter Wheel to the required position
- Execute the Small Window Free Run procedure from step 1 to step 33: the observation will take 1 h.
- Move the Filter Wheel to the required position
- Execute the Fast Diagnostic Setup for all CCDs
- Execute the Full-Frame procedure from step 3 to step 6
- Execute the EDU all CCDs Fast Diagnostic setup.
- Execute the HBR1 transparent and the Enter Fast Diagnostic FF blocks
- Execute the HBR3 transparent and the Enter Fast Diagnostic FF blocks
- Execute the HBR4 transparent and the Enter Fast Diagnostic FF blocks
- Execute the HBR5 transparent and the Enter Fast Diagnostic FF blocks
- Execute the HBR6 transparent and the Enter Fast Diagnostic FF blocks
- Execute the HBR7 transparent and the Enter Fast Diagnostic FF blocks
- Execute the HBR8 transparent and the Enter Fast Diagnostic FF blocks
- Execute the Switch-on procedure from step 13 to step 15.
- Execute steps 1-2 and 7-33 of the Refreshed Frame Store procedure: the observation will take 1 h.
- Move the Filter Wheel to the required position
- Execute the Fast Diagnostic Setup for all CCDs
- Execute the Full-Frame procedure from step 3 to step 6, including what reported in note 1 for the Threshold configuration
- Execute the EDU all CCDs Fast Diagnostic setup.
- Execute the HBR1 transparent and the Enter Fast Diagnostic FF blocks
- Execute the HBR3 transparent and the Enter Fast Diagnostic FF blocks
- Execute the HBR4 transparent and the Enter Fast Diagnostic FF blocks
- Execute the HBR5 transparent and the Enter Fast Diagnostic FF blocks
- Execute the HBR6 transparent and the Enter Fast Diagnostic FF blocks
- Execute the HBR7 transparent and the Enter Fast Diagnostic FF blocks
- Execute the HBR8 transparent and the Enter Fast Diagnostic FF blocks
- Execute the Switch-on procedure from step 13 to step 15.
- Execute steps 1-2 and 7-33 of the Full-Frame procedure, including what reported in note 1 for the Threshold configuration: the observation will take 1 h.

9.4.13 EM1COMM12

Description: EPIC-MOS1 decontamination period (48 h) following completion of the Commissioning Phase.

A detailed description of the involved steps is provided here below:

- Turn the FW to Open position
- Set the thermal control to 30 °C.
- Stay for 48 hours at +30 °C in Extraheating mode

9.4.14 EM1COMM13

Description: EPIC-MOS1 cool-down following decontamination period at the end of Commissioning Phase.
A detailed description of the involved steps is provided here below:

- Execute the Enter Idle telecommand.
- Perform the Thermal Control Setting to -100 °C.
- Wait for CCD cool-down

9.5 Health Check & LEOP procedure

The following procedure outlines all the operations to be performed in order to check the health status of the EPIC MOS camera. Note that all the activities and database references are relevant to the EMCS1 chain, unless otherwise indicated: for the EMCS2 one, the corresponding items must be considered.

- Switch-on the prime section of the experiment.
- Wait for the Initialization Log TM packet (30005)
- Wait for the FW Not Closed Report (30015), with the following parameter status (note that these parameters are also included in the regular H/K):

TM_PREF	TM_PARA_NAME	VALUE
E1254	H FW NominalStop	0 (In Position)
E1257	H FW Position	0 (Open)
E1258	H FW Redund Stop	0 (In Position)

- In the EMCS Periodic H/K TM packet (30001), check the following parameter status:

TM_PREF	TM_PARA_NAME	VALUE	Switch-on checks
E1001	D Prim PW Consum	0.4 A ± 10 %	0.3 – 0.6
E1004	D +5 V PW Supply	5.2 V ± 5 %	4.7 – 5.3
E1005	D DBU Power +6V	6.1 V ± 5 %	5.4 – 6.6
E1006	D +15V PW Supply	14.7 V ± 5 %	13.5 – 16.5
E1007	D -15V PW Supply	-15.1 V ± 5 %	-16.5 – -13.5
E1008	G EMCS Oper Mode	0 (Safe Stand-by)	0 (Safe Stand-by)
E1009	G EMCS Status	0 (Valid Mode)	0 (Valid Mode)
E1010	D Door HOP Stat.	0 (OFF)	
E1011	D Ven Val HOP St	0 (OFF)	
E1012	D FW Coil 1 Stat	0 (OFF)	

E1013	D FW Coil 2 Stat	0 (OFF)	
E1014	D Ann Heater St.	0 (OFF)	
E1015	D Shr Heater St.	0 (OFF)	
E1076	C EMAE -6 V Line	- 6.1 V ± 5 %	-6.3 – -5.7
E1077	C EMAE +6 V Line	6 V ± 5 %	5.7 – 6.3
E1078	C EMAE -13V Line	- 13.1 V ± 5 %	-13.7 – -12.3
E1079	C EMAE +13V Line	13.1 V ± 5 %	12.3 – 13.7
E1080	C EMAE +28V Line	27.7 V ± 5 %	25.6 – 29.4
E1081	C EMAE +18V Line	17.9 V ± 5 %	17.1 – 18.9
E1082	C Signal Ground	- 0.04 V ± 5 %	-0.1 – 0.1
E1083	C EMAE +32V Line	27 V ± 5 %	24.3 – 29.7
E1086	C EMCR +5 V Line	5.1 V ± 5 %	4.7 – 5.3
E1088	C EMCR -13V Line	- 13.1 V ± 5 %	-13.7 – -12.3
E1089	C EMCR +13V Line	13.1 V ± 5 %	12.3 – 13.7

- Send the TC Enter IDLE Mode.
- Send the TC Sensors On/Off (E102), with the following parameter setting:

PREF	PARA_NAME	VALUE
E128	AnnHeaterRelaySt	0 (OFF)
E129	VacuumSensorStat	1 (ON)
E130	RedThermContrSt	0 (OFF)
E131	NomThermContrSt	0 (OFF)

- In the EMCS Periodic H/K TM packet (30001), check the following parameter status:

TM_PREF	TM_PARA_NAME	VALUE
E1255	HDoorBellowState	0 (Retracted)
E1256	H Door Open uSw	1 (closed)
E1261	H Vacuum Monitor	Note 1
E1265	HDoorBellowPress	> 3.5 Bar (Note 2)

Note 1: For MOS1 chain, the vacuum monitor E1261 must be lower than 7000 mV (corresponding to 10 mB); for MOS2 chain, due to the existing vacuum leakage, it is expected to have about 1 B, which cannot be measured by the vacuum monitor K1261.
Note 2: 3.5 Warning limit, 2 Alarm limit and no-go criterium.

- Switch-off the experiment.

10. EXPERIMENT FAILURES

The paragraph deals with the management of possible failures, or incorrect operations of the Epic Mos Chain System.
It is defined as "failure" any event, due to a natural event or by an incorrect operation, which is causing, partially or totally, an incorrect working of the EMCS.
It is defined as incorrect operation, an operation which, deviating from the standard procedures, are causing an incorrect working of the EMCS
The causes of non-correct operations, failures, or corruption of data are hereafter classified on the following list of possible events.

10.1 External Failures

During the operational phase, the EMCS is fully dependent from the service supplied by XMM.
All failures or incorrect operations on systems related to EMCS could affect or jeopardise the Experiment performances.
A part the major systems, like RF Link loss or similar, (which is supposed to be managed at higher level), it is given hereafter, the list of the XMM system and related effects on EMCS in case of failure.

XMM System	Effect on EMCS	Actions / Notes
LCL Nominal	Loss of Nominal Chain	Change to Redundant LCL
LCL Redundant	Loss of Redundant Chain	Change to Nominal LCL
EPIC Power Bus	Loss of the Experiment	
RTU	Loss of DC/DC Synch	EMCS remain in full operation
	Loss of Thermistor Channels	Loss of CCD and Radiator Monitoring when EMCS is turned off.
	Loss of High Power Switches for Substitution Heaters	Loss of Safety Temperature Control on CCDs when EMCS is off. (min.T. = -150°C) Loss of Safety Temperature Control on all EMCS Unit. (min. T.= - 25°C) Possible damage if the temperature is out of the specified range
Telemetry	Loss of the Experiment	
Telecommand	Loss of the Experiment Control	

10.2 Incorrect Engineering Operations

In principle the Experiment has been conceived to be safe with respect to possible incorrect operations except for the operations related to the optical_door_entrance which, if conducted improperly, could damage the filters, as for the annealing operation, which could have, improperly done, the same effect.

10.3 Incorrect Scientific Operation

The Experiment is intrinsically safe with respect to all operations for settling parameters, modes, CCDs sequences, thresholds etc.
It must be noted that, in case of incorrect scientific operations, the information acquired by the system could be wrong.
In case of doubt on the scientific validity of the data, the calibration source represent the better and faster method for debugging.

10.4 Warning and Alarm Management

It is given, hereafter, the list of the housekeeping to be conditioned for the activation of Alarm or Warning alert. The actions to be undertaken under Alarm or Warning conditions can be addressed by clicking the relevant parameter. Some more information or possible debugging action and analysis, can be found in the link for each parameter.

PREF	TM_PARA_NAME	UNIT	Low Alarm	Low Warning	High Warning	High Alarm
E/K1001	EMDH Prim PW Consumption	A	0,3			0,5
E/K1002	EMDH Power Supply Temp. #1	°C	-20	-10		+50
E/K1003	EMDH Power Supply Temp. #2	°C	-20	-10		+50
E/K1004	EMDH +5 V PW Supply	V	+4,5			+5,5
E/K1005	EMDH DBU Power +6V	V	+5,5			+6,5
E/K1006	EMDH +15V PW Supply	V	+14			+16
E/K1007	EMDH -15V PW Supply	V	-16			-14
E/K1076	EMCR-EMAE -6 V Line	V	-6,5			-5,5
E/K1077	EMCR-EMAE +6 V Line	V	+5,5			+6,5
E/K1078	EMCR-EMAE –13 V Line	V	-14			-12
E/K1079	EMCR-EMAE +13 V Line	V	+12			+14
E/K1080	EMCR-EMAE +28 V Line	V	+26,5			+29,5
E/K1081	EMCR-EMAE +18 V Line	V	+17			+19
E/K1082	EMCR-EMAE Signal Ground	V	-0,5			+0,5
E/K1083	EMCR-EMAE +32 V Line	V	+26			+34
E/K1084	V EMVC Temp. #1	°C	-20	-10		+50
E/K1085	C EMCR Temp. #1	°C	-20	-10		+50
E/K1086	C EMCR +5 V Line	V	+4,5			+5,5
E/K1087	V EMVC Temp. #2	°C	-20	-10		+50
E/K1088	C EMCR -13V Line	V	- 14			-12
E/K1089	C EMCR +13V Line	V	+12			+14
E/K1090	C EMCR Temp. #2	°C	-20	-10		+50
E/K1253	EMCH FocalPlaneNormalRangeTemperature	°C	- 150	-135	N/A	N/A
E/K1260 PL, PDO, Decont.	EMAEFocalPlaneRedundantThermalControlTemperatureMonitor	°C	- 150	-70	+40	N/A
E/K1260 ADO	EMAEFocalPlaneRedundantThermalControlTemperatureMonitor	°C	- 150	-135	-70	N/A
E1261 PL, PDO	EMCH MOS1 Vacuum Monitor	mV	2000	4000	7000	7500
K1261 PL	EMCH MOS2 Vacuum monitor	mV	2000	7500	N/A	N/A
E/K1261 ADO	EMCH Vacuum Monitor	mV	N/A	N/A	N/A	N/A
E/K1262	EMCH Secondary Radiator Temperature	°C	N/A	-100	N/A	+100
E/K1265 PL	EMCH Door Bellow Pressure	Bar	2.5	3.5	N/A	N/A
E/K1265 PDO	EMCH Door Bellow Pressure	Bar	0.5	2	N/A	N/A
E/K1265 ADO	EMCH Door Bellow Pressure	Bar	N/A	N/A	N/A	N/A
E/K1308 PL, PDO, Decont.	EMCH FocalPlaneExtendedRangeTemperature	°C	-150	-70	+40	+135
E/K1308 ADO	EMCH FocalPlaneExtendedRangeTemperature	°C	-150	-135	-70	+135
E/K1310	EMCH FW Motor Temp	°C	-20	-10	N/A	+50
E/K1311	EMAE Electronics Temperature	°C	-20	-10	N/A	+65
E/K1312 PL, PDO, Decont.	EMAEFocalPlaneNominalThermalControlTemperatureMonitor	°C	- 150	-70	+40	N/A
E/K1312 ADO	EMAEFocalPlaneNominalThermalControlTemperatureMonitor	°C	- 150	-135	-70	N/A
E/K1315	EMCH Electr. Temperature	°C	-20	-10	N/A	+50

E/K1001	EMDH Prim PW Consumption	A	0,3			0,5

LOW ALARM ACTION:

- Go to the Safe Stand-by mode
- If the door is still closed, go to Idle mode and turn the FW to Open position
- Switch-off the EMCS chain

LOW WARNING ACTION

N/A

HIGH WARNING ACTION

N/A

HIGH ALARM ACTION

- Go to the Safe Stand-by mode
- If the door is still closed, go to Idle mode and turn the FW to Open position
- Switch-off the EMCS chain

E/K1002	EMDH Power Supply Temp. #1	degC	-20	-10		+50

LOW ALARM ACTION:

- Do not send any Telecommand to the EMCS
- Switch-on S/C EMDH Substitution Heater and leave it on until the temperature is higher than warning low limit (-10 °C).
- When the temperature is higher than warning low limit (-10 °C), switch-off the S/C EMDH Substitution Heater and enable EMCS commanding

LOW WARNING ACTION

- Do not send any Telecommand to the EMCS until the temperature is higher than warning low limit (-10 °C)

HIGH WARNING ACTION

N/A

HIGH ALARM ACTION

- Go to the Safe Stand-by mode
- If the door is still closed, go to Idle mode and turn the FW to Open position
- Switch-off the EMCS chain

E/K1003	EMDH Power Supply Temp. #2	degC	-20	-10		+50

LOW ALARM ACTION:

- Do not send any Telecommand to the EMCS
- Switch-on S/C EMDH Substitution Heater and leave it on until the temperature is higher than warning low limit (-10 °C).
- When the temperature is higher than warning low limit (-10 °C), switch-off the S/C EMDH Substitution Heater and enable EMCS commanding

LOW WARNING ACTION

- Do not send any Telecommand to the EMCS until the temperature is higher than warning low limit (-10 °C)

HIGH WARNING ACTION

N/A

HIGH ALARM ACTION

- Go to the Safe Stand-by mode
- If the door is still closed, go to Idle mode and turn the FW to Open position
- Switch-off the EMCS chain

E/K1004	EMDH +5 V PW Supply	V	+4,5			+5,5

LOW ALARM ACTION:

- Go to the Safe Stand-by mode
- If the door is still closed, go to Idle mode and turn the FW to Open position
- Switch-off the EMCS chain

LOW WARNING ACTION

N/A

HIGH WARNING ACTION

N/A

HIGH ALARM ACTION

- Go to the Safe Stand-by mode
- If the door is still closed, go to Idle mode and turn the FW to Open position
- Switch-off the EMCS chain

E/K1005	EMDH DBU Power +6V	V	+5,5			+6,5

LOW ALARM ACTION:

- Go to the Safe Stand-by mode
- If the door is still closed, go to Idle mode and turn the FW to Open position
- Switch-off the EMCS chain

LOW WARNING ACTION

N/A

HIGH WARNING ACTION

N/A

HIGH ALARM ACTION

- Go to the Safe Stand-by mode
- If the door is still closed, go to Idle mode and turn the FW to Open position
- Switch-off the EMCS chain

E/K1006	EMDH +15V PW Supply	V	+14			+16

LOW ALARM ACTION:

- Go to the Safe Stand-by mode
- If the door is still closed, go to Idle mode and turn the FW to Open position
- Switch-off the EMCS chain

LOW WARNING ACTION

N/A

HIGH WARNING ACTION

N/A

HIGH ALARM ACTION

- Go to the Safe Stand-by mode
- If the door is still closed, go to Idle mode and turn the FW to Open position
- Switch-off the EMCS chain

E/K1007	EMDH -15V PW Supply	V	-16			-14

LOW ALARM ACTION:

- Go to the Safe Stand-by mode
- If the door is still closed, go to Idle mode and turn the FW to Open position
- Switch-off the EMCS chain

LOW WARNING ACTION

N/A

HIGH WARNING ACTION

N/A

HIGH ALARM ACTION

- Go to the Safe Stand-by mode
- If the door is still closed, go to Idle mode and turn the FW to Open position
- Switch-off the EMCS chain

E/K1076	EMCR-EMAE -6 V Line	V	-6,5			-5,5

LOW ALARM ACTION:

- Go to the Safe Stand-by mode
- If the door is still closed, go to Idle mode and turn the FW to Open position
- Switch-off the EMCS chain

LOW WARNING ACTION

N/A

HIGH WARNING ACTION
N/A

HIGH ALARM ACTION
- Go to the Safe Stand-by mode
- If the door is still closed, go to Idle mode and turn the FW to Open position
- Switch-off the EMCS chain

E/K1077	EMCR-EMAE +6 V Line	V	+5,5			+6,5

LOW ALARM ACTION:
- Go to the Safe Stand-by mode
- If the door is still closed, go to Idle mode and turn the FW to Open position
- Switch-off the EMCS chain

LOW WARNING ACTION
N/A

HIGH WARNING ACTION
N/A

HIGH ALARM ACTION
- Go to the Safe Stand-by mode
- If the door is still closed, go to Idle mode and turn the FW to Open position
- Switch-off the EMCS chain

E/K1078	EMCR-EMAE –13 V Line	V	-14			-12

LOW ALARM ACTION:
- Go to the Safe Stand-by mode
- If the door is still closed, go to Idle mode and turn the FW to Open position
- Switch-off the EMCS chain

LOW WARNING ACTION
N/A

HIGH WARNING ACTION
N/A

HIGH ALARM ACTION
- Go to the Safe Stand-by mode
- If the door is still closed, go to Idle mode and turn the FW to Open position
- Switch-off the EMCS chain

E/K1079	EMCR-EMAE +13 V Line	V	+12			+14

LOW ALARM ACTION:

- Go to the Safe Stand-by mode
- If the door is still closed, go to Idle mode and turn the FW to Open position
- Switch-off the EMCS chain

LOW WARNING ACTION

N/A

HIGH WARNING ACTION

N/A

HIGH ALARM ACTION

- Go to the Safe Stand-by mode
- If the door is still closed, go to Idle mode and turn the FW to Open position
- Switch-off the EMCS chain

E/K1080	EMCR-EMAE +28 V Line	V	+26,5			+29,5

LOW ALARM ACTION:

- Go to the Safe Stand-by mode
- If the door is still closed, go to Idle mode and turn the FW to Open position
- Switch-off the EMCS chain

LOW WARNING ACTION

N/A

HIGH WARNING ACTION

N/A

HIGH ALARM ACTION

- Go to the Safe Stand-by mode
- If the door is still closed, go to Idle mode and turn the FW to Open position
- Switch-off the EMCS chain

E/K1081	EMCR-EMAE +18 V Line	V	+17			+19

LOW ALARM ACTION:

- Go to the Safe Stand-by mode
- If the door is still closed, go to Idle mode and turn the FW to Open position
- Switch-off the EMCS chain

LOW WARNING ACTION

N/A

HIGH WARNING ACTION
N/A

HIGH ALARM ACTION
- Go to the Safe Stand-by mode
- If the door is still closed, go to Idle mode and turn the FW to Open position
- Switch-off the EMCS chain

E/K1082	EMCR-EMAE Signal Ground	V	-0,5			+0,5

LOW ALARM ACTION:
- Go to the Safe Stand-by mode
- If the door is still closed, go to Idle mode and turn the FW to Open position
- Switch-off the EMCS chain

LOW WARNING ACTION
N/A

HIGH WARNING ACTION
N/A

HIGH ALARM ACTION
- Go to the Safe Stand-by mode
- If the door is still closed, go to Idle mode and turn the FW to Open position
- Switch-off the EMCS chain

E/K1083	EMCR-EMAE +32 V Line	V	+26			+34

LOW ALARM ACTION:
- Go to the Safe Stand-by mode
- If the door is still closed, go to Idle mode and turn the FW to Open position
- Switch-off the EMCS chain

LOW WARNING ACTION
N/A

HIGH WARNING ACTION
N/A

HIGH ALARM ACTION
- Go to the Safe Stand-by mode
- If the door is still closed, go to Idle mode and turn the FW to Open position
- Switch-off the EMCS chain

E/K1084	V EMVC Temp. #1	degC	-20	-10		+50

LOW ALARM ACTION:

- Do not send any Telecommand to the EMCS
- Switch-on S/C EMVC Substitution Heater and leave it on until the temperature is higher than warning low limit (-10 °C).
- When the temperature is higher than warning low limit (-10 °C), switch-off the S/C EMVC Substitution Heater and enable EMCS commanding

LOW WARNING ACTION

- Do not send any Telecommand to the EMCS until the temperature is higher than warning low limit (-10 °C)

HIGH WARNING ACTION

N/A

HIGH ALARM ACTION

- Go to the Safe Stand-by mode
- If the door is still closed, go to Idle mode and turn the FW to Open position
- Switch-off the EMCS chain

E/K1085	C EMCR Temp. #1	degC	- 20	-10		+ 50

LOW ALARM ACTION:

- Do not send any Telecommand to the EMCS
- Switch-on S/C EMCR Substitution Heater and leave it on until the temperature is higher than warning low limit (-10 °C).
- When the temperature is higher than warning low limit (-10 °C), switch-off the S/C EMCR Substitution Heater and enable EMCS commanding

LOW WARNING ACTION

- Do not send any Telecommand to the EMCS until the temperature is higher than warning low limit (-10 °C)

HIGH WARNING ACTION

N/A

HIGH ALARM ACTION

- Go to the Safe Stand-by mode
- If the door is still closed, go to Idle mode and turn the FW to Open position
- Switch-off the EMCS chain

E/K1086	C EMCR +5 V Line	V	+4,5			+5,5

LOW ALARM ACTION:

- Go to the Safe Stand-by mode
- If the door is still closed, go to Idle mode and turn the FW to Open position
- Switch-off the EMCS chain

LOW WARNING ACTION
N/A

HIGH WARNING ACTION
N/A

HIGH ALARM ACTION
- Go to the Safe Stand-by mode
- If the door is still closed, go to Idle mode and turn the FW to Open position
- Switch-off the EMCS chain

E/K1087	V EMVC Temp. #2	degC	- 20	-10		+ 50

LOW ALARM ACTION:
- Do not send any Telecommand to the EMCS
- Switch-on S/C EMVC Substitution Heater and leave it on until the temperature is higher than warning low limit (-10 °C).
- When the temperature is higher than warning low limit (-10 °C), switch-off the S/C EMVC Substitution Heater and enable EMCS commanding

LOW WARNING ACTION
- Do not send any Telecommand to the EMCS until the temperature is higher than warning low limit (-10 °C)

HIGH WARNING ACTION
N/A

HIGH ALARM ACTION
- Go to the Safe Stand-by mode
- If the door is still closed, go to Idle mode and turn the FW to Open position
- Switch-off the EMCS chain

E/K1088	C EMCR -13V Line	V	- 14			-12

LOW ALARM ACTION:
- Go to the Safe Stand-by mode
- If the door is still closed, go to Idle mode and turn the FW to Open position
- Switch-off the EMCS chain

LOW WARNING ACTION
N/A

HIGH WARNING ACTION
N/A

HIGH ALARM ACTION
- Go to the Safe Stand-by mode
- If the door is still closed, go to Idle mode and turn the FW to Open position
- Switch-off the EMCS chain

E/K1089	C EMCR +13V Line	V	+12			+14

LOW ALARM ACTION:

- Go to the Safe Stand-by mode
- If the door is still closed, go to Idle mode and turn the FW to Open position
- Switch-off the EMCS chain

LOW WARNING ACTION

N/A

HIGH WARNING ACTION

N/A

HIGH ALARM ACTION

- Go to the Safe Stand-by mode
- If the door is still closed, go to Idle mode and turn the FW to Open position
- Switch-off the EMCS chain

E/K1090	C EMCR Temp. #2	degC	-20	-10		+ 50

LOW ALARM ACTION:

- Do not send any Telecommand to the EMCS
- Switch-on S/C EMCR Substitution Heater and leave it on until the temperature is higher than warning low limit (-10 °C).
- When the temperature is higher than warning low limit (-10 °C), switch-off the S/C EMCR Substitution Heater and enable EMCS commanding

LOW WARNING ACTION

- Do not send any Telecommand to the EMCS until the temperature is higher than warning low limit (-10 °C)

HIGH WARNING ACTION

N/A

HIGH ALARM ACTION

- Go to the Safe Stand-by mode
- If the door is still closed, go to Idle mode and turn the FW to Open position
- Switch-off the EMCS chain

E/K1253	EMCH FocalPlaneNormalRangeTemperature	degC	- 150	-135	N/A	N/A

LOW ALARM ACTION:

Check Thermal Telecommands and Parameters.

If all setpoints are OK, turn on the CCD Substitution Heater.

If not, send correct Telecommand and Parameters Sequence.

LOW WARNING ACTION

Check Thermal Telecommands and Parameters.

If all setpoints are OK, change to Redundant Control
If not, send correct Telecommand and Parameters Sequence.

HIGH WARNING ACTION
N/A

HIGH ALARM ACTION
N/A

E/K1260	EMAE Focal Plane Redundant Thermal Control Temperature Monitor	degC	- 150	-70	+30	N/A

Prior to Launch and Pre Door Opening:

LOW ALARM ACTION:
Check set point, telecommands and parameters.
If ok, turn on CCDs Substitution Heaters.
If not, send correct sequence.

LOW WARNING ACTION
Check set point, telecommands and parameters.
If not, send correct sequence.
If ok, switch on redundant Thermal Control System

HIGH WARNING ACTION
Check set point, telecommands and parameters.
If not, send correct sequence.
If ok, check if Venting was properly done - see if camera temperature E/K 1315 is lower than expected
If not OK, do Venting again
If OK, send Safe Stand By Command and switch of the EMCS

HIGH ALARM ACTION
N/A

During Operation

LOW ALARM ACTION:
Check set point, telecommands and parameters.
If ok, turn on CCDs Substitution Heaters.
If not, send correct sequence.

LOW WARNING ACTION
Check set point, telecommands and parameters.
If not, send correct sequence.
If ok, switch on redundant Thermal Control System

HIGH WARNING ACTION
Check set point, telecommands and parameters.
If not, send correct sequence.
If ok, check whether Decontamination necessary - see if camera temperature E/K 1315 is lower than expected
If yes, do Decontamination
If not, change to redundant Thermal Control System

HIGH ALARM ACTION
N/A

E/K1261	EMCH Vacuum Monitor	mV	2000	4000	7000	7500

LOW ALARM ACTION
Command vacuum sensors ON

LOW WARNING ACTION - MOS1
Vacuum probably OK, but camera is too warm for meaningful reading.
Confirm camera temperature E/K 1315 above +25C

HIGH WARNING ACTION - for MOS1

Prior to Launch:
Check camera temperature E1315
If E1315 > +15C evacuate camera if possible.

Pre Door Opening.
Check camera temperature E1315
If E1315 > +15C do camera Venting. Do not open the door!

During Operation
Possible failure in Vacuum H.K. Dont care.

HIGH ALARM ACTION - for MOS1

Prior to Launch:
Check camera temperature E1315
If E1315 > +15C Pump down Camera. Do not launch!

Pre Door Opening.
Check camera temperature E1315
If E1315 > +15C do camera Venting. Do not open the door!

During Operation
Possible failure in Vacuum H.K. Dont care.

LOW WARNING ACTION - MOS2 (7500)

Prior to Launch:
If K1315 < +25C top up Helium if possible

HIGH WARNING ACTION - MOS2

Prior to Launch: N/A

Other conditions as for MOS1

E/K1262	EMCH Secondary Radiator Temperature	degC	N/A	-100	N/A	+100

LOW ALARM ACTION
N/A

LOW WARNING ACTION
Decontamination necessary if E/K 1315 is lower than expected

HIGH WARNING ACTION
N/A

HIGH ALARM ACTION
Switch off Secondary Shroud Heater

E/K1265	EMCH Door Bellow Pressure (PL)	Bar	2.5	3.5	N/A	N/A
	PDO	Bar	0.5	2.0	N/A	N/A

LOW ALARM ACTION

Prior to Launch:
Check whether bellows and vac sensors are switched ON.
If Yes, Pump Up Pressure in the Bellows. Do not launch! Door could open

Pre Door Opening (0.5 Bar)
Check whether bellows and vac sensors are switched ON.
    If Yes
        If Open Door Operation is in process: discard the Alarm.
        Else prepare for immediate door opening

During Operation
Don't care.

LOW WARNING ACTION

Prior to Launch:
Pump Up Pressure in the Bellows. Do not launch! Door could open

Pre Door Opening (2.0 Bar)
If Open Door Operation is in process: discard the Alarm.
Else alert camera representative

During Operation
Don't care.

HIGH WARNING ACTION
N/A

HIGH ALARM ACTION
N/A

E/K1308	EMCH Focal Plane Extended Range Temperature (PL and PDO)	degC	-150	-70	+30	+135
	Normal Operation	degC	-150	-135	-70	+135

Prior to Launch and Pre Door Opening:

LOW ALARM ACTION
Check set point.
If ok, switch on the FPA Substitution Heaters.
If not, send the correct TLC Sequence

LOW WARNING ACTION
Check set point.
If ok, change to Redundant Control.
If still on Warning Condition, switch on the FPA Substitution Heater
If not, send the correct TLC Sequence

HIGH WARNING ACTION (Prior to Launch)
Check set point.
If not OK send the correct TLC Sequence

HIGH WARNING ACTION (Pre Door Opening)
Check set point.
If OK, check whether Venting necessary - is E/K 1315 lower than expected?
If not, send the correct TLC Sequence

HIGH ALARM ACTION
Switch off Annealing Heater

During Operation

LOW ALARM ACTION
Check set point.
If ok, switch on the FPA Substitution Heaters.
If not, send the correct TLC Sequence

LOW WARNING ACTION
Check set point.
If ok, change to Redundant Control.
If still on Warning Condition, turn on the FPA Substitution Heater
If not, send the correct TLC Sequence

HIGH WARNING ACTION
Check set point.
If OK, check whether Decontamination necessary
If not, send the correct TLC Sequence

HIGH ALARM ACTION
Turn off Annealing Heater

E/K1310	EMCH FW Motor Temp	degC	-10		+45	+50

LOW ALARM ACTION
Check ambient temperature. Possible problem in FPA Thermal Control

LOW WARNING ACTION
N/A

HIGH WARNING ACTION
Check if the Filter Wheel is moving.
If yes, check the difference between E/K 1310 and E/K 1315.
If the difference is higher than 10°C, switch off the Filter Wheel.
If not, discard the TC. Possible problem in FPA Thermal Control
If not, check for possible problem in FPA Thermal Control

HIGH ALARM ACTION
Check if the Filter Wheel is moving.
If yes, check the difference between E/K 1310 and E/K 1315.
If the difference is higher than 10°C, switch off the Filter Wheel.
If not, discard the TC. Possible problem in FPA Thermal Control
If not, check for possible problem in FPA Thermal Control

E/K1311	EMAE Electronics Temperature	degC	-10		+55	+65

LOW ALARM ACTION:
If the alarm is generated immediately after EMCS switch on, check the ambient temperature.
If the ambient temperature (read via RTU) is equal to the EMAE temperature, +10/- 5°C, monitor the change rate of the EMAE temperature, which must increase.
If the temperature reach the limit, proceed with the operations
If not, switch off the EMCS, activate the Unit Substitution Heaters and check for a possible failure in thermal control of FPA
If not, switch off the EMCS and check for possible problem in EMAE temperature HK.
If the alarm is generated during EMCS nominal operation, switch off the EMCS, activate the Units Substitution Heaters and check for possible problem in the thermal control of the FPA

LOW WARNING ACTION
N/A

HIGH WARNING ACTION
Check the ambient temperature.
If the ambient temperature is equal to the EMAE temperature, +10°/-5°C, monitor the change rate of the EMAE and switch off if the HIGH ALARM is activated.
If not, switch off the EMCS and check for possible problem in EMAE temperature HK.

HIGH ALARM ACTION
Check the ambient temperature.
If the temperature is equal to the EMAE temperature, +/- 5%C, switch off the EMCS and check for possible problem on FPA thermal control.
If not, switch off the EMCS and check for possible problem in EMAE temperature HK.

E/K1312	EMAE Focal Plane Nominal Thermal Control Temperature Monitor	degC	-135	-120	-75	+130

Prior to Launch and Pre Door Opening:

LOW ALARM ACTION:
Check set point, telecommands and parameters.
If ok, turn on CCDs Substitution Heaters.
If not, send correct sequence.

LOW WARNING ACTION
Check set point, telecommands and parameters.
If not, send correct sequence.
If ok, switch on redundant Thermal Control System

HIGH WARNING ACTION
Check set point, telecommands and parameters.
If not, send correct sequence.

If ok, check if Venting was properly done - see if camera temperature E/K 1315 is lower than expected

If not OK, do Venting again

If OK, send Safe Stand By Command and switch of the EMCS

HIGH ALARM ACTION
N/A

During Operation

LOW ALARM ACTION:
Check set point, telecommands and parameters.

If ok, turn on CCDs Substitution Heaters.

If not, send correct sequence.

LOW WARNING ACTION
Check set point, telecommands and parameters.

If not, send correct sequence.

If ok, switch on redundant Thermal Control System

HIGH WARNING ACTION
Check set point, telecommands and parameters.

If not, send correct sequence.

If ok, check whether Decontamination necessary - see if camera temperature E/K 1315 is lower than expected

If yes, do Decontamination

If not, change to redundant Thermal Control System

HIGH ALARM ACTION
N/A

E/K1315	EMCH Electr. Temperature	degC	-10	-5	+45	+50

LOW ALARM ACTION:
If the alarm is generated immediately after EMCS switch on, check the ambient temperature.

If the ambient temperature (read via RTU) is equal to the EMCH temperature, +/- 5°C, monitor the change rate of the EMCH temperature, which must increase.

If the temperature reach the limit, proceed with the operations

If not, switch off the EMCS, activate the Unit Substitution Heaters and check for a possible failure in thermal control of FPA

If not, switch off the EMCS and check for possible problem in EMCH temperature HK.

If the alarm is generated during EMCS nominal operation, switch off the EMCS, activate the Units Substitution Heaters and check for possible problem in the thermal control of the FPA

LOW WARNING ACTION
N/A

HIGH WARNING ACTION

If the warning is generated immediately after switch on, check the ambient temperature.

If the ambient temperature is equal to the EMCH temperature, +/- 5°C, monitor the change rate of the EMCH temperature, and switch OFF if the temperature reaches the High Alarm setting.

If not, switch off the EMCS and check for possible problem in EMCH temperature HK.

If the warning is generated during EMCS nominal operation, check the ambient temperature.

If the temperature is equal to the EMCH temperature, -5°/ +10°C, monitor the change rate of the EMCH and switch off if the HIGH ALARM is activated.

If not, switch off the EMCS and check for possible problem in EMCH temperature HK.

HIGH ALARM ACTION

Check the ambient temperature.

If the temperature is equal to the EMCH temperature, +/- 5°C, switch off the EMCS and check for possible problem on FPA thermal control.

If not, switch off the EMCS and check for possible problem in EMCH temperature HK.

11. EXPERIMENT BUDGETS

11.1 POWER BUDGET

The single unit power, including specific experiment items, and the whole experiment power consumption is shown in the following table:

Notes

- The Operating Heater current contribution is always considered at the maximum value. When the temperature is stable it should be significantly lower.
- The Decontamination Heater current consumption is not continuous but pulsed, therefore the average current is significantly lower.
- It is considered that the Filter Wheel is operated in Normal mode.

11.2 MASS BUDGET

The following table contains the mass of each units and the total mass of the Epic MosCamera System:

UNIT	EMCH	EMAE	EMCR	EMVC	EMDH	EMHN	EMPS	*EMCS*
MASS	32650	6700	6200	3800	14950	6700	3950	74950

Where:

EMCH: Camera Head
EMAE: Analog Electronics
EMCR: Control & Recognition
EMVC: Voltage Converter
EMDH: Data Handling
EMHN: Harness
EMPS: Proton Shield

11.3 TELECOMMAND BUDGET

The number of telecommands for each category is shown in the following table.
The total telecommands number is 113.

Type	5					6			9					10			13
Subtype	1	2	3	4	5	1	2	3	1	2	3	4	5	2	3	5	1
TCs Number	**1**	**1**	**71**	**13**	**10**	**3**	**3**	**2**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

11.4 TELEMETRY BUDGET

The number of telemetry packets for each category is shown in the following table.
The total telemetry number is 77.

Type	1	3			4			5	6		9	10	15			
Subtype	1	1	2	4	1	2	3	4	2	3	1	5	1	2	3	4
TMs Number	**1**	**1**	**10**	**25**	**5**	**2**	**5**	**13**	**3**	**2**	**1**	**1**	**2**	**2**	**1**	**3**

12. INTERFACE CONTROL DRAWING

The following part contains all the Interface Control Drawings of the Units composing the Epic Mos Camear System.

12.1 **Epic Mos Analog Electronis** **EMAE Interface Configuration Drawing**

12.2 **Epic Mos Control and Recognition** **EMCR Interface Configuration Drawing**

12.3 **Epic Mos Voltage Converter** **EMVC Interface Configuration Drawing**

12.4 **Epic Mos Data Handling** **EMDH Interface Configuration Drawing**

12.5 **Epic Mos Camera Head 1** **EMCH 1 Interface Configuration Drawing**

12.6 **Epic Mos Camera Head 2** **EMCH 2 Interface Configuration Drawing**

12.7 **Epic Mos Proton Shield** **EMPS Interface Configuration Drawing**

12.8 **Epic Mos Camera 1 Harness** **EMHA 1 Interface Configuration Drawing**

12.9 **Epic Mos Camera 2 Harness** **EMHA_2 Interface Configuration Drawing**

13. APPENDIX A

OFFEST AND VARIANCE ALGORITHM

14. APPENDIX B

EVENT RECOGNITION METHOD