AGILE	DWG

DOCUMENT TYPE: **SUBSYSTEM SPECIFICATION**

TITLE: **GRID LEVEL-1.5 TRIGGER SPECIFICATIONS**

DOCUMENT Ref. No.: AGILE-DWG-SP-002 **N° OF PAGES:** i-iii, 14

ISSUE No.: 2 **DATE:** 19/02/2003

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CHANGE RECORD

ISSUE	DATE	PAGE	DESCRIPTION OF CHANGES	RELEASE
1	06/03/2002		First Issue	
2	18/11/2002	All 3 10	Revised according to the Reference System defined by AGILE-AST-TN-009 issue-1. Inclusion of the AGILE-AST-TN-009 issue-1 in the Applicable Document List. URS-3.3.3.6, URS-3.3.4.6: TBC cancelled	

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1. INTRODUCTION

1.1 SCOPE OF THE DOCUMENT

The aim of this document is to provide the specifications of the Level-1.5 Trigger algorithm for the Gamma-Ray Imaging Detector (GRID) of the AGILE Instrument.

1.2 ACRONYMS

AC	Anti-Coincidence system
FTB	Front-End and Trigger Board
FEF	Front-End Freeing
GRID	Gamma-Ray Imaging Detector
LUT	Look-Up Table
ST	Silicon Tracker
TC	TeleCommand
1M	1-Matrix logic
2M	2-Matrix logic

2. APPLICABLE AND REFERENCE DOCUMENTS

2.1 APPLICABLE DOCUMENTS

AD [1] *AGILE-DWG-SS-002 Issue 7*
AD [2] *AGILE-AST-TN-009 Issue 2*

2.2 REFERENCE DOCUMENTS

RD [1] *AGILE Phase A Report*
RD [2] *AGILE Phase C/D Technical Proposal – Executive Summary TL16397 – Issue 2 (LABEN)*

2.3 DOCUMENT PRIORITY

A priority in the applicability of documents is established as follows:

1. P/L System Requirements
2. Current Document
3. Applicable Documents
4. Minutes of Meeting

In case of conflict among technical material contained in these documents, the highest rank document shall have the precedence.

3. GRID LEVEL-1.5 TRIGGER

3.1 GENERAL

URS-3.1.1 The Level-1.5 trigger shall be implemented in order to reject the charged particles (mostly protons, electrons and positrons) penetrating from AC lateral panels. The algorithm shall use the information of all the triggered TAA1s and the AC lateral side signals (the ORs of the three trigger signals related to the same AC lateral side).

URS-3.1.2 The trigger bits of the TAA1s belong to the X and Z projections shall be arranged in two matrices **X** and **Z** as shown in Figure 1. The trigger bits shall be disposed in the matrix in the same order of the chips in the ST detector. Furthermore, the information of each matrix shall be completed with the trigger bits of the two AC lateral sides having the plastic panels parallel to the strips direction (see Figure 2).

URS-3.1.3 The Level-1.5 trigger is composed by the following processing steps:

I) A Level-1.5 Access Procedure checking the AC and FTB trigger bits.

II) Three different trigger algorithms carried out in parallel and processing the triggered TAA1 maps and the AC trigger bits:

II.1) a NEAR algorithm verifying the presence of fired TAA1 close to the fired AC lateral side;

II.2) a COEF algorithm evaluating the size of the ST area covered by the detected track;

II.3) a DIS algorithm evaluating the slope of the track respect to the fired AC lateral sides.

III) An output trigger logic which combines in a suitable way the partial triggers in order to carry out the Level-1.5 Trigger.

$$X = \begin{bmatrix} x_{1,1} & \cdots & x_{1,12} \\ \vdots & & \vdots \\ x_{i,j} & & \\ \vdots & & \vdots \\ x_{12,1} & \cdots & x_{12,12} \end{bmatrix} \qquad Z = \begin{bmatrix} z_{1,1} & \cdots & z_{1,12} \\ \vdots & & \vdots \\ z_{i,j} & & \\ \vdots & & \vdots \\ z_{12,1} & \cdots & z_{12,12} \end{bmatrix}$$

Figure 1 – The X and Z matrices.

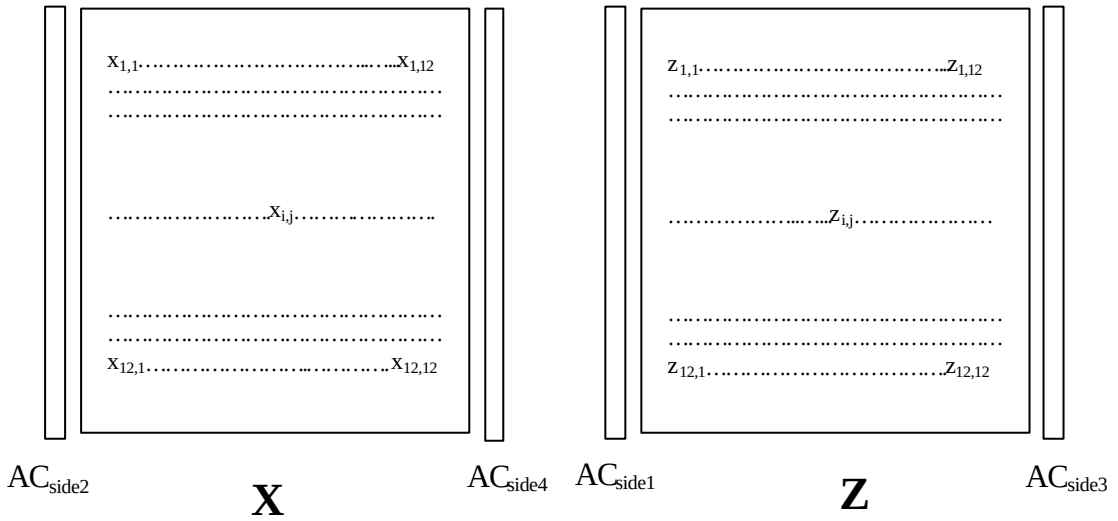

Figure 2 – The X and Z trigger bits and the relevant AC lateral sides (see AD[2]).

3.2 LEVEL-1.5 ACCESS PROCEDURE

URS-3.2.1 At the beginning of the Level-1.5 trigger stage, the configuration of the fired AC lateral sides and the configuration of the active View Trigger Strobes (the strobes generated, for each projection, by the "majority trigger logic"; see AD[1]) shall be checked in order to carry out the proper trigger processing.

URS-3.2.2 Two kinds of Level-1.5 trigger logic, distinguished by different input data, are foreseen:

1-MATRIX (1M) Logic – the processing involves either the **X** matrix or the **Z** matrix separately with the relevant AC lateral trigger bits.

2-MATRIX (2M) Logic – the processing involves both the **X** and **Z** matrices and all the four AC lateral trigger bits.

URS-3.2.3 The Level-1.5 Access Procedure, aimed to assign to each event the proper trigger logic, shall be performed according to the following rules (see Figure 3):

1) If **only one** AC lateral side is fired and the relevant View Trigger Strobe is **active**, a 1M Logic shall be applied considering the matrix in correspondence with the fired AC lateral side.

2) If **two** adjacent AC lateral sides are fired and **both** the View Trigger Strobes are **active**, a 2M Logic shall be applied considering both the **X** and **Z** matrix.

3) If **two** adjacent AC lateral sides are fired and **only one** View Trigger Strobe is **active**, a 1M Logic is applied considering the active strobe corresponding matrix.

4) If **only one** AC lateral side is fired and the relevant View Trigger Strobe is **inactive**, the trigger processing shall be interrupted and the FEF shall be activated.

5) In **all other cases**, as determined by TC, the event rejection or the FEF procedure shall be started.

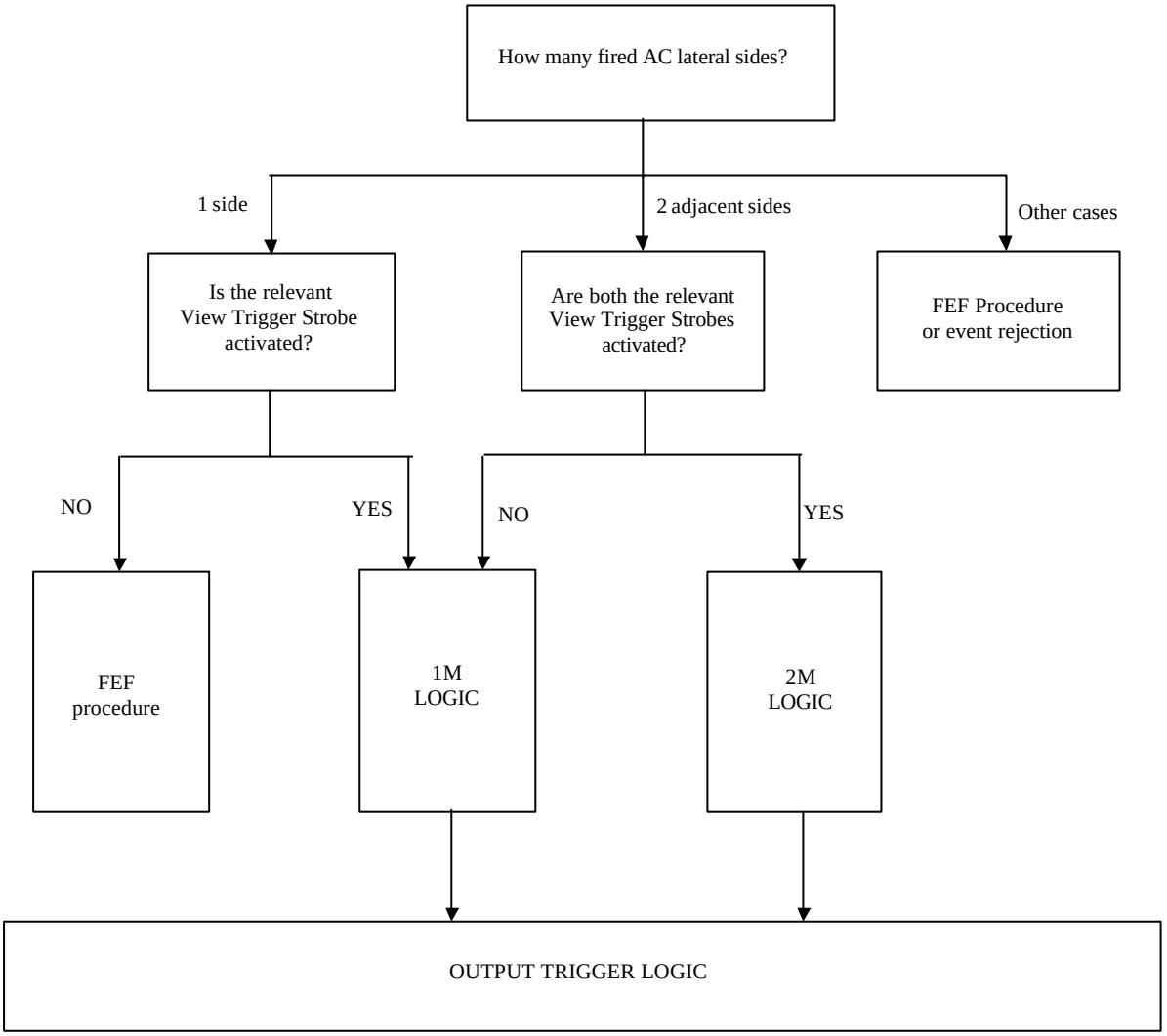

Figure 3 – The Level-1.5 Access Procedure Logic.

3.3 2-MATRICES TRIGGER LOGIC

3.3.1 GENERAL

URS-3.3.1.1 The trigger logic shall be able to extract, from the **X** and **Z** matrices, the sub-matrices **X** and **Z** determined, as shown in Figure 4, by the first and the last rows with elements different to zero. Such rows, labelled by i_{frx}/i_{frz} and i_{lrx}/i_{lrz} respectively, are related to the first and the last fired ST views.

URS-3.3.1.2 The trigger logic shall be able to process the sub-matrix data in order to carry out in parallel the NEAR, the COEF and the DIS algorithms as shown in Figure 5.

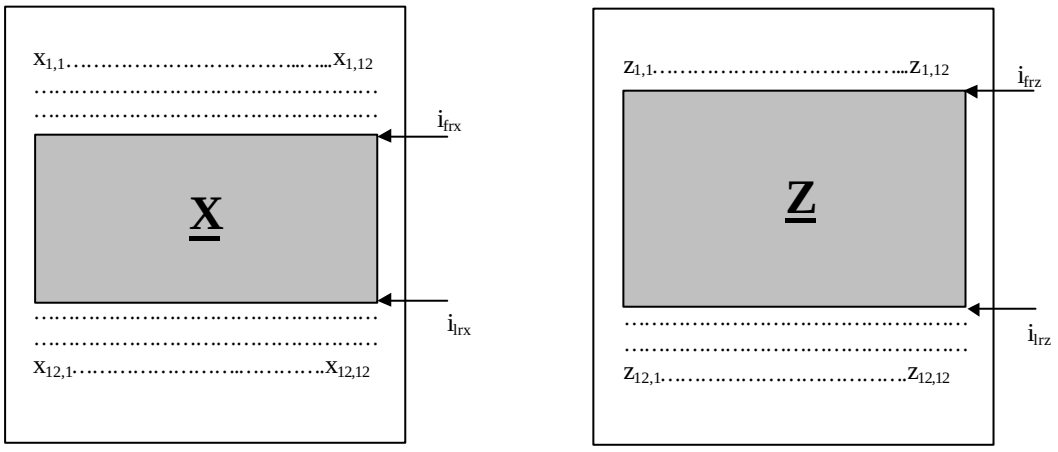

Figure 4 – The X and Z sub-matrices.

3.3.2 NEAR TRIGGER ALGORITHM

URS-3.3.2.1 **X-NEAR Trigger**. The NEAR trigger logic shall be able to check (processing the trigger bits of the sub-matrix **X**) the presence of triggered TAA1 in the first n_X ST columns closest to the fired AC lateral side.

URS-3.3.2.2 **Z-NEAR Trigger.** The NEAR trigger logic shall be able to check (processing the trigger bits of the sub-matrix **Z**) the presence of triggered TAA1 in the first n_Z ST columns closest to the fired AC lateral side.

URS-3.3.2.3 The n_X parameter shall be programmable by TC.

URS-3.3.2.4 The n_Z parameter shall be programmable by TC.

URS-3.3.2.5 The X-NEAR and Z-NEAR Trigger stages can be disabled separately by TC.

3.3.3 COEF TRIGGER ALGORITHM

URS-3.3.3.1 The COEF trigger logic shall be able to identify (processing the trigger bits of the sub-matrix **X**) the ST columns containing the closest and the farthest triggered TAA1 from the fired AC lateral side. The relevant columns in the matrix **X** shall be labelled by the index j_{fcx} and j_{lcx} respectively.

URS-3.3.3.2 The COEF trigger logic shall be able to identify (processing the trigger bits of the sub-matrix **Z**) the ST columns containing the closest and the farthest triggered TAA1 from the fired AC lateral side. The relevant columns in the matrix **Z** shall be labelled by the index j_{fcz} and j_{lcz} respectively.

URS-3.3.3.3 The COEF trigger logic shall be able to calculate the following quantities:

$$\Delta W_x = |i_{frx} - i_{lrx}|$$

$$\Delta Z_x = |j_{fcx} - j_{lcx}|$$

$$\Delta W_z = |i_{frz} - i_{lrz}|$$

$$\Delta Z_z = |j_{fcz} - j_{lcz}|$$

The resulting ΔW_x, ΔZ_x, ΔW_z and ΔZ_z shall be coded by 4-bit words.

URS-3.3.3.4 The COEF trigger shall be carried out reading a dedicated Look-Up Table (LUT) with a 16-bit address composed by the 4-bit words ΔW_x, ΔZ_x, ΔW_z and ΔZ_z disposed in a fixed order.

URS-3.3.3.5 The COEF LUT shall be programmable by TC.

URS-3.3.3.6 The COEF Trigger stage can be disabled by TC, i.e., the reading of the COEF LUT by-passed and the COEF Trigger forced to the inactive state.

3.3.4 DIS TRIGGER ALGORITHM

URS-3.3.4.1 The DIS trigger logic shall be able to calculate (processing the trigger bits belong to the sub-matrix **X**) the distance DIS_{fvx} on the first fired view and the distance DIS_{lvx}.on the last fired view between the closest triggered TAA1 and the fired AC lateral side. Such distances shall be evaluated considering the number of TAA1.

URS-3.3.4.2 The DIS trigger logic shall be able to calculate (processing the trigger bits belong to the sub-matrix **Z**) the distance DIS_{fvy} on the first fired view and the distance DIS_{lvz}.on the last fired view between the closest triggered TAA1 and the fired AC lateral side. Such distances shall be evaluated considering the number of TAA1.

URS-3.3.4.3 The evaluated DIS_{fvx}, DIS_{lvx} , DIS_{fvz} and DIS_{lvz} shall be coded with 4-bit words.

URS-3.3.4.4 The DIS trigger shall be carried out reading a dedicated LUT with a 16-bit address composed by the 4-bit words DIS_{fvx}, DIS_{lvx} , DIS_{fvz} and DIS_{lvz} disposed in a fixed order.

URS-3.3.4.5 The DIS LUT shall be programmable by TC.

URS-3.3.4.6 The DIS Trigger stage can be disabled by TC, i.e., the reading of the DIS LUT by-passed and the DIS Trigger forced to the inactive state.

3.4 1-MATRIX TRIGGER LOGIC

In the following, we call "processed ST projection" the X- or the Z-projection identified by the Access Procedure defined in section 3.2.

3.4.1 GENERAL

URS-3.4.1.1 In case that the Level-1.5 Access Procedure selects a 1M Logic, the processing foreseen for the 2M Logic shall be applied with the differences described here below and shown in Figure 6.

3.4.2 NEAR TRIGGER ALGORITHM

URS-3.4.2.1 The NEAR trigger logic shall be able to carry out the NEAR Trigger, related to the processed ST projection, with the same algorithm described in section 3.3.2.
The NEAR Trigger, related to the orthogonal projection, shall be left in the inactive state.

3.4.3 COEF TRIGGER ALGORITHM

URS-3.4.3.1 The COEF trigger logic shall be able to calculate the quantities ΔW and ΔZ, referred to the processed ST projection, with the same algorithm described in section 3.3.3.
The couple of parameters ΔW and ΔZ, related to the orthogonal ST projection, shall be set to zero.

URS-3.4.3.2 The COEF trigger shall be carried out, as for the 2M Logic, reading the COEF LUT with an address composed as required by the URS-3.3.3.4.

3.4.4 DIS TRIGGER ALGORITHM

URS-3.4.4.1 The DIS trigger logic shall be able to calculate the distances DIS_{fv} and DIS_{lv}, referred to the processed ST projection, with the same algorithm described in section 3.3.4.

The couple of parameters related to the unprocessed ST projection shall be set to zero.

URS-3.4.4.2 The DIS trigger shall be carried out, as for the 2M Logic, reading the DIS LUT with an address composed as required by the URS-3.3.4.4.

3.5 OUTPUT TRIGGER LOGIC

URS-3.5.1 The Level-1.5 Trigger shall be carried out reading a dedicated LUT with a 5-bit address composed, in a fixed order, by the X-NEAR trigger bit, the Z-NEAR trigger bit, the COEF trigger bit, the DIS trigger bit and one bit which shall signal the application of a 1M Logic.

URS-3.5.2 The Level-1.5 Trigger LUT shall be programmable by TC.

2-MATRIX LOGIC

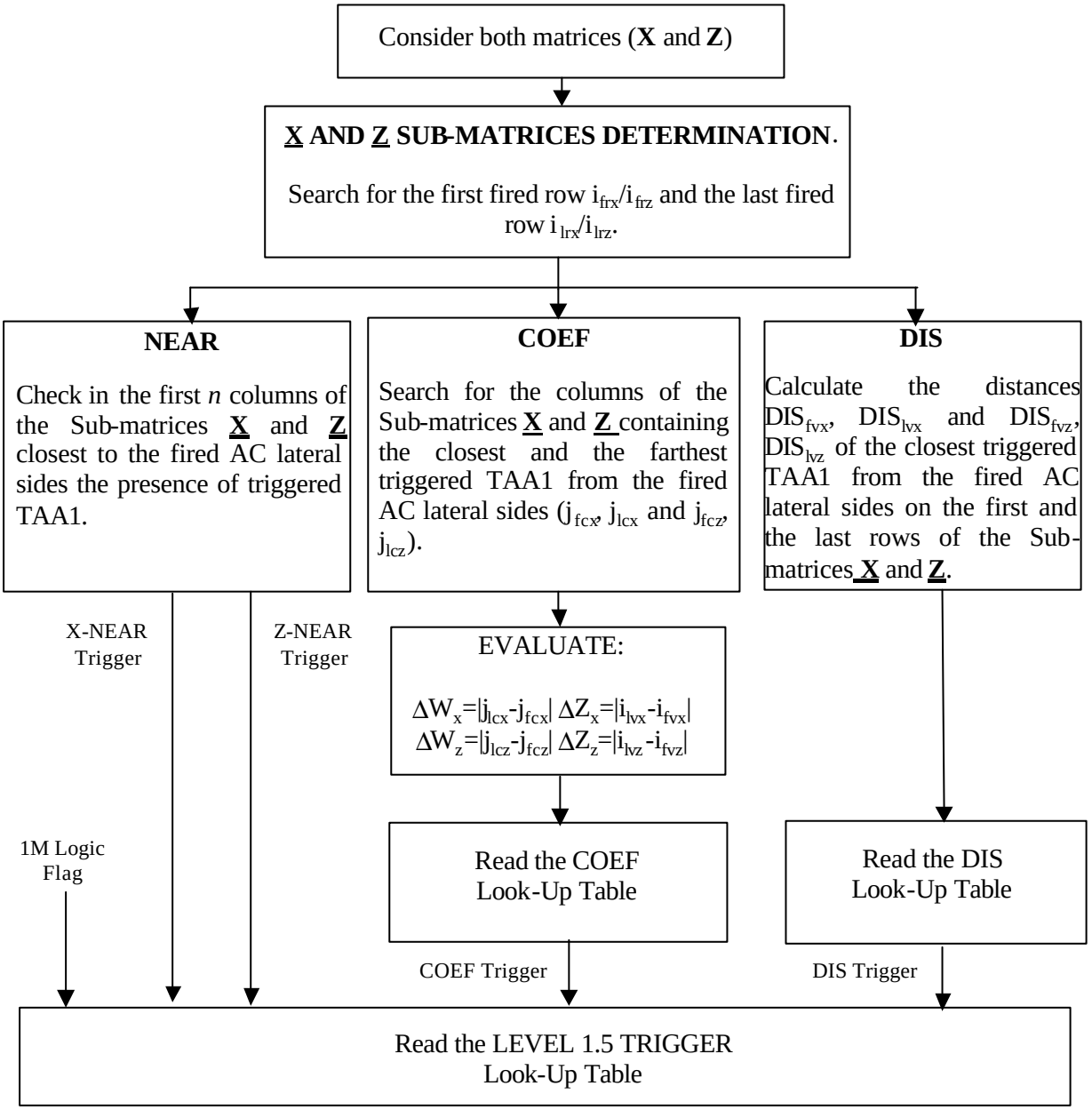

Figure 5 – The 2-MATRIX Logic.

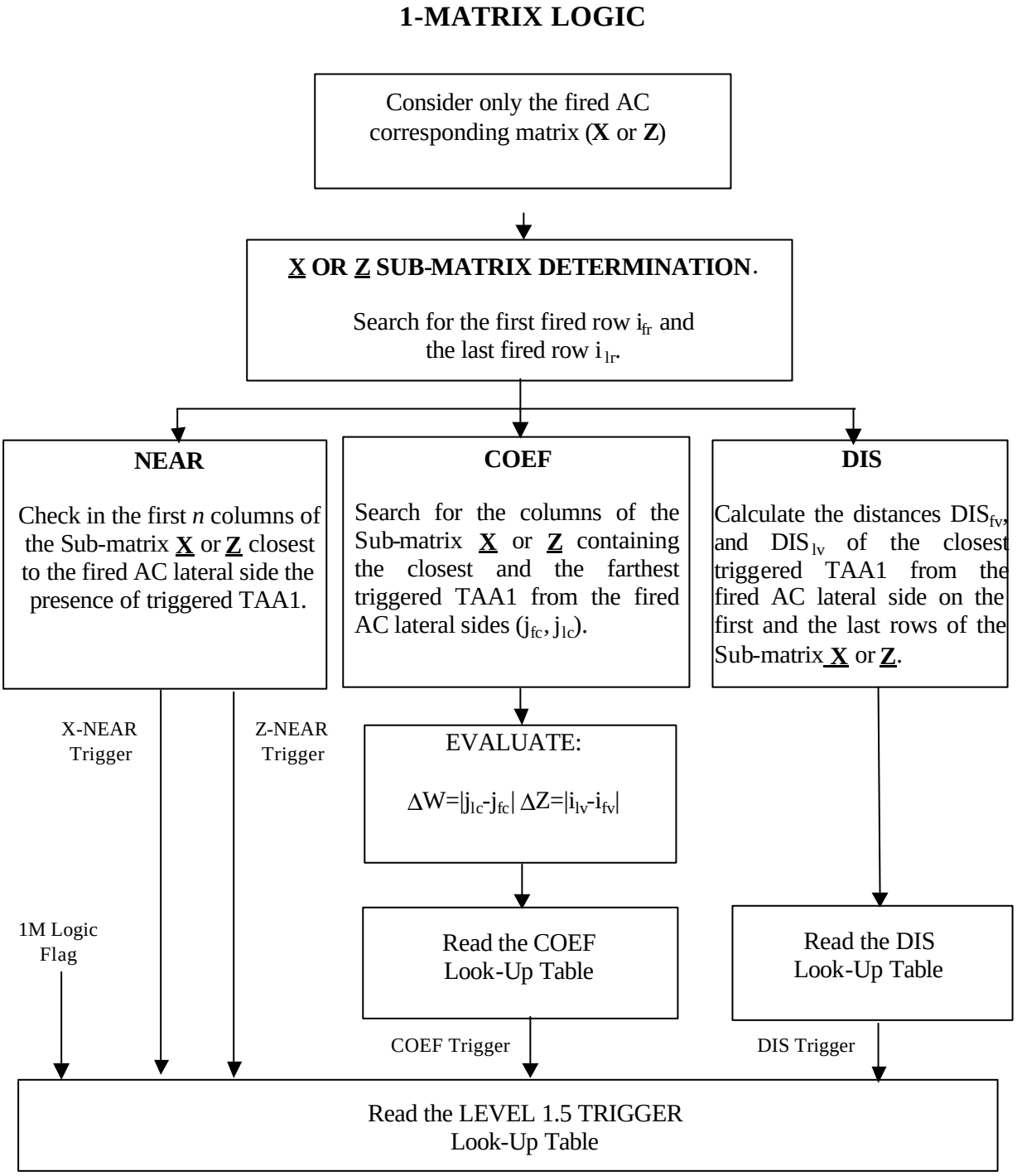

Figure 6 – The 1-MATRIX Logic.