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TABLE OF CONTENTS

1 INTRODUCTION..... IV
1.1 Scope and Purpose of the Document..... iv
Definitions, Acronyms, Abbreviations..... iv
1.1.1 Acronyms..... iv
2 REFERENCE DOCUMENTS..... V
3 SA CONFIGURATION..... VI
3.1 DESCRIPTION OF SA CONFIGURATION..... vii
3.1.1 REGIN config (DC REGISTER _IN FOR “SCIE MODE”)..... vii
3.1.2 SAIE DAC..... viii
3.1.3 SAFEE DAC..... viii
3.1.4 number of calpulses..... ix
3.1.5 DC master reset..... ix
3.1.6 DC SUPPLY (DC supply switch)..... ix
3.1.7 LatchUP Monitor enable..... ix
3.1.8 MGO sampling delay..... x
3.1.9 veto enable..... x
3.1.10 ST VETO CONFIG (ST_VETO_CONF)..... x
3.1.11 MCAL VETO CONFIG (MCAL_VETO_CONF)..... x
3.1.12 DC ENABLE..... xi
3.2 FORMAT OF FITS FILE FIELDS for SA CONFIGURATION..... xii
3.2.1 CONFIGURATION SEQUENCE..... xiii
4 SA COMMUNICATION WITH ST, MCAL AND AC..... XIV
5 CONFIGURATION REGIN FOR XAA1.2 DAISY CHAINS WITHIN SAGILE SAFEES..... XV

List OF Figures

1 INTRODUCTION

1.1 Scope and Purpose of the Document

Definitions, Acronyms, Abbreviations

The following is a list of definitions used throughout this document.

1.1.1 ACRONYMS

EGSE	Electrical Ground Support Equipment
GSE	Ground Support Equipment
Instrument SC	Instrument Science Console
IP	Integrated Payload
P/L	Payload
PDHU	Payload Data handling Unit
TBC	To Be Confirmed
TBD	To Be Defined
TC	Telecommand
TE	Test Equipment
TM	Telemetry

2 REFERENCE DOCUMENTS

[1] SAIE 2 PFM TEST REPORT
[2] SAIE specification and requirement document
[3] AGILE IPL reference system

3 SA CONFIGURATION

The SAFEEs configuration is performed by the SAIEs. To make this task, the SAIEs receive commands from the PDHU (these commands are described in the “SA-IE 1 PFM Test Report”, table 1 and in the “ SA-IE 2 PFM Test Report”, table 1”).

To perform physics run and calibrations with the SuperAGILE instrument, is then necessary to know:

1. the SAIEs configuration (sRAM included);
2. the commands sintax that the PDHU send to the SAIEs;
3. the commands sintax for the commands received by the PDHU
4. the commands list.

3.1 DESCRIPTION OF SA CONFIGURATION

According to the previous considerations, we have found this set of “structures” to describe the SuperAGILE configuration:

3.1.1 REGIN CONFIG (DC REGISTER _IN FOR “SCIE MODE”)

This structure describe the “register in” that will be sent to SAFEEs DCs with a “CONFIGURATION Start” command from the PDHU to the SAIEs. The same structure is used as “base regins” by the “calibration Start” command.

This structure is a vector of 8 sub-structures. Each substructure describes the regin for one DC. Internally each substructure is subdivided in 3 segments. Each segment describes the regin configuration of the 3 XAA1.2 inside a Daisy Chain.

The “Regin CONFIG” of a SAIE contains 646 bit x 3(XAA1 chip) x 4(DC) x 2(SAFEE boards).

NB: The SAIE uses two different SRAM segments to store the “regin config” for the DCs. One memory segment is for the configuration of the “OBSERVATION MODE”, the other memory segment is for the “CALIBRATION MODE”. Unfortunately the PDHU stores the same “regin config” in both the segments.

The format of “REGIN CONFIG” structure is given later in this document .....

3.1.2 **SAIE DAC**

Inside a SAIE we can configure 8x3 DACs (type AD8800, with 8bit DACs):

1. MGO low threshold DC0-S0
2. MGO low threshold DC1-S0
3. MGO low threshold DC2-S0
4. MGO low threshold DC3-S0
5. MGO high threshold DC0-S0
6. MGO high threshold DC1-S0
7. MGO high threshold DC2-S0
8. MGO high threshold DC3-S0
9. MGO low threshold DC0-S1
10. MGO low threshold DC1-S1
11. MGO low threshold DC2-S1
12. MGO low threshold DC3-S1
13. MGO high threshold DC0-S1
14. MGO high threshold DC1-S1
15. MGO high threshold DC2-S1
16. MGO high threshold DC3-S1
17. S0 HV regulation
18. S0 Energy upper threshold
19. S1 HV regulation
20. S1 Energy upper threshold
21. Cal. amplitude 0
22. Cal. amplitude 1
23. Cal. amplitude 2
24. Cal. amplitude 3

“The SAIE DAC” structure contains 8 x 3 fields.

3.1.3 SAFEE DAC

Inside each SAFEE we can configure 32 DACs (AD8842 type, 8 bit for each DAC).

We use a structure with 64 fields (8 fields for evey DC) containing:

1. Analog threshold DC0-S0
2. Vfs DC0-S0
3. Vfp DC0-S0
4. prebias DC0-S0
5. shabias DC0-S0
6. TrigDelbias DC0-S0

7. TrigWbias DC0-S0
8. ResWbias DC0-S0

8 x 4 x 2 (BYTE VALUES)

3.1.4 NUMBER OF CALPULSES

A configuration word is used to set the number of pulses of a given amplitude to send to the channel during a calibration.

3.1.5 DC MASTER RESET

1 bit is used to enable the master reset generation for a single DC. A structure of 8 fields (1 bit size each) is used to configure the master reset generation option on the 8 DCs.

8 x 1bit values (active = high)

3.1.6 DC SUPPLY (DC SUPPLY SWITCH)

1 bit is used to switch on/off the supplies of the SAFEEs. A structure of 10 fields is used to configure the option for:

1. +-5V S0
2. +-5V S1,
3. +-2V DC0-S0
4. +-2V DC1-S0
5. +-2V DC2-S0
6. +-2V DC3-S0
7. +-2V DC0-S1
8. +-2V DC1-S1
9. +-2V DC2-S1
10. +-2V DC3-S1

10 x 1bit values (active = high)

3.1.7 LATCHUP MONITOR ENABLE

1 bit is used to switch on/off the latchup monitor on the supply lines of the SAFEEs. A structure of 10 fields is used to configure the option for the following lines:

11. +5V S0
12. +5V S1,
13. +2V DC0-S0
14. +2V DC1-S0

15.+2V DC2-S0
16.+2V DC3-S0
17.+2V DC0-S1
18.+2V DC1-S1
19.+2V DC2-S1
20. +2V DC3-S1

10 x 1bit values (active = high)

3.1.8 MGO SAMPLING DELAY

6 bit, (1 value)

3.1.9 VETO ENABLE

1 bit is used to enable/disable the VETO. A structure of 8 fields is used to configure the option for:

1. dummy events enable
2. abt events enable
3. AC TOP veto enable
4. AC LAT veto enable
5. AC ST veto enable
6. AC MCAL veto enable
7. MGO high threshold
8. Energy high threshold

8 x 1bit values (active = high)

3.1.10 **ST VETO CONFIG** (ST_VETO_CONF)

A structure containing two fields is used to configure the timimg of the Anticoincidence signal from the ST:

1. 3bit (time width us)
2. 4bit (time delay us)

array st_veto_config[2] (size=2)
st_veto_conf[0] values in [0, 7]
st_veto_conf[1] values in [0, 15]

3.1.11 **MCAL VETO CONFIG** (MCAL_VETO_CONF)

A structure containing two fields is used to configure the timimg of the Anticoincidence signal from the ST:

1. 3bit (time width us)
2. 4bit (time delay us)

mcal_veto_conf[0] values in [0, 7]

mcal_veto_conf[1] values in [0, 15]
2 values
minicalorimeter

3.1.12 DC ENABLE

1 bit is used to enable/disable the DCs triggers to the SAIE (DC LISTENING ENABLE). A structure of 8 fields is used.
1bit x 4DCs X 2SAFEEs

3.2 FORMAT OF FITS FILE FIELDS for SA CONFIGURATION

Conventional name	*Component to set*	*Description*	*n. of values*	*Values data type*
DC_REGIN_SCIE				
DC_REGIN_CALI				
SAIE_DAC				
SAFEE_DAC				

Table 1Configuration macro parameters

3.2.1 CONFIGURATION SEQUENCE

XAA1 configuration

2 steps :

- 1 SRAM fetch
- 2 XAA1 config

Single command, 3 registers sent configuration control

4 SA COMMUNICATION WITH ST, MCAL AND AC

5 CONFIGURATION REGIN FOR XAA1.2 DAISY CHAINS WITHIN SAGILE SAFEES

In the following tables, bit number 0 is the first bit sent with the programming string for REGIN.

Configuration regin for D.C.#0

bit	*XA*	*DC*
0-645	0	0
646-1291	1	0
1292-1937	2	0

configuration regin for D.C. #1:

bit	*XA*	*DC*
0-645	0	1
646-1291	1	1
1292-1937	2	1

configuration regin for D.C. #2:

bit	*XA*	*DC*
0-645	0	2
646-1291	1	2
1292-1937	2	2

configuration regin for D.C. #3:

bit	*XA*	*DC*
0-645	0	3
646-1291	1	3
1292-1937	2	3

configuration regin for a single XA (I.e. X1):

bit	*significato*	*note*
0	enable/disable test input of ch 0	1: test input is enabled 0: test input is disabled
...		
127	enable/disable test input of ch 127	
128-130	fine threshold bits 0	bit 128: sign bit 129: fine threshold MSB bit 130: fine theshold LSB
...		
509-511	fine threshold bits 127	
512	disable/enable trigger signal from ch 0	1: disable trigger 0: enable trigger
...		
639	disable/enable trigger signal from ch 127	
640	XA address LSB	examples: 0000: address 0 1000: address 1 0100: address 2 ...
...		
643	XA address MSB	
644	Stretcher bit	1: stretcher ON 0: stretcher OFF
645	“test mode” bit of XAA1.2	1: XAA1.2 in “test mode” (working mode for calibration run) 0: XAA1.2 in “Normal” mode

Logic value 1 corresponds to +2v, logic value 0 corresponds to -2v.

XAA1.2 indexing within the SAFEE rises from left to right while looking SAFEE from side with components and with detector on top.

Term “ch” refers to physical channel of X1.

It should be mentrioned that the “real address” produced during calibration run with the SAIEf has inverted sign with respect to physical numeration of SuperAGILE strips: Electronic calibration of first daisy chain

starts from physical channel number #383 (real address=0) and stops with physical channel #0 (real address=383).