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Authors	MEDINACELI VILLEGAS, Eduardo; Dusini, Stefano; SIRIGNANO, CHIARA; FRANCESCHI, ENRICO; AURICCHIO, NATALIA; et al.
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Custodian:	Eduardo Medinaceli		

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Contributors:	Function:	Date:	Signature:
Stefano Dusini	NI-AIV deputy manager		
Chiara Sirignano			
Enrico Franceschi	NI-EGSE manager		
Natalia Auricchio	NISP peduty PA		
Massimo Trifoglio	NI-IWS manager		
Paola Battaglia			
Sebastiano Ligori	NI-ICU-ASW manager		
Andrea Balestra			
Ruben Farinelli			
Gabriele Sirri			
Jean-Claude Clemens			
William Gillard			
Anton Zadeja	TAS-I		
Stamatakopoulos Panagiotis	ADS		
Raoul Grimoldi	OHB-I		
Eduardo Medinaceli	NI-DPU-ASW Manager		
Approved by:	Function:	Date:	Signature:
Luca Valenziano	NI-Italy Local Project Manager		
Authorized by:	Function:	Date:	Signature:
Thierry Maciaszek	NI-Project Manager		

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1. [Change-log](#)

Issue	Date	Page	Description of Change
1.0	09/06/2021	all	First issue

2. [Documents](#)

2.1 [Applicable documents](#)

AD	Title / Author	Document Reference	Issue	Date
1	PLM_TBTV_PLM_Detailed_Performances_Test_Specification	EUCL-ASFT-TS-3-070	3.0	12/05/2021
2	NI-DCU Firmware ICD	EUCL-OPD-ICD-7-002	2.1	06/04/2018
3	NI-WE to Focal Plane ICD	EUCL-OPD-ICD-7-001	4.8	06/04/2018
4	Euclid SIDECAR Engineering Firmware - ICD	EUCL-MKS-ICD-7-001	3.1	09/03/2018
5	Teledyne Input to NISP ICD	EUCL-TIS-TN 7007	2.1	26/08/2014
6	NI-DCU Firmware ICD	EUCL-OPD-ICD-7-002	2.1	06/04/2018

2.2 [Reference documents](#)

RD	Title / Author	Document Reference	Issue	Date
1	NISP Acronyms List	EUCL-IAP-LI-1-001	2.0	04/05/2013
2	EUCLID: DCU FPGA Design Description	EUC-TN-ATI-036	2.0	01/06/2016
3	Teledyne: SIDECAR ASIC Technical Manual	MAN-0013	1.0	20/07/2009
4	Teledyne: SIDECAR ASIC-kit start-up Manual	MAN-0007	1	31/03/2009
5	Teledyne: HAWAII-H2RG Technical Manual	MAN-0001	3	25/09/2007

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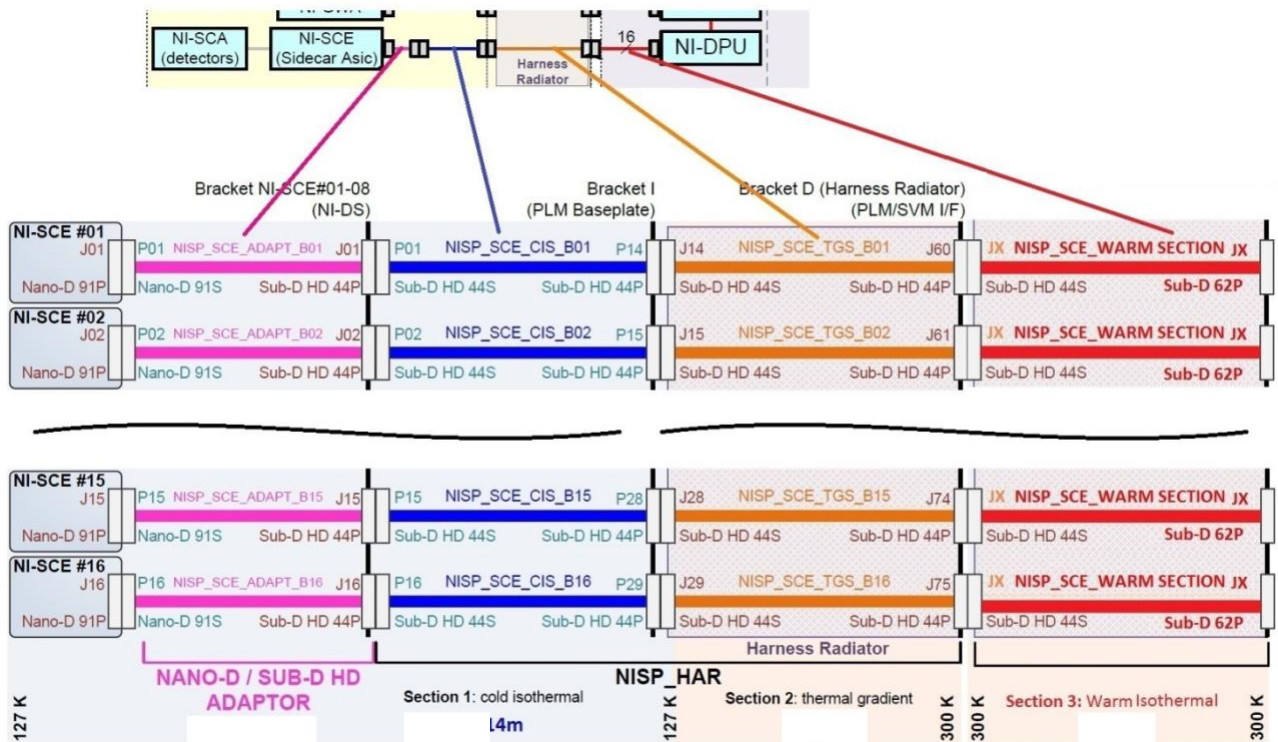
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3. Initial TB/TV activities of NISP in the PLM setup at CSL Liège – NI-CRT (updated to 06/03/21 – used in the discussion with NASA-JPL, Markury Elect. experts)

NISP-team 06/03/21

Setup

NISP is configured in the nominal Flight setup using a dedicated 3m extension (in addition to the nominal 5.5m long) of the harnesses (DCU-SCE). The NI harness is composed by three sections to thermally isolate the focal plane from the warm electronics (“hot”- “thermal gradient” – “cold”); the extension is added in the “hot” section-warm isothermal, the harness is mainly made by copper wires, only the Thermal Gradient part is made by PhBr, for all the detectors.



The 3m extension cable added to Section 3 – warm isothermal is not shown in the scheme above

Operations

The operations of NISP started at the PLM TBTv phase 50. We powered up the entire focal plane (DCU powered up and SCEs bootstrapped) on May 28 at 21:00pm at the operation temperature of ~90K of the CSS.

Results

1st test

On Saturday 29 at ~8:00am - after collecting a full night of nominal telemetry values registered by NISP including the focal plane, we started an acquisition of type MACC(3,2,1). The acquisition was completed for the entire focal plane, but several DCUs reported errors in the parallel science data interface between DCU and SCE; the errors appear for 7

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out of 16 detectors. DCU errors where 0x80000003 (bit0 and bit1), 0x80000004 (bit2), and 0x80000007 (bit0, bit1, bit2), the description of the errors is given below:

bit2	Science_IF_CRC_err_0	This bit goes high when a transmission error has occurred in the science packet and, consequently, a wrong CRC is received. This error is referred only to FIFO_0. This error can be triggered also if a valid synch and block length are received but the transmission by the SCE is interrupted in the half of the packet
bit1	Invalid_block_length_0	This bit goes high if, after the reception of a valid Synch, an invalid block size is detected. This error is referred only to FIFO_0
bit0	Science_IF_Synch_err_0	This bit goes high when the SCE science bus leave the idle state and the first received byte is different from the synch word. This error is referred only to FIFO_0

Since the moment the acquisition started (the exact time was not determined due to the small exposure time and the slower telemetry rate) the telemetry retrieval of the SCEs was not longer available for all the ones experiencing “transmission errors” (the ones which had errors signaled by the associated DCUs described above). A periodic task of the DPU-ASW samples the telemetry each 5 seconds, therefore an error was generated periodically for these SCEs; this of course is non-nominal but in principle it was not a showstopper.

We decided to proceed with a second broadcast exposure and realized that it was not executed by the SCEs. When trying to understand what the state of the SCEs was, and we found the ones that gave transmission errors were unreachable i.e. not able to perform a soft-boot, and also alive command failed.

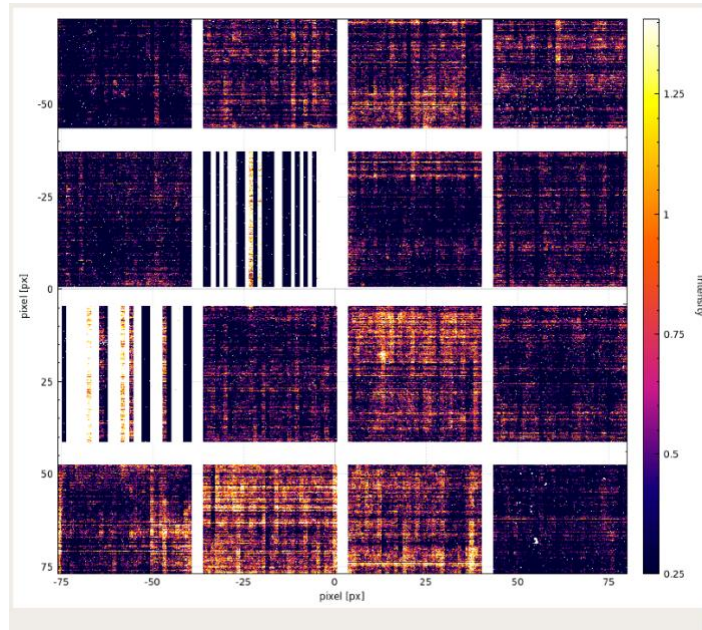
This scenario was reproducible i.e. we perform a full power cycle of the Focal Plane and the DPU units, started all over a first exposure and see again the detector chains with more or less the same errors (always combinations of the errors quoted in the previous table – transmission errors), and again the second broadcast exposure was not executed. Also in this case we were not able to communicate with the SCEs, and in some few cases we had error on the exposure command (statistics not yet available for these occurrences).

Concerning the images produced during the correct acquisition we saw artifacts in some of the images produced (in both cases during the first MACC(3,2,1)). During the first test run artifacts were seen in detectors SCS#31 and SCS#22 as shown in the next plot

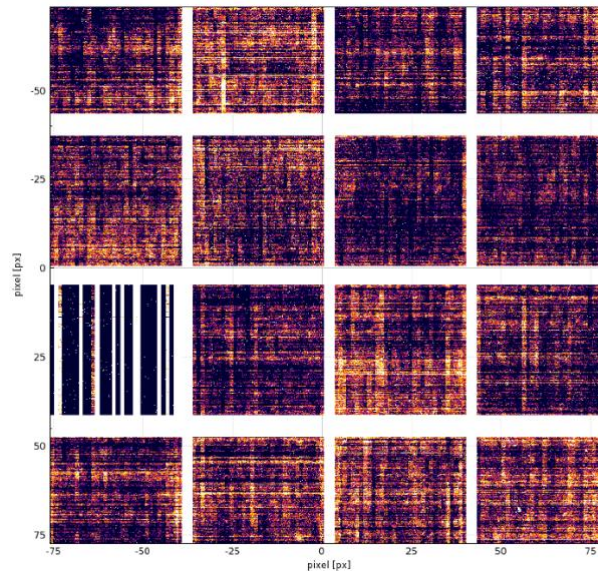


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Then, during the second test run an artifact was seen only in detector SCS#31 (detector SCS#22 was recovered from the image quality point of view) as shown below.



'Artifacts' are related to high dishomogeneities between readout channels, that vary from one acquisition to another (no systematic repetitions has been done, but a single case is presented here). By comparing the reference pixels signal from two full Raw Lines of detector SCS#31 was concluded that the signal level (ref pxs) was homogeneous in both images. The signal compatibility also applies to SCS#22 even if the 'artifact' in the second case disappeared during the second MACC. Below, are shown the two consecutive acquisitions taken with SCS#22 (on the left with the 'image artifact' and at the center without it); on the right of

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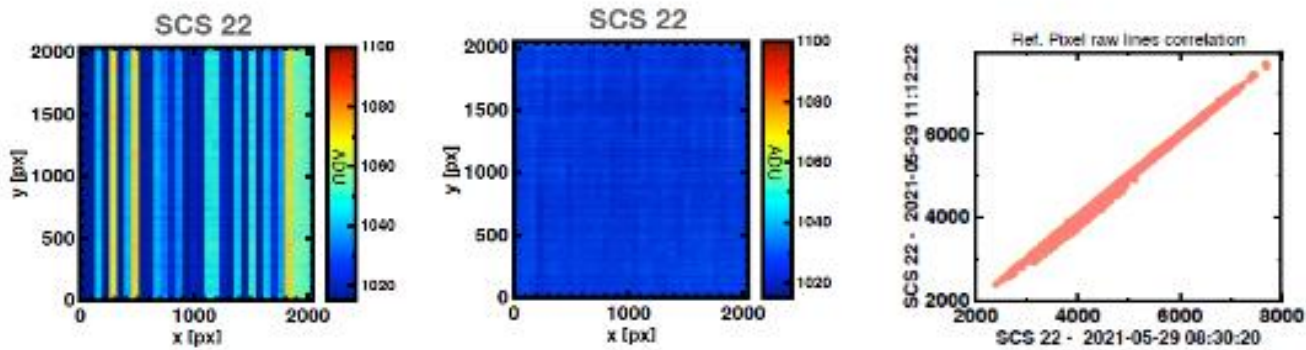
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the same figure is plotted the comparison of reference pixels signal from raw lines showing the expected correlation (same values).



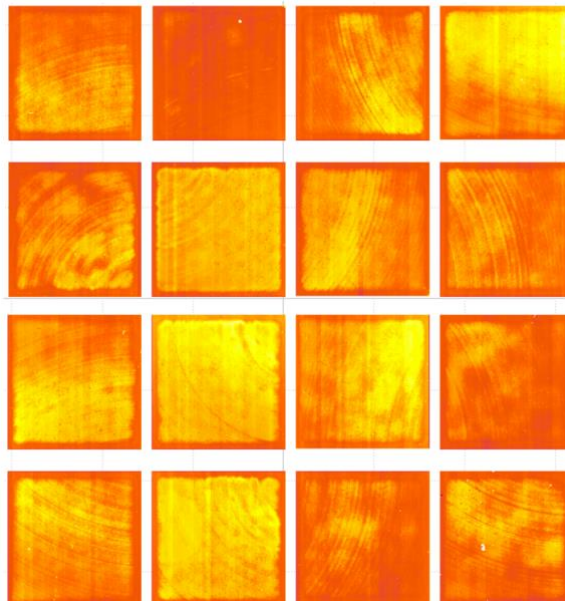
Reference pixels signal from raw lines comparison

It was verified that before entering in the error condition, telemetries of the DCUs, SCEs and SCAs were all nominal, as well as the temperature of the focal plane which was stable (within specifications).

Variant of test 1 – baseline verification

A MACC(1,1,1) was acquired to 'visually inspect' if there were errors in the images (by checking the detectors patten).

Again in this case the same kind of errors were reported by the DCUs but without artifacts in the images as shown below.



For example, below are show images from detectors SCS#31 to SCS#34 (top row), and for comparison are shown the images of the same detectors taken during TV3@LAM (bottom row), which by a visual inspection are compatible.

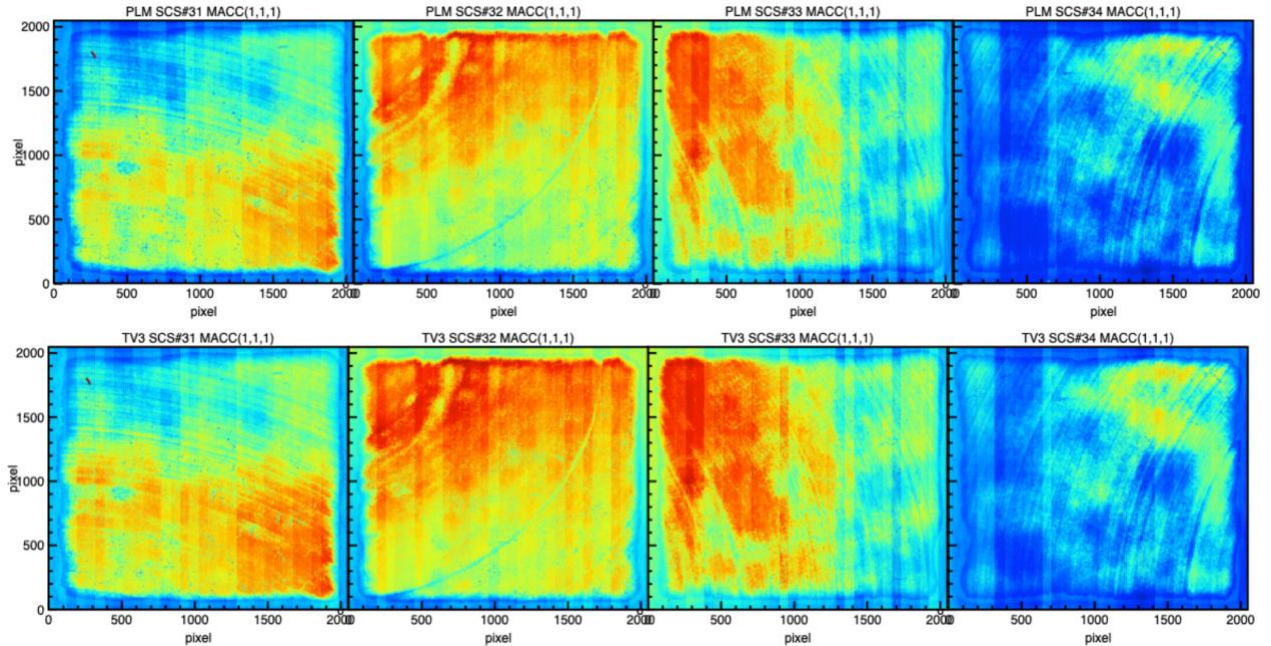
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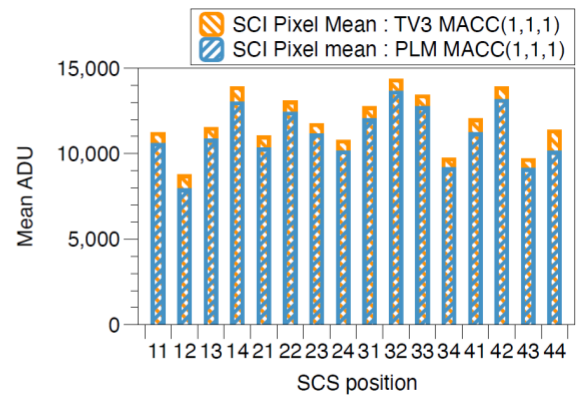
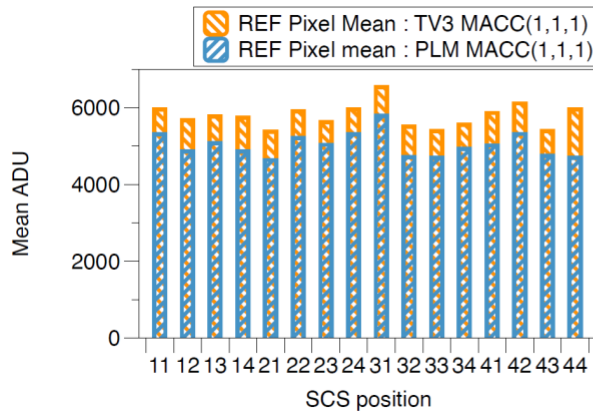


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Also, the baseline was verified and found compatible with TV3 (considering the Temperature differences – slightly hotter than TV3 ~ 3K at SCA level); the following histograms shows the comparison between PLM and TV3 baselines, on the left for the reference pixels, while on the right for science pixels.



2nd test

We repeat a procedure successfully performed at ambient temperature during ART2, the sequence chosen as a benchmark was the one used to determine disconnected pixels using a MAC(1,1,1) with dedicated values of the VRefMain. Again this time we get the usual units in an error state with one of the detectors with error code 0x80000c7 (bit0, bit1, bit2, bit 6 and bit7) – indicating missing lines in the image. The description of errors reported in bits 6 and 7 is in the following table:

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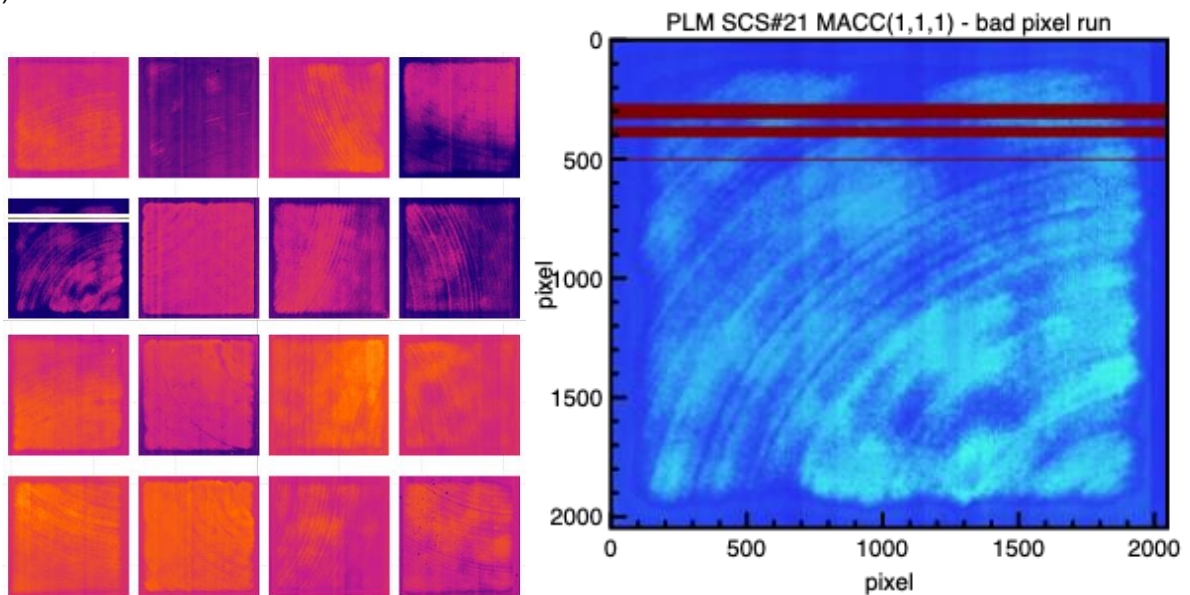
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bit7	Row_timeout	This bit goes high when the SCE has not transmitted a valid science data packet within the defined timeout, during the execution of a MACC operation. The timeout is disabled between two consecutive frames.
bit6	Line_number_error	This bit goes high when the line number received in the header of the packet is not equal to the internal row counter.

By checking the image it was verified that some lines were not transmitted (compatible with the DCU error code); also SCE telemetry recorded the same line errors in the ErrorTable.

The signal of the entire FPA is represented on the left-side of the following display; on the right is shown the image of detector SCS#21 (with a different color scale) with the line transmission errors (indicated with dark red horizontal lines).



3rd test

A broadcast acquisition using the SCE simulated image was done – MACC(1,1,1); in this case we also had the same error condition during the first exposure. The acquisition was correctly start but we got a systematic error for all the detectors in the DPU-ASW related to the data transmission, this error was never seen before and could be related somehow to the nature of the data. We used in the past successfully the ASIC simulated mode without any issues, but in the current conditions we are not able run the procedure. After a full DPU power cycle we acquired a MACC(2,2,2) and we get exactly the same errors for all the detectors.

Using telemetry only (error codes) we are not able to assess the nature of the malfunctioning (which is an error in a very consolidated software function used each time data is transfer to the SVM MMU), dedicated software debugging tools should be used to check the consistency of the data arriving to the DPU (by checking not only CRC which is indeed calculated in all the data transfer processes inside the DPU). We did not perform further studies.

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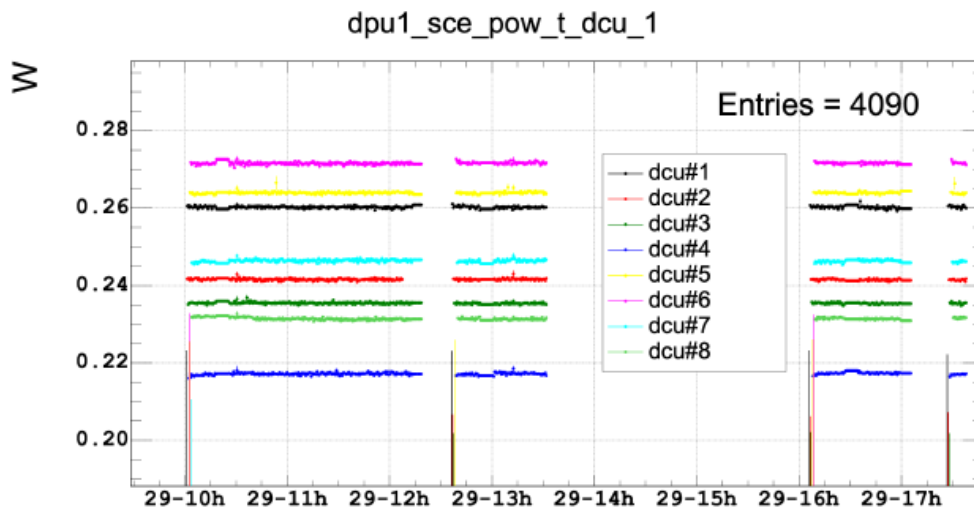
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Focal Plane Telemetry

During all the previous tests before entering the error condition (where we cannot obtain SCE telemetry) and in the ~12 hours period since the first focal plane array (FPA) power up, the telemetry of all the NISP subsystems was nominal.

ASIC's power consumption never shows anomalies before, and while starting the acquisitions. For example, in the next figure are plotted SCE's total power for DPU1; to be noticed that even when SCEs enters in the "non-nominal" state a power drop is not seen. No power reduction is also evident in DCU power lines nor in the DPU main power supply.



SCE's total power down for DPU1, no abnormal power consumption was detected.

Mean values of the VDDIO and VSSIO voltages do not show a significant difference with respect to TV3's values. As well as the mean values of the main SCA's biases.

DCUs telemetries are always nominal even after the error condition. DCU's state registers after the MACC execution are nominal for all the DCUs (0x35) indicating that:

- SIDECAR_CMD_DONE
- SCE_STATUS OK
- MACC (co-adding) DONE
- LCL_STATUS_OK
- SIDECAR_PWR_STATUS OK

While DCUs error registers indicate an error for 9 out of 16 systematically for broadcast exposures. In all the case errors are related with science data transmission between DCU and SCE, error codes are quoted in the results of the 1st and 2nd tests.

At the moment of the acquisition – with a precision that still has to be determined – SCE's telemetry is no longer available for the unites linked to DCUs signaling the error. The error code obtained recursively for each one of these SCEs is SCE_ESHSK - PUS(5,2) event, indicating that SCEs cannot be reached. The telemetry of the entire FPA before entering in the error condition was nominal.

“Stable” FPA configuration

We had a subset of detector chains (DCU-ASIC) showed below that never experience “failures” during acquisitions – green boxes highlight the 7 out of the 16 detector chains working nominally, while the ones with red values are the

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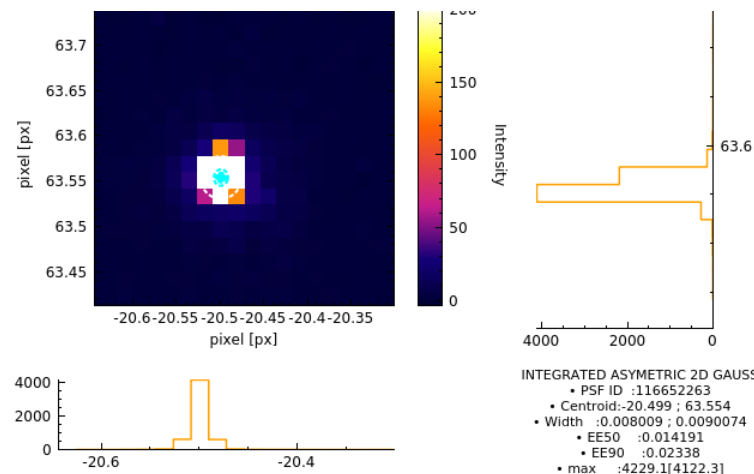
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ones kept powered down. Using this FPA configuration middle long-term stability has been tested by performing several broadcast acquisitions. We acquired short MACC(1,1,1) – MACC(3,2,1) and several nominal MACC(15,16,11) and MACC(4,16,11) consecutively without having problems.



This configuration is being used since the 1st of June intensively, no errors related to the images were found. Detectors were even used successfully for performances tests, e.g. next figure show the NISP PSF in the Y photometric band.



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Open points

- what could be the source of the instability which seems to be present in the DCU-SCE LVDS communication link where the science and telemetry data is being exchange? In a case we clearly see that some lines were not correctly transmitted to the DCU as in the 2nd test.

With the *caveat* that this effect is not present in all the detectors (9 out of 16 detectors).
(The VDDIO and VSSIO power strengths are fixed by the DCUs and cannot be tuned)

- what is a possible cause that could lead the ASICs entering the error condition after the first exposure, considering that this condition is reproducible.

- why simulated data (digital test pattern mode) generated by the ASICs seems to be correctly transmitted but having not nominal format or size inducing the error inside the DPU in the current configuration.

- is the detectors “stable configuration” related to a difference in the setup of the focal plane? (still under investigation)

- by verifying the detector’s baseline – MACC(1,1,1) values are fully compatible with TV3 results given the differences in Temperature, which is an indication of the good health of the SCSs

- having during test 2 a non-correct first image (with the current statistics it is the only occurrence of this condition) is an indication of external perturbances in the communication link?

DPU prime input – OHB-I (info from OHB documentation)

COMMUNICATION I/F VDDIO/VSSIO

The VDDIO value can be set using resistors to be soldered on the DCU board.

The VSSIO value can be set using resistors to be soldered on the DCU board. VSSIO current is drained by the DCU.

VSSIO power supply can be bypassed to provide 0V output at the SCS with a jumper on the DCU.

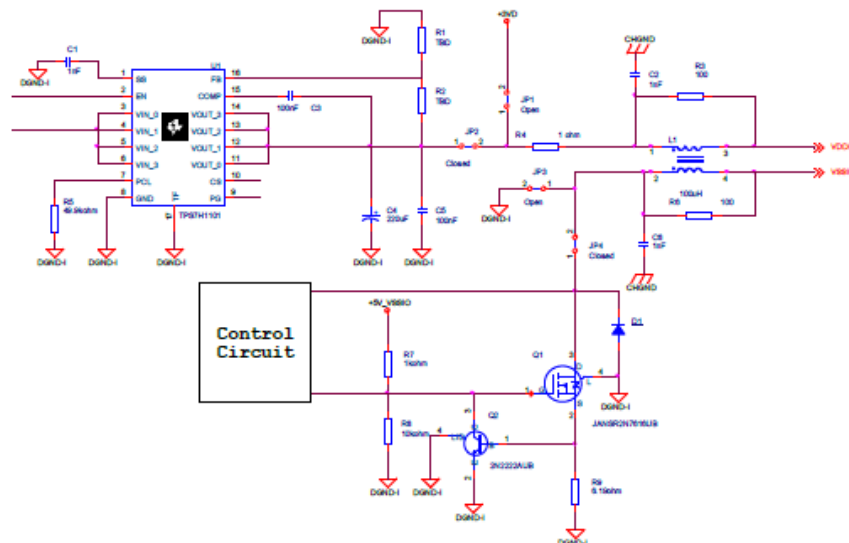


Figure 6-6: VDDIO and VSSIO power supply simplified circuit diagram

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DCU-SIDECAR I/F

The communication uses a parallel interface with two FIFOs sampling asynchronously with a delay of 50ns between them. SCE clock is 10 MHz (100 ns).

Examples of nominal and non-nominal IF between DCU and SCE

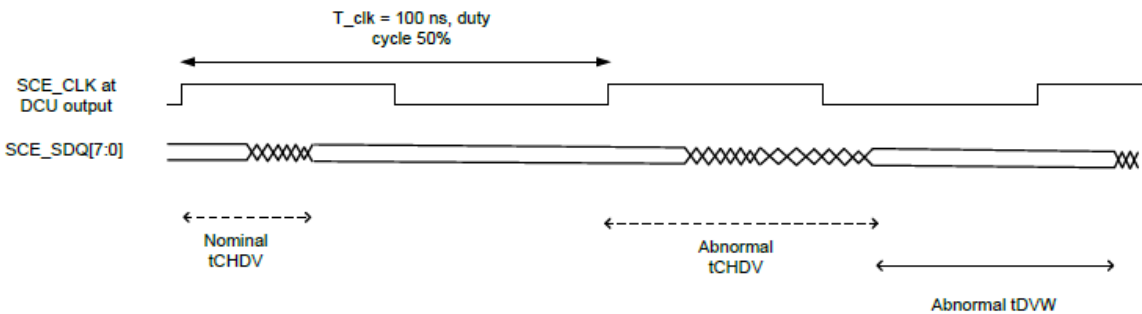


Figure 6-6: SIDECAR science IF abnormal waveform model

Possible errors in the double FIFO mechanism

CRC 0	CRC 1	PACKET VALIDATED	COUNTER INCREMENTED
wrong	wrong	The packets received are discarded	Not incremented
correct	wrong	The packet is taken by the FIFO 0	Incremented FIFO 1 error counter
wrong	correct	The packet is taken by the FIFO 1	Incremented FIFO 0 error counter
correct	correct	The packet is taken by the FIFO identified by the configuration of EDGE_SEL	Not incremented

Table 6-2: double FIFOs CRC errors effect

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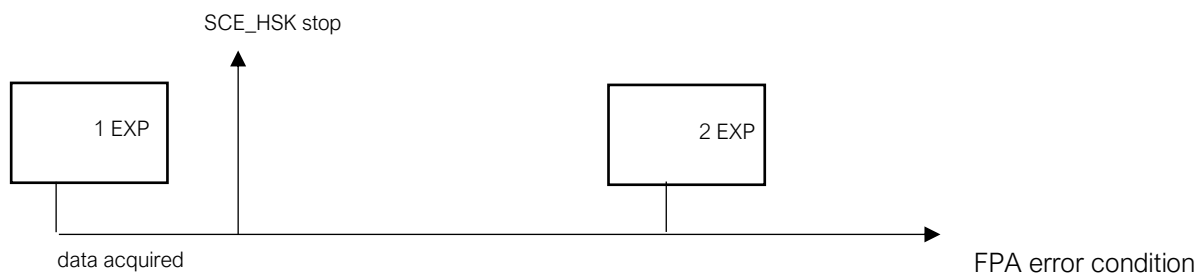
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4. Test report of dedicated NISP activities using ADS TB/TV setup

Test 1: Error encountered using a new test procedure

The usual sequence triggering the error condition was applied to the Focal Plane Array (FPA) of the ADS TB/TV setup. This condition is the final state after the following sequences: a first broadcast exposition was executed which generated data (no quality analysis presented here), nevertheless the DCUs signals non-blocking errors during transmission in the LVDS data link. ASIC TLM (during the acquisition) taken from the first frame stored in the scientific file is nominal (separated report). But two seconds after the exposure started, the SCE housekeeping retrieval stopped working for 9 out of 16 units. This operation is done by a SW task – HSK scanner, that periodically access SCE TLM registers using the DCU TM/TC I/F. Then, a second exposure was issued but the command was not executed (no data generated); this could happen because the serial TM/TC interface is down, or because the ASIC is in a non-nominal state unable to communicate with the DCU. Below is a scheme of the sequence leading to this error condition.



This condition is reproducible, even when the software HSK scanners are not enabled. The same error condition was reached also when operating with the single units that already showed failures during broadcast exposures.

To investigate the state of the FPA the test was repeated in stable thermal conditions without auto-regulated temperature controllers. A SCE power decrease (reduction of ~30%(TBC) of the power in each ASIC) due to a halt of the firmware in 9 units should induce a detectable temperature change; but no temperature change was observed in the system. Therefore, it was inferred that SCE's firmware was running for all the FPA after the 1st exposure.

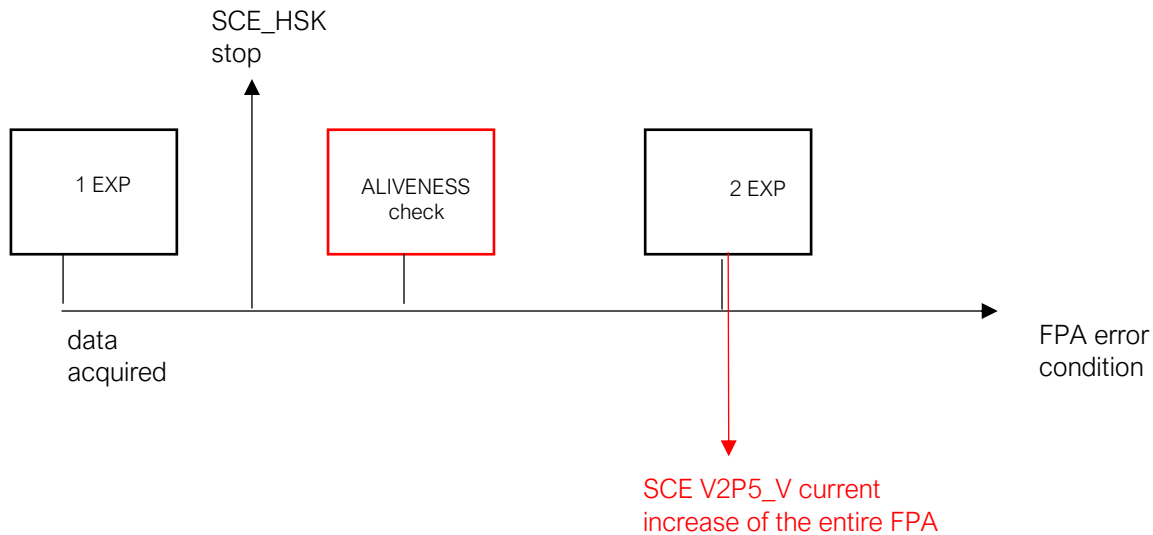
The recovery action applied was a full FPA and DPUs power cycle.

A second sequence was executed to understand the state of the ASICs (not providing TLM). Again, in this case a 1st exposure was executed (with the usual transmission errors), then the ALIVENESS check was applied serially to the entire FPA (all ASICs). The test was done using the SCE_ALIVE command that makes two consecutive SCE accesses (Reads) to get the current line number separated by 250 ms. If the line difference (L0-L1) is equal to zero, it is deduced that the firmware is not running. In this case, the application SW does not longer consider this ASIC for the next broadcast instructions. If for any reason the ALIVE command fails during execution the SCE is also excluded. The new sequence was:



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Results of the previous sequence are summarized in the following table:

DCU-ID	DCU error (after 1 st EXP)	SCE TLM Aliveness	Aliveness check	2 nd exposure
DPU1-DCU1 to 5	no error	available	OK	error
DPU1-DCU6	47	not available	NO	error
DPU1-DCU7	no error	avalibale	OK	error
DPU1-DCU8	C7	not available	NO	error
DPU2-DCU1	44	not available	NO	error
DPU2-DCU2	47	not available	NO	error
DPU2-DCU3	7	not available	NO	error
DPU2-DCU4	4	not available	NO	error
DPU2-DCU5	no error	available	OK	error
DPU2-DCU6	4	not available	NO	error
DPU2-DCU7	no error	available	OK	error
DPU2-DCU8	no error	available	OK	error

Table 1. Test sequence results

After the first exposure, 7 out of 16 DCUs signal errors during transmission, and give an error during the Aliveness check execution. Later, the second exposition failed for the entire FPA.

DCU6 and DCU8 of DPU2 signal SCE line errors (with line error counter 1834 and 48407 respectively), as well as errors in the LVDS FIFO_0 as the other DCUs in error.

The image below (left) shows the data acquired during the 1st exposure (errors and artifacts can be seen in the plot), DPU1-DCU8 failed to transmit the data due to the SCE line errors. (On the right is the map of the DCU/SCE IDs).

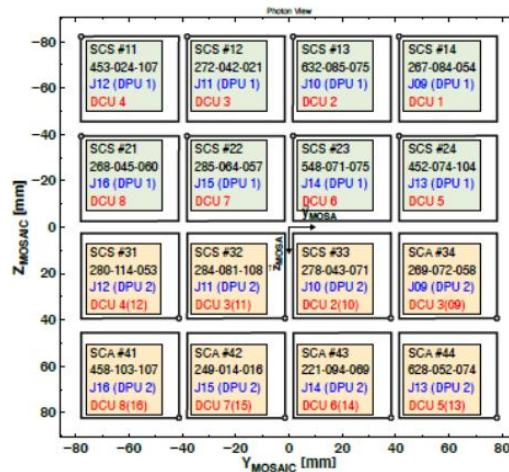
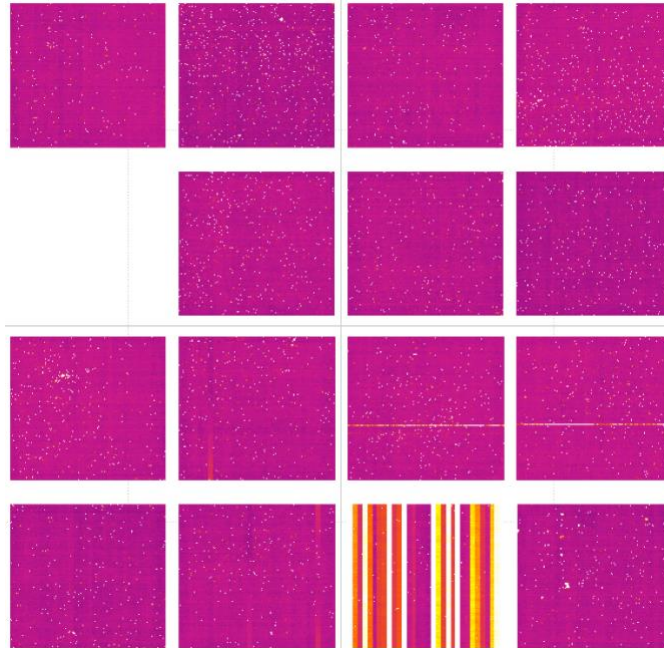
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The ALIVENESS check results are shown in Table 1; only SCEs linked to DCUs without errors have a positive ALIVE test.

Later, when the 2nd exposure was issued, it reflected an increase of ~40% of the SCE power for the entire FPA (16 SCEs) - from 250 mW to ~310 mW. This power increase was almost all due to an anomalous absorption in the V2P5_V current line which increases ~4 times - from 10 mA to ~40 mA.

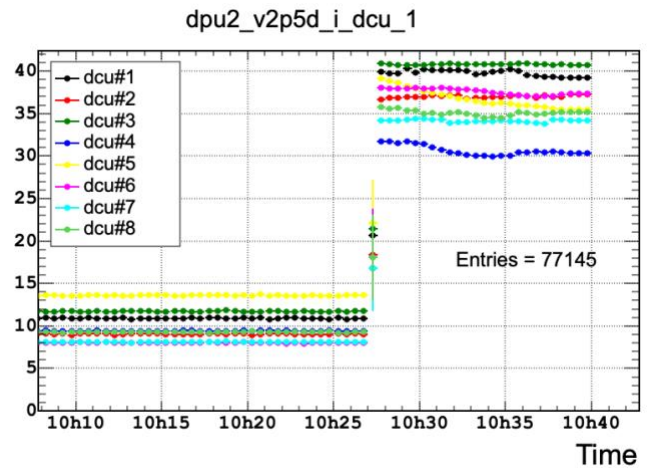
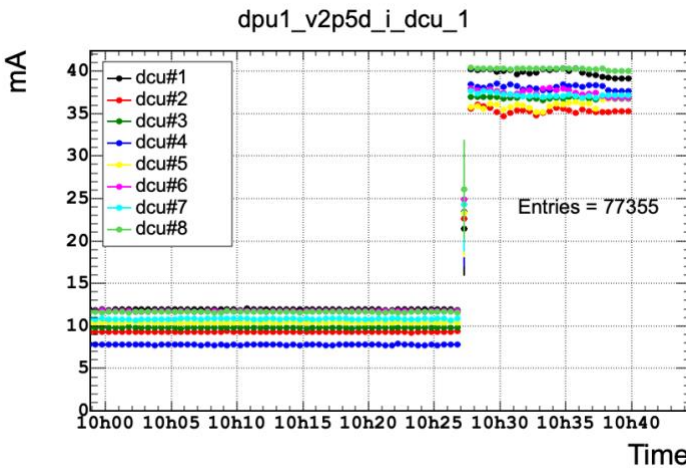
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preparing them for the synchronized operation. In this test case, during the 2nd exposure the DPU's watchdogs were armed; and immediately after, the following operation was executed to prepare the synchronization mechanism:

```
res = WriteSCE(DPU_BRD_DEV, SCE_CMDREG, SCE_CMDSYNC);  
where: SCE_CMDREG = 0x4000,  
       SCE_CMDSYNC = 0x0003
```

At this point the firmware should execute the following steps:

1. Reset and hold internal preamp / SAR ADC finite state machine.
2. Remove ADC and microcontroller clock divider setting.
3. Load Command Register with an acknowledge value.
4. Microcontroller goes to sleep.

Question: is it possible that the above steps are not all executed due to an error condition, resulting in the microcode running with the clock divider reset?

We verified with a stand-alone ASIC readout electronics that if the microcontroller and ADC clock dividers are set to 0x0000, the V2P5_I go from 15 mA to 53 mA (~38 mA increase) leading to a total power of ~440 mW. We also verified that changing the clock frequency to intermediate values of 2.5 and 5 MHz, the current increases proportionally.

The open question is, how a simple command as the ALIVE check could lead to such failure inside the SCE, leading to this anomalous absorption condition observed in the entire FPA.

Do you think that there could already be an error condition at the end of the 1st exposure, even if the data was produced?

We are now adopting the hypothesis of an error occurring during 1st exposure leading to malfunctioning of the LVDS link. Because we observed errors during transmission signaled by the DCUs, and line errors in the SCEs for the first-time. Now we are defining new test procedures to focus our attention in this initial phase.



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Test 2: ASIC's LVDS current mode

The test was conducted using a single DCU which systematically enters in the error condition i.e., DPU2-DCU1.

The following current values were used 1.5, 2.6, 3.5, 5 and 9 mA

In all the cases the "usual error condition*" was triggered - *after a 1st exposure the DCU indicates errors during DCU-SCE transmission, but the image was transferred; instead, the 2nd exposure was not executed.

DPU2-DCU1 errors were all equal to 0x80000007 (transmission done using FIFO_1) for all the current values – same type of error obtained with the LVDS driven in voltage mode.

Error code 0x80000007 corresponds to the following errors (bits 0, 1, and 2 of the error register)

2	Science_IF_CRC_err_0	0	This bit goes high when a transmission error has occurred in the science packet and, consequently, a wrong CRC is received. This error is referred only to FIFO_0. This error can be triggered also if a valid synch and block length are received but the transmission by the SCE is interrupted in the half of the packet
1	Invalid_block_length_0	0	This bit goes high if, after the reception of a valid Synch, an invalid block size is detected. This error is referred only to FIFO_0
0	Science_IF_Synch_err_0	0	This bit goes high when the SCE science bus leave the idle state and the first received byte is different from the synch word. This error is referred only to FIFO_0

Results: No difference has been observed (tested with only a single DCU) with respect to the nominal LVDS voltage mode.



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5. Test report of the 2nd dedicated NISP test activities using ADS TB/TV setup

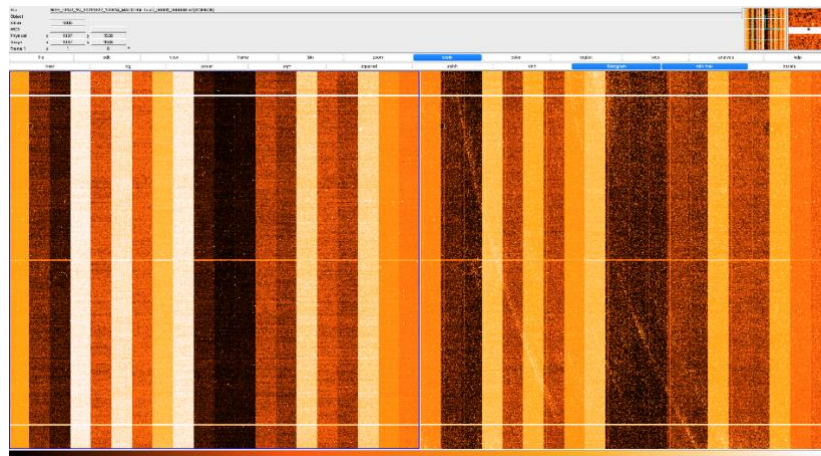
Eight tests were scheduled for these activities (detailed in NISP_test_plane_in_phase_61-70-71.pdf test numbering is referred to this document, test 9 to 12 were discarded). Here are presented only the most relevant results which do not include all the repetitions and the dedicated analysis; more details can be found in the separate presentations. Results are presented sorted according to the importance of the results.

Error condition: during this second test session the focus was on the first broadcast acquisition where some DCUs indicates “recuperable” errors in the communication (errors related to FIFO_0) between the DCU/SCE (LVDS data line); nevertheless, data is produced by all the ASICs.

bit2	Science_IF_CRC_err_0	This bit goes high when a transmission error has occurred in the science packet and, consequently, a wrong CRC is received. This error is referred only to FIFO_0. This error can be triggered also if a valid synch and block length are received but the transmission by the SCE is interrupted in the half of the packet
bit1	Invalid_block_length_0	This bit goes high if, after the reception of a valid Synch, an invalid block size is detected. This error is referred only to FIFO_0
bit0	Science_IF_Synch_err_0	This bit goes high when the SCE science bus leave the idle state and the first received byte is different from the synch word. This error is referred only to FIFO_0

Table 1, “non-blocking” DCU errors related to FIFO_0, “recovered” using FIFO_1.

SCE’s telemetry is not available just after the start of the MACC acquisition. In some cases when the DCU signal a transmission error, in the image can be seen “artifacts”, for example lines with non-nominal values as:



Images from two different detectors showing “horizontal lines” (artifacts) in the same rows.

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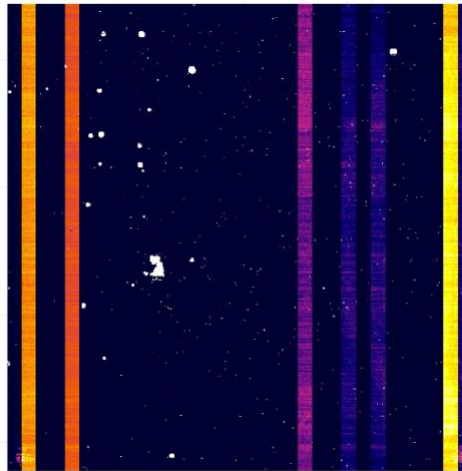
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This kind of “strange” lines were also found in the reference pixels. In these cases, the reference pixel correction performed by the DPU-ASW creates an artifact showing channel-to-channel patterns in the image, like:



Vertical structure induced by the reference pixel correction when a non-nominal row of reference pixel is acquired. This image was acquired at the DPU's lowest operative temperature.

With a lower frequency missing lines were seen in the images, they were reported by the DCU (with error codes including the ones in Table 2) and by the SCE in the error buffer (not null) of the scientific product.

* A dedicated analysis is presented afterwards for RAW data (Test4).

bit7	Row_timeout	This bit goes high when the SCE has not transmitted a valid science data packet within the defined timeout, during the execution of a MACC operation. The timeout is disabled between two consecutive frames.
bit6	Line_number_error	This bit goes high when the line number received in the header of the packet is not equal to the internal row counter.

Table 2, error codes signaled by the DCU in the case of SCE's missing lines; also, combinations of errors in Table 1 are signaled.

As already verified in the previous dedicated test campaign if a second exposure is commanded in this error condition, the exposure it is not executed by the entire focal plane.

General Result Stop of SCE TLM: it was observed that the SCE TLM stops when the DCU signals the transmission error; it was register that in most of the cases this happens just about 2 seconds after the exposure starts.

A different case was observed showing the SCE TLM stop at ~ the middle of a Spectrometric MACC (total length ~10 min), just after the DCU showed the transmission error in the FIFO_0 (combinations of values in Table 1).

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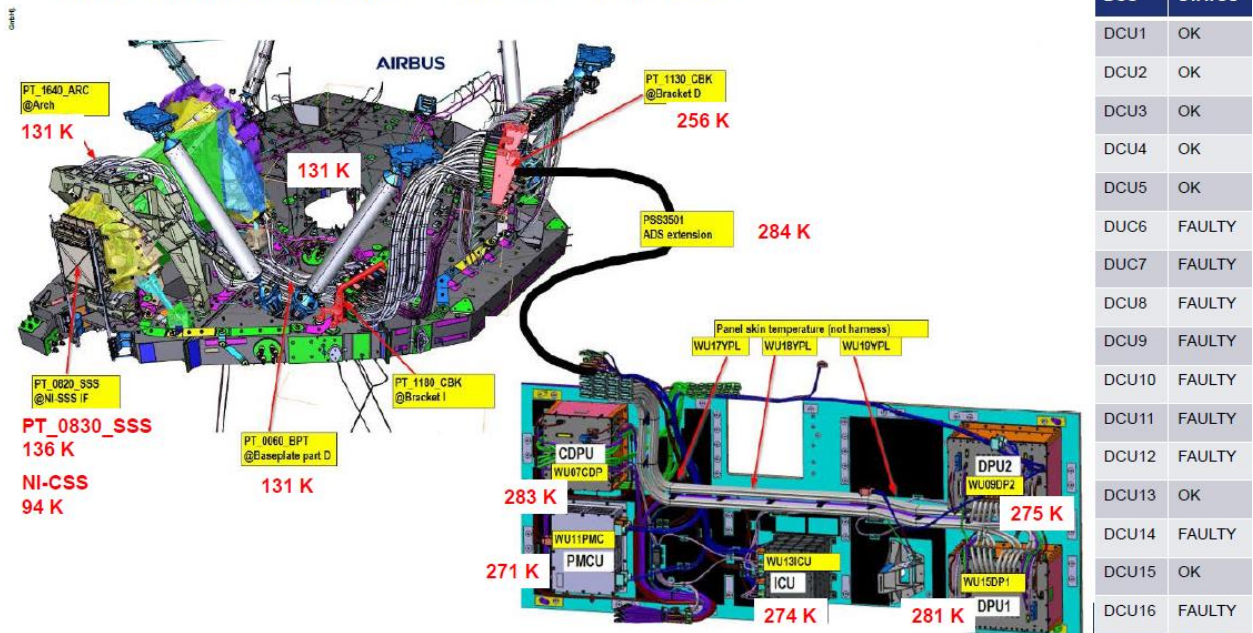
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Test8 change of the operative temperature: CSS (SCAs holder), SSS (SCEs holder), PLM baseplane, ADS extension harnesses, bracket D (thermal interface with the NIOMADA) and Warm Electronics (ICU, DPU1 and DPU2) Temperatures were modified during thermal phases 50c, 61, 60, 70, and 80. During these phases a broadcast exposure using the entire focal plane was issued, testing the error condition, if it was present a second exposure was issued to verify the impossibility to execute it.

A dependence of the number of detector chains working nominally (without entering in the error condition described above, nor in the two consecutive exposures error condition) with the Temperature was found.

Results are given in the following pictures (courtesy of ADS), where the Temperatures of the different components are indicated; as well as a table with the DCU ID (from 1-8 for DPU1 and from 9-16 for DPU2) and the STATUS which indicates units correctly operating (OK) and the ones entering in the error condition (FAULTY).

First Occurrence: 29/05/2021 – 08:30 UTC – PHASE 50c



Confidential	
DCU	STATUS
DCU1	OK
DCU2	OK
DCU3	OK
DCU4	OK
DCU5	OK
DUC6	FAULTY
DUC7	FAULTY
DCU8	FAULTY
DCU9	FAULTY
DCU10	FAULTY
DCU11	FAULTY
DCU12	FAULTY
DCU13	OK
DCU14	FAULTY
DCU15	OK
DCU16	FAULTY

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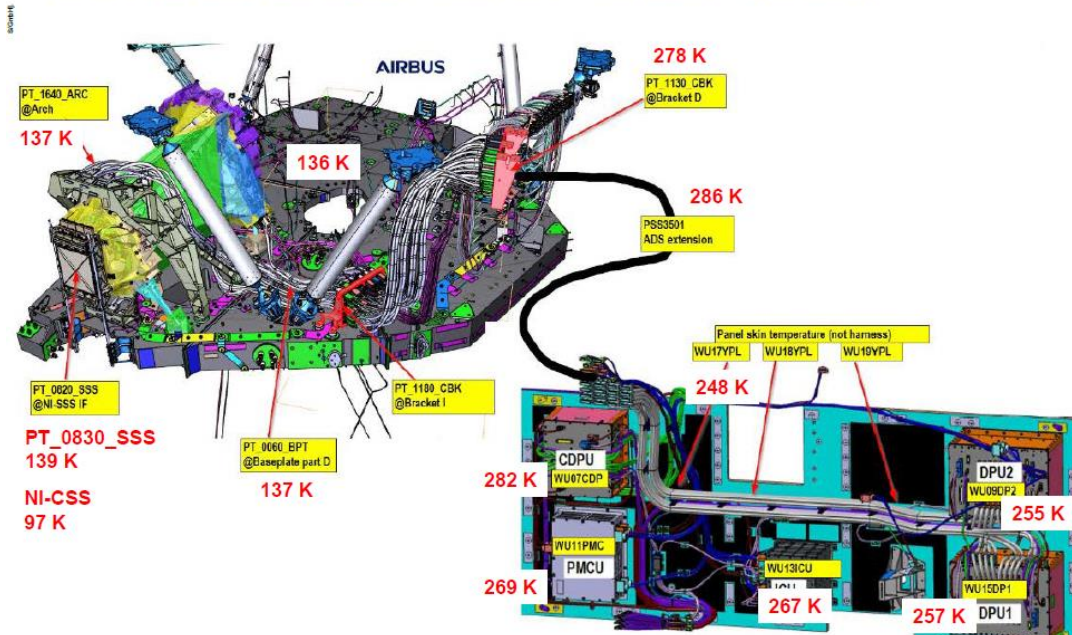
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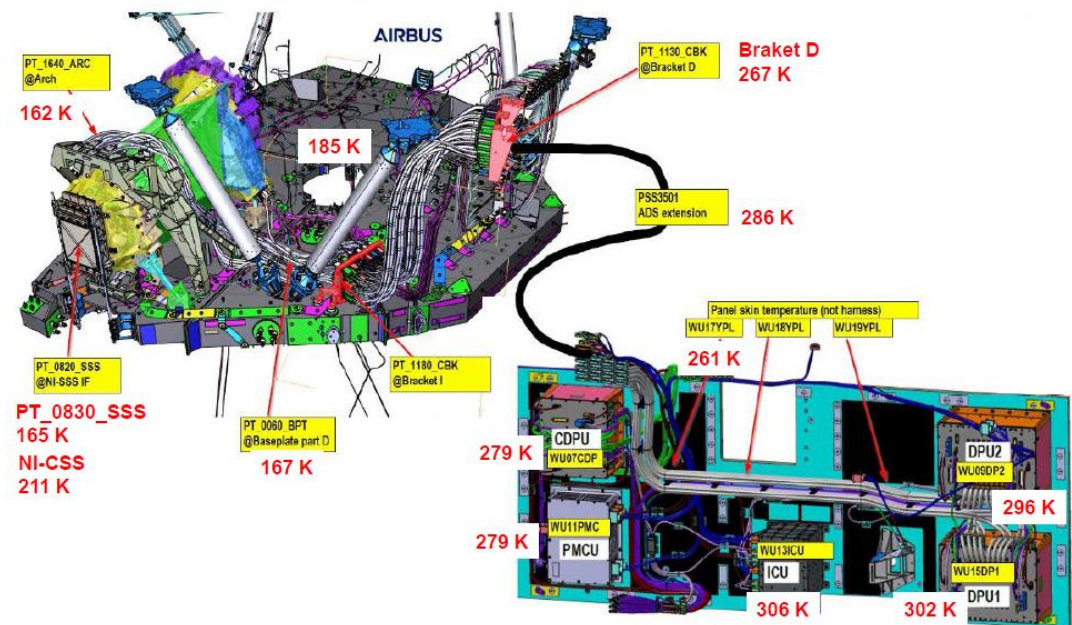
First Occurrence: 29/06/2021 – 11:10 UTC – PHASE 61 – (Test#08)



Confidential

DCU	STATUS
DCU1	OK
DCU2	FAULTY
DCU3	OK
DCU4	FAULTY
DCU5	OK
DUC6	FAULTY
DUC7	FAULTY
DCU8	FAULTY
DCU9	FAULTY
DCU10	FAULTY
DCU11	FAULTY
DCU12	FAULTY
DCU13	FAULTY
DCU14	FAULTY
DCU15	OK
DCU16	FAULTY

First Occurrence: 02/07/2021 – 07:46 UTC Phase 70



Confidential

DCU	STATUS
DCU1	OK
DCU2	OK
DCU3	OK
DCU4	OK
DCU5	OK
DUC6	OK
DUC7	OK
DCU8	FAULTY
DCU9	FAULTY
DCU10	OK
DCU11	FAULTY
DCU12	OK
DCU13	OK
DCU14	OK
DCU15	OK
DCU16	OK

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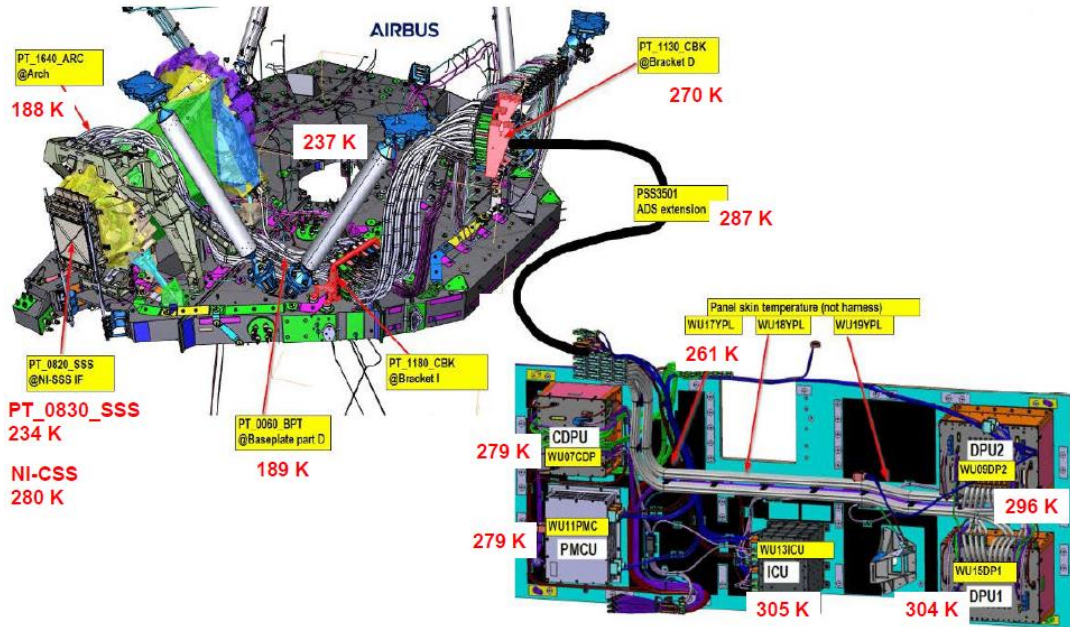
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First Occurrence: 04/07/2021 – 08:40 UTC Phase 80



Confidential

DCU	STATUS
DCU1	OK
DCU2	OK
DCU3	OK
DCU4	OK
DCU5	OK
DUC6	OK
DUC7	OK
DCU8	OK
DCU9	OK
DCU10	OK
DCU11	OK
DCU12	OK
DCU13	OK
DCU14	OK
DCU15	OK
DCU16	OK

The stability of the DCU status was tested during all the phases performing two consecutive broadcast exposures using the entire focal plane. In all the case when there are “Faulty DCUs” (DCUs showing errors during the 1st exposure), the second exposure was commanded but not executed in all 16 lines.

An analysis of the Temperature variation of each component correlated with the number of units is on-going (not reported here).

Test4 SCE Raw data results: Using a configuration at a given temperature with 10 stable DCUs (showing no errors after the 1st exposure), we perform a NI-Engineering Raw mode run acquiring MACCs(15,1,1) (15 groups composed by 1 frame followed by a single intergroup drop frame). In this case we collect 15 raw frames which were non “averaged” (co-added) by the DCUs and not processed by the DPU.

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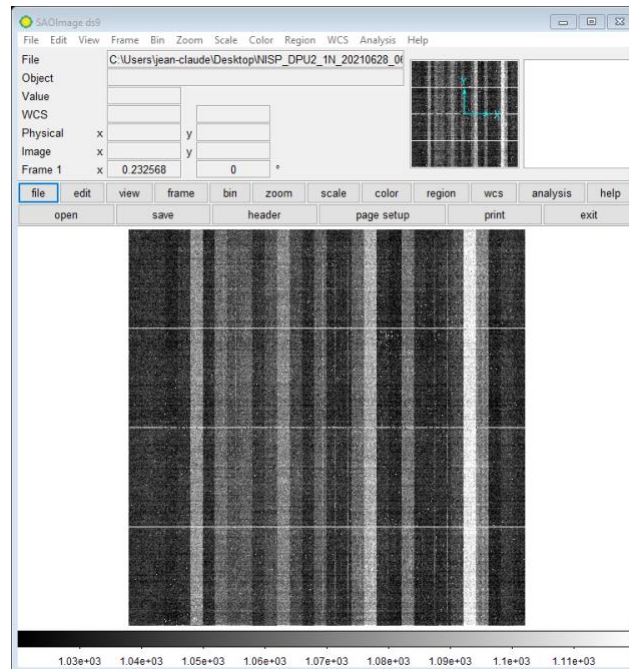
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Results are the following:

DCU1 no error	DCU2 no error	DCU3 no error	DCU4 4
DCU5 no error	DCU6 3*	DCU7 4	DCU8 3
DCU1 (9) 7	DCU2 (10) 3	DCU3 (11) 7	DCU4(12) 4
DCU5(13) no error	DCU6(14) 7	DCU7(15) no error	DCU8(16) 4

Table 3, results of the MACC(15,1,1) 'raw mode' – DCUs IDs labeled in parenthesis correspond to the DPU2. The number besides the DCU ID are the errors reported during the acquisition. For DCU6* we have an internal error in the DPU handling the data produced (still under investigation).

- Only in 6 out of the 10 stable DCUs does not show an error during the 1st exposure, indicating a "degradation" of a stable initial configuration (of 10 DCUs) for the engineering raw mode data acquisition. Several images were showing "non-nominal rows" (artifacts), and in some case multiple ones, for example on data from DCU4(12) are present 3 lines:



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- An extensive analysis of the raw data was performed, and a technical note was written (file Analysis of engineering raw frames.pdf) with all the details. In brief, 'non-nominal' repeated pixel values were observed in a single line which was transmitted to the DCU that detects a transmission error (DCU8(16) error 4). This condition affects the same lines of consecutive frames.

- Two engineering Raw mode MACC(15,1,1) were performed consecutively using DCU8 of both DPUs. For both DPUs the second acquisition was not executed, reproducing a known anomalous condition seen in "unstable" DCUs with normal MACCs (in science mode).

In this case, the raw mode acquisition was done using a single detector (not broadcast).

Test2 DCU status results: DCU registers were inspected before and after the error condition using a MACC(3,2,1). Results for a DCU entering in the error condition are:

Register	Before EXP: Value	After EXP: value
0x0028 FIFO_0_err_counter	0	0x3000
0x002C FIFO_1_err_counter	0	0
0x0034 Frame counter	0	6
0x0038 group counter	0	3
0x0030 row counter	0	0x3000
0x003C DCU_Sync_counter	0	0
0x0004 SIDE CAR_sync_counter	0	0
0x001C DCU status register	0x31	0x35
0x0008 DCU_CONFIG1	0x1C 00 01 01	0xBC 91 03 02
0x000C DCU_CONFIG2	0x10 05 C4 8E	0x10 95 C4 8E
0x0010 HK_CONFIG	0x00 0F FF FD	0x00 0F FF FD
0x0020 Error register	0x80 00 00 00	0x80 00 00 07

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No anomalous telemetry from the DCU is evident before and after the error condition, error register reports the error on FIFO_0.

SCE registers were inspected before the error condition showing nominal values (after the error condition is no longer possible to access the ASIC):

Register	Value
0x6903	0x19 00
0x400d	0x12 04 (NISP nominal)
0x6901	0x00 00
0x4000	0x00 00
0x6904	0x05 05
0x6905	0x05 05

Similar results were obtained for different detection chains, for both DCUs and ASICs.

Test5 SCE simulated images:

Using a DCU that already shows errors handling data was used to perform the same tests using SCE's simulated images.

The results were exactly the same ones, i.e. during the first acquisition of the simulated image the DCU signal a transmission error (in FIFO_0), the SCE TLM stops and it is not possible to acquire the second exposure.

The results were the same using both types of simulated images – Px by Px and Frame by Frame, using two DCUs with different type of MACCs with the same results.

For the "good DCU" for the 2nd EXP the WD_EXP was armed and triggered, while for the "DCU not ok" during the 2nd EXP we obtain SCE_EEXP and the watchdog was not armed.

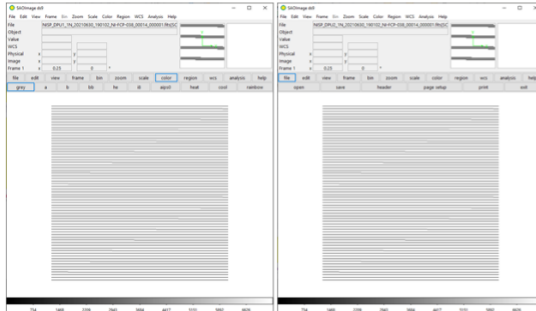
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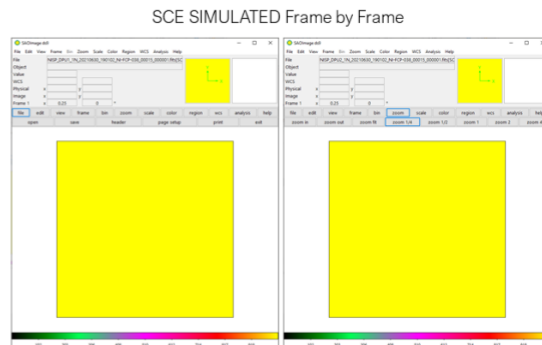


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SCE SIMULATED Px by Px



all images OK,
but 2nd exposure not executed in
both OK and NOT OK DCUs

Simulated Images for the 1st EXP for both (OK and not OK) DCUs showing nominal signal; on top results using a simulated image generated Px by Px, and on the bottom generated frame by frame.

Test1 TM/TC I/F reset results: once that the error condition was engaged, and for a single DCU the TM/TC I/F was reset with a dedicated procedure. The I/F was not recovered, therefore memory locations (0x400D) and registers (0x6903) from the SCE were not accessible through a MEM DUMPs (single SCE read).

Test3 2.5V current issue: It was verified that the sequence leading to an anomalous power consumption of the entire focal plane is not present when is applied only to "stable" DCUs (not entering in the error condition). A mask of 7 stable DCUs was used for the test.

The sequence was composed by a broadcast exposure followed by the SCE firmware aliveness check, and a consecutive second broadcast exposure.

Test7 redundant configuration: redundant sections of DPU1 & 2 were used, the redundancy is only of internal cPCI sectors including a Power Supply Board, a Buffer Board, a Router Board and a CPU. The power supply feeds these components as well as the DCUs; ASICs are powered and controlled by the DCUs – no redundancy on the focal plane array (including DCUs and ASICs).

The same error condition is present using fully redundant configuration, resulting in the same DCUs entering in the anomalous condition as when using the nominal DPU configuration.

Results are summarized in the following tables:

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Nominal DPU configuration results as reference:

DCU1 no error	DCU2 no error	DCU3 no error	DCU4 no error
DCU5 no error	DCU6	DCU7 no error	DCU8
DCU1 (9)	DCU2 (10)	DCU3 (11)	DCU4(12)
DCU5(13)no error	DCU6(14)	DCU7(15)no error	DCU8(16)no error

Fully Redundant DPU configuration (DPU1 red, DPU2 red) results:

DCU1 no error	DCU2 no error	DCU3 no error	DCU4 no error
DCU5 no error	DCU6 7	DCU7 no error	DCU8 7
DCU1 (9) 7	DCU2 (10) c7*	DCU3 (11) 47*	DCU4(12) 4
DCU5(13)no error	DCU6(14) 4	DCU7(15)no error	DCU8(16)no error

Quoted error codes for the fully redundant configuration are just indicative (no errors quoted for nominal configuration -all related to FIFO_0 in principle recuperable). In the latest case errors * indicates a line error counter implying a missing line; those were considered as casual (and not related to the test configuration) because only a single repetition of the test was made.

Test6 DCU simulated images: not successfully executed; therefore, no results.

Systematic transmission errors in FIFO_0 case:

This is an example of communication errors signaled by DCUs.

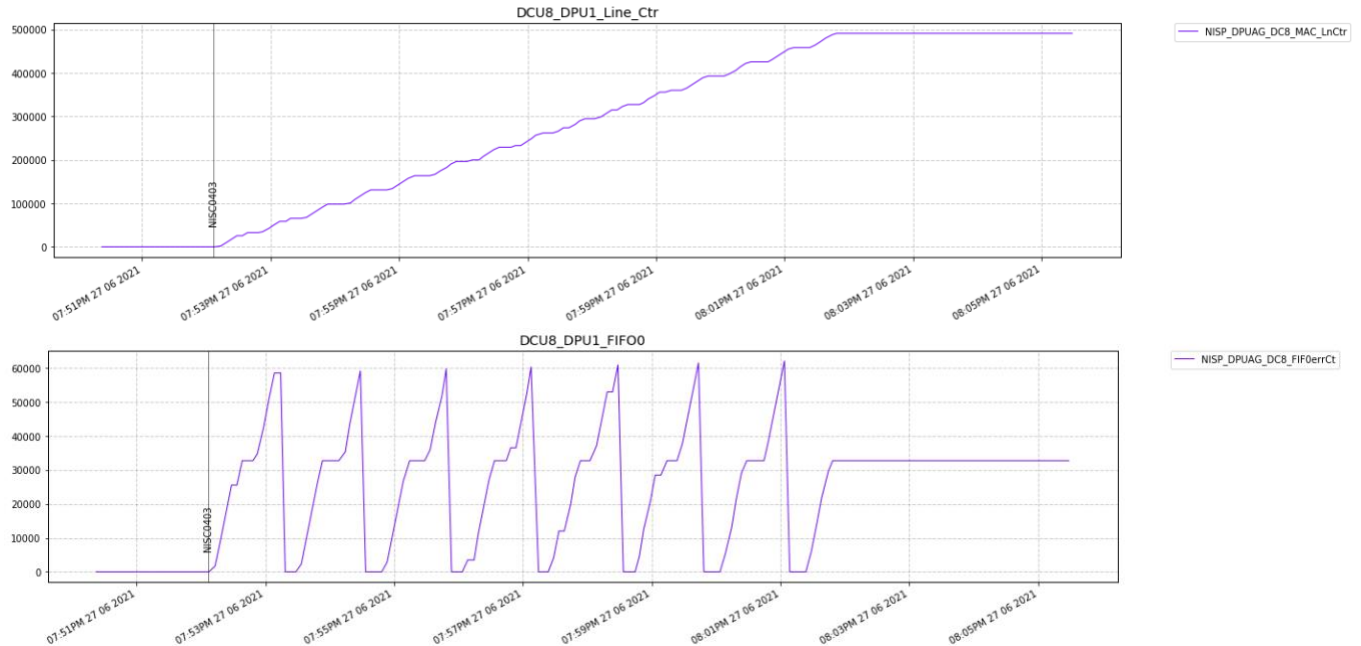
During a nominal spectrometric exposure MACC(15,16,11) using a “faulty DCU” – DPU1-DCU8, the complete data transmission was done using FIFO_1. The DCU signal error code 7 (bits 0, 1, and 2 of Table 1) and the FIFO_0 error counter was systematically increased.

The next figure shows as reference in the top the line counter, where the 15 groups structure can be identified. In the bottom part of the same figure the FIFO_0 error counter is plotted; this variable is allocated in a 16bit variable which is increased after each transmitted line (TBC), the reset to zero is due to the variable wrap-around.



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This DCU failed to perform a second consecutive exposure; even if the above condition showing a wrong communication using FIFO_0 was “recovered” using FIFO_1 (no errors related to FIFO_1 signalled by the DCU).

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6. [Test report of the NISP dedicated test activities using OHB procedures](#)

In this test session the simplest operations that can be applied to a SCE in the “error condition” experienced at CSL were applied. The error condition for this test is defined as having at least one DCU with an error register different than 0x8000 0000 after the first broadcast exposure (this condition was always present during the CSL test campaign at cold). While NISP is in this condition it was not possible to acquire data using the complete focal plane because a consecutive exposure (NISP SCE_EXP command) was not executed. The aim is to exercise bare minimum operations on the SCE implementing read and write operations while NISP was in the error condition described above. The test session was divided in two parts: in the first one, nominal ‘simplified’ operations were performed using the DPU-ASW implementing driver functions; and in a second part ‘higher-level’ software operations – both DPU-ASW and DPU drivers were bypassed using dedicated procedures that execute the read and write instructions by accessing DCU registers using the Load (patch) function were used.

The error condition was triggered executing a broadcast exposure MACC(3,2,1), and all the following tests were done using DCU8 of DPU1 (found with the DCU error register equal to 0x8000 0003 – Science_IF_Sync_err_0 and Invalid_block_length_0 both referred to the data sampling FIFO_0). Tests were held on 07/13/2021 using the NISP PLM setup at CSL in nominal cold conditions, with the support of the OHB industry.

Condition generating a Hardware response

In previous test was observed that starting in the ‘error condition’ (described above) if the SCE_ALIVE and a new exposure are commanded in sequence an anomalous SCE power increase is observed. This sequence was studied and was found in a laboratory test that the power increase can be reproduced when the SCE_Sync() mechanism is applied stand-alone. This mechanism described in appendix A, is part of the NISP broadcast exposure command. During nominal operations it is internally executed during the preparation of the broadcast exposure and is always followed after few milliseconds by successive actions that completes the synchronized acquisition; therefore, in the nominal exposure command the power increase is not triggered.

The anomalous power absorption was documented in Section 4. A dedicated analysis of this condition was done at the Bologna lab with a stand-alone readout system (Markury); a sequence causing this power increase was found and reported to Markus Loose in a dedicated email (7/9/2021), see the Appendix 1 at the end of this report.

This condition was verified using DPU-DCU8 at CSL, starting in the error condition the SCE_ALIVE command was applied to the related SCE followed by an exposure MACC(1,1,1). This induces a total SCE power increases of ~40%, mainly due to a factor 4 increase of the V2P5_I line for all ASICs.

So, this sequence was chosen as an indication of the response of the NISP hardware to the commands issued to the SCEs.

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Tests using nominal NISP commands issued to a SCE in the error condition

Test 1– SCE write using a DPU-ASW command

This test was executed after a full power cycle of NISP. In this case a single SCE write was executed using the SCE_CONFIG command of the DPU-ASW; this command executes a single SCE write of a given register (address) with a given value.

So once in the error condition, using the NISP command SCE_CONFIG the SCE_sync() was engaged writing in register address = 0x400 the value = 0x003. The command was accepted and partially executed rising a high-level error before completion SCE_ECONFIG. Nevertheless, the power increase in the V2P5_V current was verified (~30 mA), see Figure 1. This implies that the command execution induced a hardware response, then it can be inferred that the SCE write function was executed, showing that the DCU-SCE TM/TC I/F was working.

To test the state of the SCE a MEM DUMP (which implements a SCE read instruction) was done without success – due to the so-called 'loss of communication condition'. Nevertheless, a second SCE write operation was done successfully executing DPU-ASW command SCE_Awake. This last command restarts the ASIC firmware by writing at register address = 0x6903 the value = 0x1900; and as a consequence, the current decreases to the nominal value – see Figure 1.

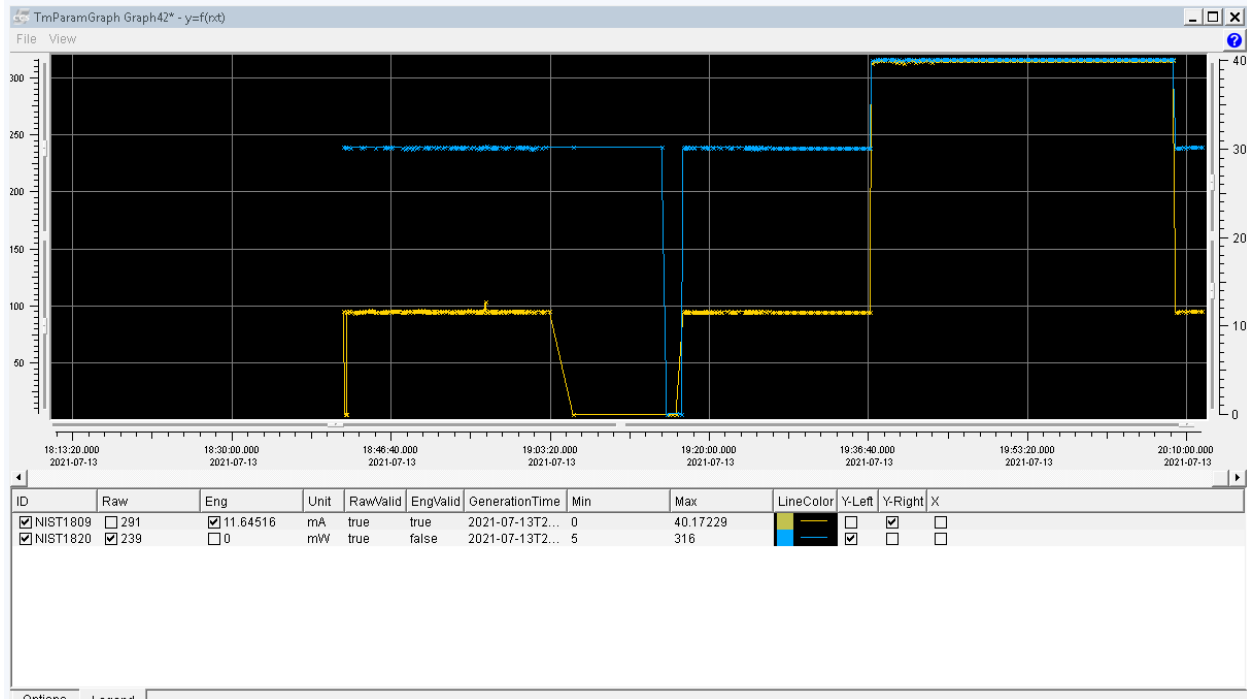


Fig. 1, NISP (DCU) telemetry showing the increase at around 19:36:40.0 and successive decrease at around 20:20:00.0 of the V2P5_V current - NIST1809 (yellow) and total power – NIST1820 (blue), associated to the execution of SCE_CONFIG and SCE_AWAKE commands respectively.

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Test 1 conclusion:

This test demonstrates that a SCE write instruction was executed using the DPU-ASW (nominal NISP commanding) causing a hardware response when NISP was in the error condition; and also showed that a SCE read implemented in a DPU-ASW command fails during this condition.

Tests using non-nominal read and write instructions bypassing the DPU-ASW and DCU drivers issued to a SCE in the error condition – low level SIDECAR access

For the following tests the test procedures were prepared by OHB-I: DPU/DCU prime (R. Grimoldi).

Two different procedures were provided to execute a single SCE read and write. Each procedure is composed by several Load (patch) of different DCU registers performed in sequence one at the time, as a result read/write operations are implemented bypassing the DCU drivers (and DPU-ASW instructions). We will refer to these operations as *low-level SCE access*.

The main differences with respect to nominal operations using driver calls implemented in the DPU-ASW commands is that there are not timing constrains (no SW nor HW timeouts) and there are no intermediate tests over the single operation, and there are not done the recovery actions implemented by the software in case of a specific set of communication errors (TM/TC reset in case of one of the following errors CRC, parity, timeout or acknowledge).

Both test procedures (read and write) were validated using a DCU which was not in the error condition (DPU1-DCU5). Only then, the procedures were applied to DPU1-DCU8 (in error 0x8000 0003 - errors described above in section 2nd test). DCU configuration registers were also DUMPED before and after applying the procedure to look for anomalies in the DCU, no anomalies were found. Registers changed during the test procedure were also verified.

Test 2 – SCE write with low-level ASIC access

Using the low-level access to the ASIC the SCE_Sync process was engaged (writing in register address = 0x400 the value = 0x003) triggering the current increase of the SCE (by about ~30 mA); proving that the SCE write instruction was executed inducing a hardware response, see Figure 2.



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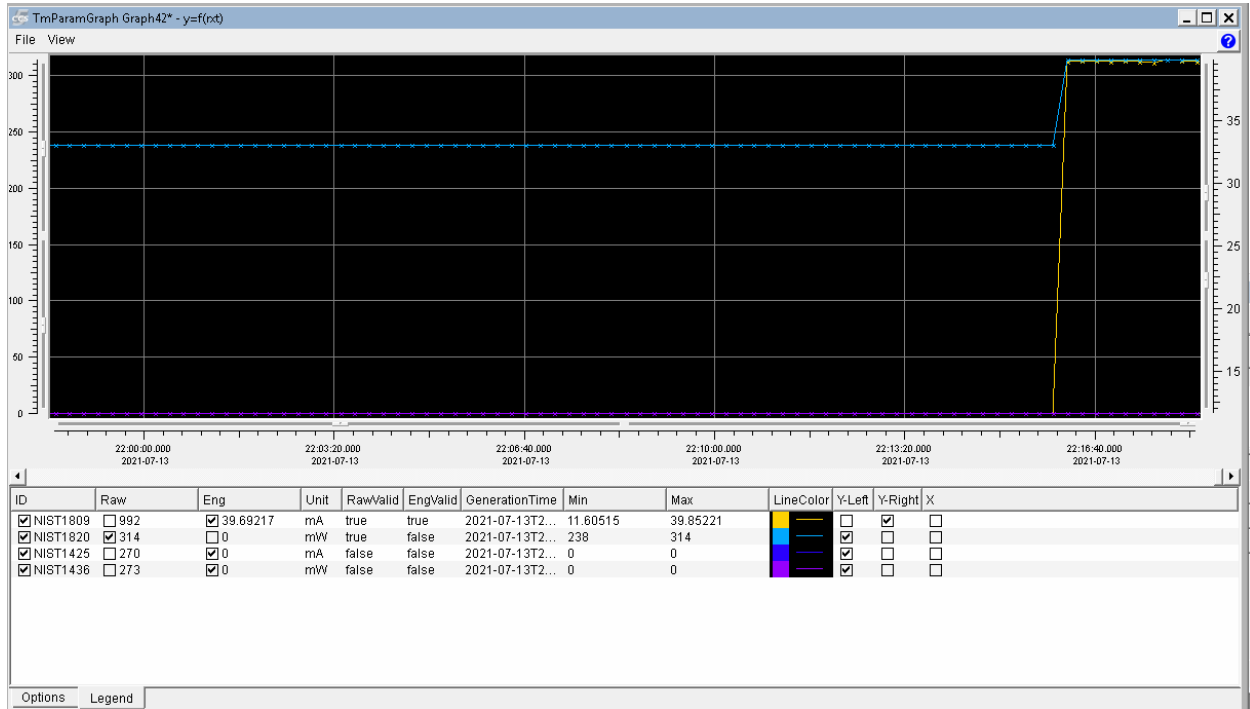


Fig. 2, NISP (DCU) telemetry showing the increase at around 22:16:40.0 of the V2P5_V current - NIST1809 (yellow) and total power – NIST1820 (blue), associated to the execution of SCE write executed with a low-level access.

Test 2 conclusion:

a SCE write was successfully executed using a low-level access (bypassing the DCU drivers and DPU-ASW) proving that the electrical interface was working while NISP in the 'error condition'.

Test 3 – SCE read with low-level ASIC access

This test was executed after test 2, so the ASIC was already in the high current absorption state (triggered by test 2).

The dedicated OHB procedure to read the address = 0x6903 register was applied to DCU8. The value found at the end of the procedure was 0x1901 which is compatible with the state provoking the high current absorption (stopped ASIC's microcode). These values were accessed directly from the following DCU registers:

DCU Address	Value
0x00000400	80006903
0x00000404	19011901

Table 1, DCU registers accessed during the low-level SCE read.

Test 3 conclusion: a SCE read instruction was successfully executed using a low-level access proving that the electrical interface was working while NISP in the 'error condition'.

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Test 4 – loop of SCE read with low-level access

The same procedure applied in test 3 (low-level read access to ASIC) was repeated in loop. Between two consecutive repetitions of the read procedure, a scan of the DCU telemetry using nominal NISP procedures (enabling the DPU-ASW telemetry scanners only for that single DCU) was applied.

The procedural steps are summarized here:

1. trigger the error condition (perform a single broadcast exposure with the entire focal plane and choose a DCU with an error register different than null, i.e. DCU8-DPU1).
2. perform the low-level SCE read instruction and check expected results (DCU registers: Address and Value shown in Table 1.)
3. enable for 1 minute the DCU HSK scanners and check DCU telemetry
4. disable DCU HSK scanners
5. re-start the procedure from point 2.

The complete sequence was repeated successfully for 22 cycles.

At the end of the sequence a nominal exposure was commanded to the single SCE associated to DCU8 (non-broadcast), and was verified that the error condition was still present, i.e. the exposure command was not executed (rising error SCE_EEXP), and no data was generated. The end of exposure watchdog was armed and triggered indicating that at least a single SCE read was executed before arming the watchdog, nevertheless the exposure command failed during the SCE write execution.

Test 4 conclusion: a series of consecutive low-level SCE read instructions were executed successfully showing that the at the electrical level the DCU-SCE TM/TC I/F was correctly working while NISP was in the error condition.

Final remarks

The conclusions of this dedicated test session are:

- Single SCE write function applied while NISP in error condition (described in the first paragraph) works correctly triggering a hardware response both using a simple NISP command and by a low-level access.
- Single SCE read function applied while NISP in the error condition works correctly only when the low-level access is performed.

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Appendix A – analysis of the power increase during SCE sync

The SCE_sync() processes is embedded in the NISP Broadcast SCE exposure command (is the 1st operation done internally). This operation is completely handled by a single write instruction of the ASIC firmware:

```
WriteSCE(DPU_BRD_DEV, SCE_CMDREG, SCE_CMDSYNC);  
where: SCE_CMDREG = 0x4000,  
       SCE_CMDSYNC = 0x0003
```

when the EEF receives a synchronize command from external host, the code will perform the following steps:

1. Reset and hold internal preamp / SAR ADC finite state machine.
2. Remove ADC and microcontroller clock divider setting.
3. Load Command Register with an acknowledge value.
4. Microcontroller goes to sleep.

Then inside the DPU-ASW exposure command, is executed the EEF routine SyncEnable() that prepares the ASIC for the synchronization signal. Then, to start the synchronous acquisition the SyncSend() instruction is executed broadcast.

In our lab we 'manually' execute the SCE_sync() procedure using the Markury electronics, without doing the following steps implemented in the exposure command i.e. SyncEnable() and SyncSend(); provoking a very similar power increase as the one observed (of 30 mA) during the PLM CSL test campaign. The following email reports the results of the measurement:

Subject: Re: Webex: Communication anomalies between SCE and DCU (NISP Warm Units) during PLM TVAC campaign
Date: Fri, 9 Jul 2021 12:57:26 +0200
From: Eduardo Medinaceli <eduardo.medinaceli@inaf.it>
Organization: INAF-OAPd
To: Markus Loose <markus.loose@markury-scientific.com>
CC: Pniel, Moshe (US 7700) <moshe.pniel@jpl.nasa.gov>, Holmes, Warren A (389I) <warren.a.holmes@jpl.nasa.gov>, Jhabvala, Murzy D. (GSFC-5500) <murzy.d.jhabvala@nasa.gov>, Augustyn Waczyński <Augustyn.Waczynski-1@nasa.gov>, allan.j.runkle@jpl.nasa.gov, Mehta, Jitendra S (US 5150) <jitendra.s.mehta@jpl.nasa.gov>, thierry.maciaszek@lam.fr, clemens@c ppm.in2p3.fr, Giuseppe.Racca@esa.int, Stefano Dusini <stefano.dusini@pd.infn.it>, Paolo Strada <Paolo.Strada@esa.int>, Remi Barbier <rbarbier@ipnl.in2p3.fr>, CLEMENS Jean-claude <jean-claude.clemens@univ-amu.fr>, gillard@c ppm.in2p3.fr <gillard@c ppm.in2p3.fr>

In the lab we put both the clock divider set to 0 and the micro-controller in halt, performed during the SCE_sync(). We immediately obtain an increase of the V2P5_V current (VDD1) of 30mA, plus a small increase in the VDDA current, confirming that the anomalous power consumption is compatible with this scenario:

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	Voltage (V)	Current (mA)	Power (mW)
VDDA1	3.2460	52.5000	170.4144
VDDA2	0.0366	-0.0029	-0.0001
VDDA3	0.0363	-0.0029	-0.0001
VDDA4	0.0342	-0.0033	-0.0001
VRef1	3.2939	0.0199	0.0656
VRef2	0.0043	-0.0008	-0.0000
VRef3	0.0003	-0.0010	-0.0000
VRef4	0.0003	0.0004	0.0000
VDD3p3_1	2.8416	31.7448	90.2062
VDD3p3_2	2.8399	3.2992	9.3691
VDD3p3_3	2.8399	3.2373	9.1935
VDD3p3_4	2.8399	3.2992	9.3691
VDD1	2.4744	15.8984	39.3393
VDD2	2.4736	1.4347	3.5490
VDD3	2.4736	1.4136	3.4966
VDD4	2.4735	1.4242	3.5227
VDDIO1	3.1862	75.8654	241.7203
VDDIO2	3.1819	15.3005	48.6840
VDDIO3	3.1824	15.2043	48.3857
VDDIO4	3.1818	15.3005	48.6831
B0 Total Pwr	0.0000	0.0000	300.0255
B1 Total Pwr	0.0000	0.0000	12.9180
B2 Total Pwr	0.0000	0.0000	12.6900
B3 Total Pwr	0.0000	0.0000	12.8917

Note: Total Pwr = VDDA + VREF + VDD3p3 + VDD

6903 = 1900
 6904 e 6905 = 0505

	Voltage (V)	Current (mA)	Power (mW)
VDDA1	3.2484	65.3192	212.0537
VDDA2	0.0481	-0.0025	-0.0001
VDDA3	0.0479	-0.0033	-0.0002
VDDA4	0.0458	-0.0025	-0.0001
VRef1	3.2936	0.0203	0.0669
VRef2	0.0043	-0.0008	-0.0000
VRef3	0.0003	-0.0008	-0.0000
VRef4	0.0002	0.0004	0.0000
VDD3p3_1	2.8419	31.9531	90.8062
VDD3p3_2	2.8401	3.4212	9.7166
VDD3p3_3	2.8402	3.4049	9.6706
VDD3p3_4	2.8401	3.4212	9.7166
VDD1	2.4594	45.3646	111.5702
VDD2	2.4567	4.6289	11.3720
VDD3	2.4569	4.5996	11.3006
VDD4	2.4567	4.6224	11.3560
VDDIO1	3.1857	75.5289	240.6150
VDDIO2	3.1815	15.3966	48.9842
VDDIO3	3.1819	15.3005	48.6840
VDDIO4	3.1814	15.3966	48.9823
B0 Total Pwr	0.0000	0.0000	414.4971
B1 Total Pwr	0.0000	0.0000	21.0885
B2 Total Pwr	0.0000	0.0000	20.9710
B3 Total Pwr	0.0000	0.0000	21.0725

Note: Total Pwr = VDDA + VREF + VDD3p3 + VDD

6903 = 1901
 6904 e 6905 = 0000

uC STOPPED Δcurrent = 30 mA
 clock div STOPPED

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