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The Ariel Instrument Control Unit its role within the Payload and B1 Phase design

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Abstract:	Ariel, the Atmospheric Remote-sensing Infrared Exoplanet Large-survey mission, has been selected in March 2018 by ESA for the fourth medium-class mission (M4) launch opportunity of the Cosmic Vision Program, with an expected lift off in 2028. It is the first mission dedicated to measuring the chemical composition and thermal structures of the atmospheres of hundreds of transiting exoplanets, enabling planetary science far beyond the boundaries of our own Solar System. Its Payload (P/L) has been designed to perform transit spectroscopy from space during primary and secondary planetary eclipses in order to achieve a large unbiased survey concerning the nature of exoplanets atmospheres and their interiors, to determine the key factors affecting the formation and evolution of planetary systems. Ariel will observe hundreds of warm and hot transiting gas giants, Neptunes and super-Earths around a wide range of host star types, targeting planets hotter than ~600 K to take advantage of their well-mixed atmospheres. It will exploit primary and secondary transit spectroscopy in the 1.10 to 7.80 μm spectral range and broad-band photometry in the optical (0.50 - 0.80 μm) and Near IR (0.80 - 1.10 μm) . One of the two instruments of the Ariel Payload is the IR Spectrometer (AIRS), providing low-resolution spectroscopy in two IR channels: Channel 0 (CH0) for the 1.95 − 3.90 μm band and Channel 1 (CH1) for the 3.90 − 7.80 μm range. AIRS is located at the intermediate focal plane of the telescope and common optical system and it hosts two HgCdTe-based hybrid IR detectors and two cold front- end electronics (CFEE) for detectors control and readout. Each CFEE is driven by a Detector Control Unit (DCU) part of AIRS but hosted within and managed by the Instrument Control Unit (ICU) of the Payload.
Response to Reviewers:	All the requests for revision have been processed and implemented; some architectural choices and/or design lacks have been commented and justified in relation to present design Phase (end of B1)

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The Ariel Instrument Control Unit

its role within the Payload and B1 Phase design

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Abstract Ariel, the Atmospheric Remote-sensing Infrared Exoplanet Large-survey mission [1], [3], [6], has been selected in March 2018 by ESA for the fourth medium-class mission (M4) launch opportunity of the Cosmic Vision Program, with an expected lift off in late 2028. It is the first mission dedicated to measuring the chemical composition and thermal structures of the atmospheres of hundreds of transiting exoplanets, enabling planetary science far beyond the boundaries of our own Solar System.

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Its Payload (P/L) [2], [4], [10], has been designed to perform transit spectroscopy from space during primary and secondary planetary eclipses in order to achieve a large unbiased survey concerning the nature of exoplanets atmospheres and their interiors, to determine the key factors affecting the formation and evolution of planetary systems [7], [9].

Ariel will observe hundreds of warm and hot transiting gas giants, Neptunes and super-Earths around a wide range of host star types, targeting planets hotter than $\sim$600 K to take advantage of their well-mixed atmospheres. It will exploit primary and secondary transit spectroscopy in the 1.10 to 7.80 μm spectral range and broadband photometry in the optical (0.50 - 0.80 μm) and Near IR (0.80 - 1.10 μm) .

One of the two instruments of the Ariel Payload is the Fine Guidance System (FGS), including three photometric channels (two used for guiding as well as science) between 0.5-1.1 μm plus a low resolution NIR spectrometer for 1.1-1.95 μm range.

Along with FGS an IR Spectrometer (AIRS) [12] is foreseen, providing low-resolution spectroscopy in two IR channels: *Channel* 0 (CH_0) for the $1.95-3.90$ μm band and *Channel* 1 (CH_1) for the $3.90-7.80$ μm range. Finally, an Active Cooler System (ACS) including a Ne Joule-Thomson cooler is adopted to provide active cooling capability to the AIRS detectors working at cryogenic temperatures.

AIRS is located at the intermediate focal plane of the telescope and common optical system and it hosts two HgCdTe-based hybrid IR detectors and two cold front-end electronics (CFEE) for detectors control and readout. Each CFEE is driven by a Detector Control Unit (DCU) part of AIRS but hosted within and managed by the Instrument Control Unit (ICU) of the Payload [8].

ICU is a warm unit residing into the S/C Service Module (SVM) and it is based on a cold redundant configuration involving the Power Supply Unit (PSU) and the Commanding and Data Processing Unit (CDPU) boards; both DCUs are instead cross-strapped and can be managed by the nominal or the redundant (PSU+CDPU) chain. ICU is in charge of AIRS management, collecting scientific and housekeeping (HK) telemetries from the spectrometer and HK from the telescope (temperatures readings), the P/L Optical Bench (OB) and other Subsystems (SS), thanks to a warm slave unit (TCU, Telescope Control Unit) interfaced to the ICU. Science and HK telemetries are then forwarded to the S/C, for temporary storage, before sending them to Ground.

Here we describe the status of the ICU design at the end of B1 Phase, prior to the Mission Adoption Review (MAR) by ESA, with some still open architectural choices to be addressed and finalised once selected the ICU industrial Prime contractor.

Keywords Exoplanets Atmospheres · Transit Spectroscopy · Infrared Spectrometer · Payload Electronics · Instrument Control Unit · On-Board SW

1 Introduction

The Ariel Mission Consortium (AMC) structure, along with the present architecture of the Ariel Payload, is illustrated by the block diagram of Figure 1. It shows some control electronics units, besides the ICU, hosted by the Service Module of the satellite: the FCU (Fine Guidance System or FGS Control Unit) [13], the TCU (Telescope

Control Unit) [14] and the CCE (Cryocooler Control Electronics) [16] for the active cryocooler (ACS) management.

The Instrument Control Unit of the Ariel Payload is the electronic unit in charge of managing the TCU, the whole AIRS Spectrometer and processing the collected scientific data from it, before sending them to the on-board data handling system of the Spacecraft (S/C).

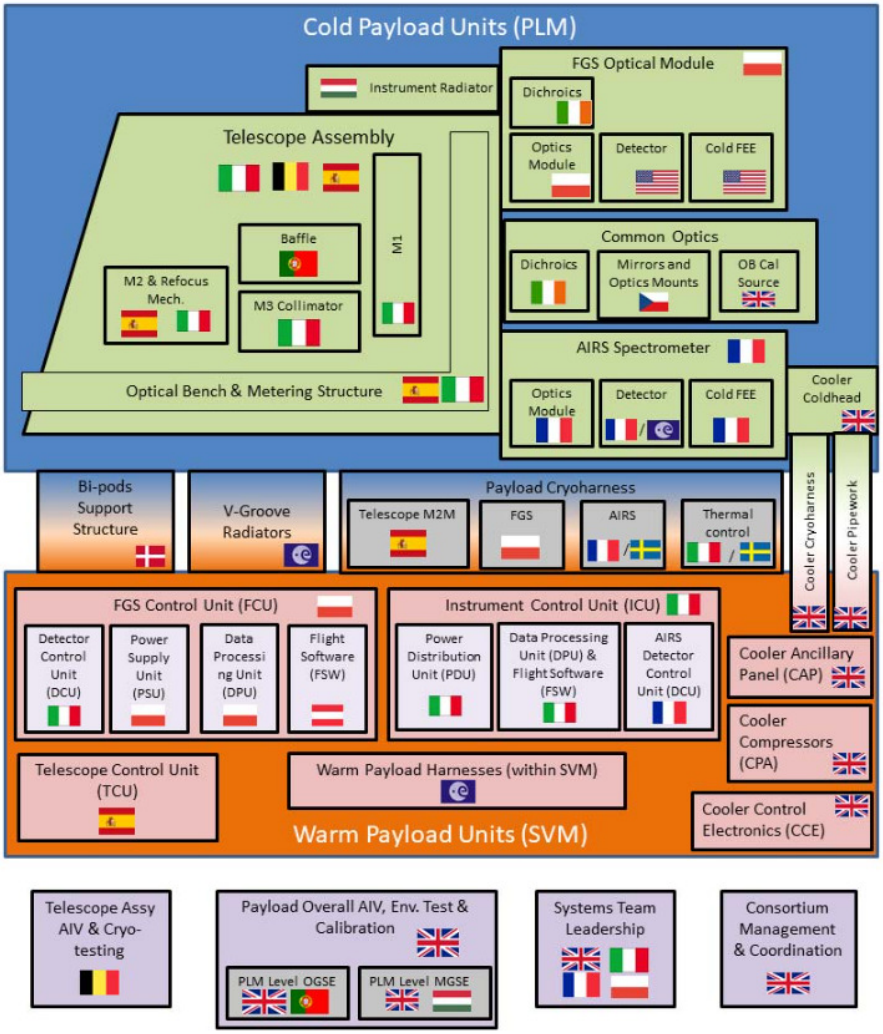

Fig. 1 Ariel Payload block diagram and Ariel Mission Consortium (AMC) Countries responsibilities - courtesy Ariel Mission Consortium (AMC)

The ICU P/L subsystem is conceived as an assembly composed of a mechanical enclosure provided with a back panel hosting the internal connectors, to plug and interface the electronics boards, and several external-mounted connectors for electrically interfacing the external world (Payload and Spacecraft). Its architecture relies on a cold redundant and partially cross-strapped configuration hosting five subsystems with the following operational configuration:

- 1 PSU – Power Supply Unit (N and R);
- 1 CDPU – Commanding and Data Processing Unit (N and R);
- 2 DCU – Detector Control Unit (only N) for the AIRS CH_0 and CH_1 channels;
- 1 BP - backplane;

and it is linked, by a serial cross-strapped interface (I/F) to the external Telescope Control Unit box (N and R chains, in a cold redundant configuration), in charge of managing the Thermal Control stabilisation System (TCS for operational heaters and thermistors) of the M1 and M2 mirrors, the M2 mechanism (M2M) and the on-board calibration source (OBCS).

The ICU design (enclosure included), the Power Supply Unit, the back panel and the Commanding and Data Processing Unit (including HW drivers, boot SW and Application SW), along with the ICU AIV/AIT activities, are in charge and under the responsibility of Italy (INAF, for the Italian Space Agency - ASI and its Prime/Industrial Contractor, to be selected in the next Phase), while the DCUs and TCU requirements specification, design and manufacturing are respectively in charge of France (CEA - Saclay) and Spain (IEEC - Barcelona). These P/L subsystems will be provided to ASI/INAF as external furnished equipments and delivered from CEA and IEEC to ASI/INAF and tested, along with the ICU, at INAF premises in Italy, before delivering to RAL Space (UK) for AIT/AIV activities at Payload level.

The AIRS Detector Control Units are implemented in a not redundant configuration and represent the spectrometer warm Front End Electronics located in the SVM, within the ICU box as baseline. They are interfaced to the AIRS CFEE and the T-e2v H1RG detectors for $CH0$ and $CH1$ channels (refer to Figure 2) by means of cryoharness in order to control the data generation and acquisition process and constrain the heat load on the FPAs.

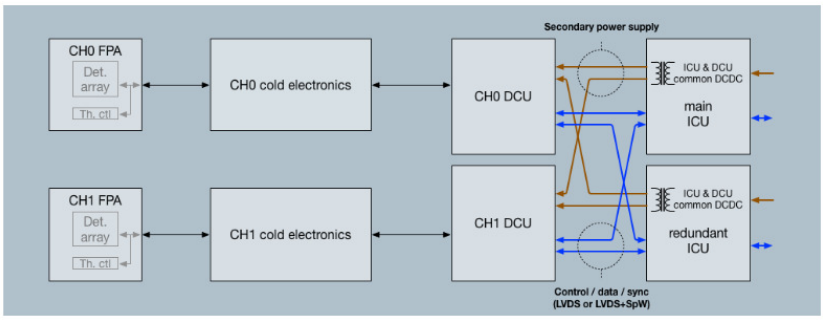

Fig. 2 Overview of AIRS electrical system - courtesy CEA, France

The main functions of the DCU are:

- providing housekeeping for AIRS-OB (optical bench) and AIRS-FPA (detectors and CFEEs) - refer to Figure 3 ;
- to control the data acquisition at detector level through the CFEE from users entry;
- pre-processing digital data from the detector (on-board its FPGA);
- to control the thermal stabilisation of the detectors through temperature probes and heaters;
- interfacing the ICU CDPU for telecommands (TC) reception, housekeeping (HK) and Science data transmission.

For a simple and efficient P/L operation and control, the TCU management will be in charge of the ICU processor, the only chip running a high-level SW (Application SW) controlling both DCUs and TCU as well, as the latter will implement only a slave FPGA[1].

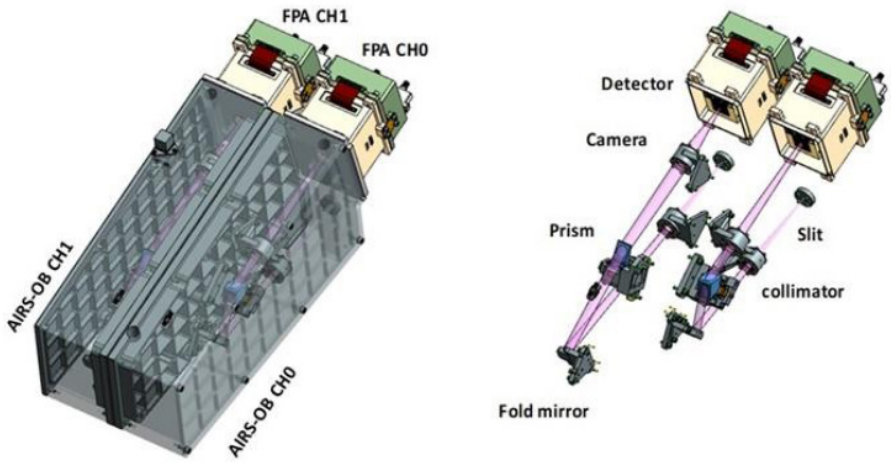

Fig. 3 AIRS Spectrometer showing two joint boxes hosting the optical benches and detectors for $CH0$ and $CH1$ channels - courtesy CEA, France

2 AIRS detectors and CFEE selection

The following picture (Figure 4) shows a synoptic overview of the AIRS end-to-end data acquisition and processing chain up to the electrical I/F to the ICU (DCU to CDPU I/F).

[1] Field Programmable Gate Array

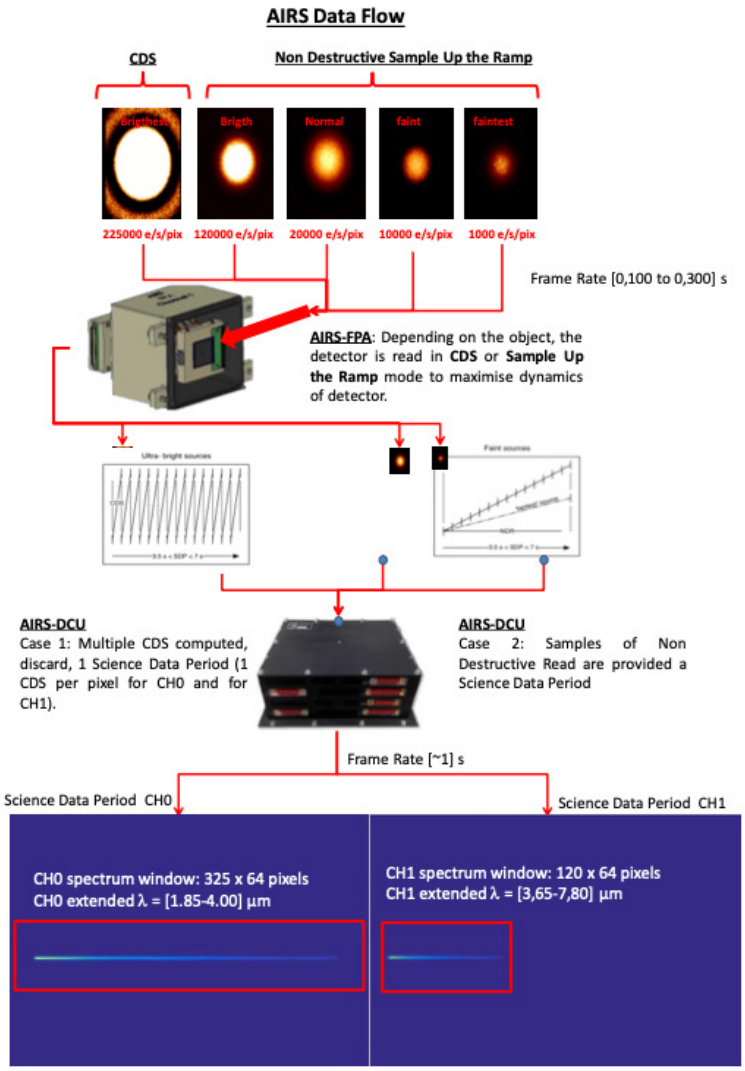

Fig. 4 AIRS detectors readout and digital processing electronics up to the DCU to CDPU I/F - courtesy CEA, France

In the AIRS former baseline design both the detectors and cold front end electronics are from Teledyne (H1RG + SIDECAR) but it is still open the possibility to adopt, as new baseline, a CFEE customised analog electronics based on discrete components and working at a lower temperature (T $\leq$ 55-60K, w.r.t. 120-130K of the baseline solution) with a DCU hosting on-board the analog to digital (ADC) conversion section (provided by SIDECARs in the former baseline design, as ASIC embedded capabil-

ity). This choice would greatly help the thermal arrangement and integration of the CFEE within the cold Instrument cavity, working at 55-60K.

The ICU design is partially driven by the data acquisition chain and detectors selected to be used at the AIRS focal plane. The baseline architecture relies on the use of H1RG-type detectors and its customised driving and readout ASIC. This choice is due to the very high TRL (Technology Readiness Level) and space heritage of these FPA systems with respect to the present European alternatives. The SIDECAR solution is the best one to drive properly the US MCT (HgCdTe) detectors and to save mass, volume and power at the same time.

The SIDECAR (System for Image Digitisation, Enhancement, Control And Retrieval) ASIC [17] is a Sensor Chip Array (SCA) providing clocks and biases and performing amplification and analog-to-digital conversion of the SCA analog outputs. It can run with up to 36 ADC with a maximum sampling frequency of 500 KHz. Given the selected small windows for spectra on the detectors, lower readout frequencies (100 Kpx/s) are selected for the AIRS sensors in order to limit noise, power consumption and thermal dissipation affecting the Spectrometer performance.

The two AIRS detectors will be interfaced to the relevant SIDECAR ASICs by means of a space-qualified flexy-ribbon cryoharness, as already adopted for the Euclid/NISP and JWST/MIRI on-board instrumentation.

Alternatively, preferred from a thermal point of view and design simplification, still guaranteeing functional and signal to noise ratio performance, a CFEE based on discrete components and a differential preamplifier (exploiting two OPA2350) can be adopted.

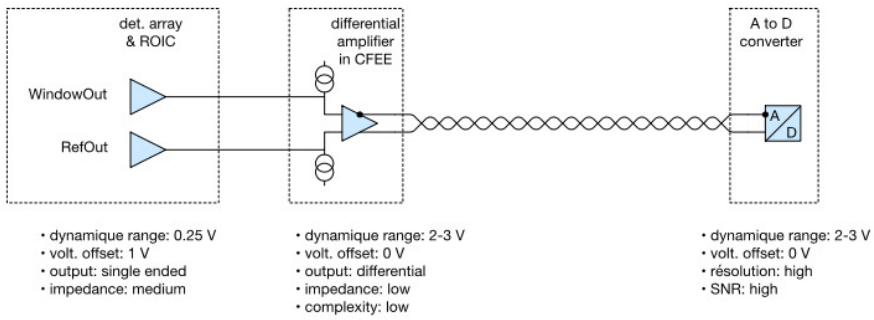

Fig. 5 AIRS analogue signal chain, discrete electronics option - courtesy CEA, France

With this configuration, the differential amplifier is in charge of:

- amplifying the amplitude limited (typically 200 mV) output signal of the ROIC to
- enabling transmission of the amplified signal over several meter-long harness to the warm electronics while limiting the ROIC out buffer current setting and thus the risk of glow

- transmitting the video signal in differential mode to reduce noise pick-up effect along the harness to the warm electronics.

The preamplifier, as shown in Figure 5, is a differential input to a differential output amplifier. Inputs are respectively connected to one of the ROIC active pixel outputs and to the ROIC reference pixel output. Any drift or low frequency noise common to both output signals is rejected to the differential operation of the preamplifier. Analogue to digital conversion is, then, demanded to DCU.

3 ICU allocated budgets and design drivers

The allocated budgets for the Unit, to be considered for the design assessment, are summarised in Table 1. The volume allocation for the ICU enclosure includes the mounting feet, connectors and ground lugs, while external harnessing along with its bending radius is excluded.

The ICU science data volume is intended as the nominal weekly allocation from AIRS DCUs ($CH0$ and $CH1$) and sent to the ICU CDPU (equivalent to 317.1 Gbit per week before compression, without margin), excluding internal housekeeping from TCU and DCUs (not compressed data). Assuming an achievable averaged compression ratio ($< CR >$) of 2.5, the expected ICU-to-S/C nominal weekly science + internal HK data volume is 129.1 Gbit (155.0 Gbit including 20% of margin).

	Power (W)	Mass (Kg)	Dimensions (mm) L x W x H	AIRS weekly data volume before compression (Gbit)	AIRS weekly data volume after compression (Gbit)	HK weekly volume (Gbit)
Allocated	29.1	6.7	N/A	317.1	126.8	2.3
Margin (20%)	5.8	1.3	N/A	63.3	25.4	0.5
Total with margin	**34.9**	**8.0**	**320 x 185.1 x 220**	**380.4**	**152.2**	**2.8**

Table 1 ICU allocated budgets, DCUs included

3.1 CDPU input data rate

The ICU hardware and software design is strongly affected by the AIRS input data rate to be managed by the CDPU board and on the actual needs in terms of buffering and real time data processing. Therefore, to correctly size the CDPU on-board memories and the needed processing capabilities, a basic analysis of the expected input data rate has been performed as an assessment of the overall weekly data volume in terms of HK and science telemetries.

3.1.1 Housekeeping data rate

Concerning the housekeeping to be collected by the ICU assembly, the overall budget is dominated by those collected by the TCU subsystem. Anyway, the HK daily volume is negligible with respect to that concerning scientific data (refer to Table 1).

3.1.2 Science data rate and data volume assessment criteria

The selection of the detectors for the Ariel Spectrometer is based on the Teledyne MCT 1k x 1k array already developed for the NASA's NEOCam mission and based on the heritage of the WISE mission; this kind of detectors allow for non-destructive (or multi-accumulate sampling up-the-ramp) readout modes. This capability can effectively reduce the equivalent readout noise, improving the signal to noise ratio and allowing an easier identification and rejection of glitches induced by cosmic rays hits affecting the signal.

Data coming from AIRS $CH0$ and $CH1$ CFEEs are firstly managed by the two AIRS DCUs and then transferred across the Spacewire (SpW) RMAP[2] links to CDPU. Data from detectors/CFEEs are represented by cropped windows of 300 x 64 pixels for $CH0$ and 100 x 64 pixels for $CH1$ with a pixel depth of 16 bit (2 bytes). If we assume to sample up-the-ramp pixels in a non-destructive manner with the length of the ramp determined by the saturation limits of the detector, an estimation of the expected data rate can be provided, in principle, for any target of known flux (bright, medium, faint). The performed estimation is including the need of having a detector reset between each ramp or a correlated double sampling (CDS).

The Ariel P/L overall weekly data budget has been calculated and reported in Table 2, where a breakdown of the expected data rate including the housekeeping collected by ICU (TCU included) is provided.

The Payload data volume is dominated by the FGS NIRSpec, AIRS-$CH0$ and AIRS-$CH1$ channels and takes into account the observing efficiency (95% - targets + calibration), as well as the system margin. The calculation provided in Table 2, on which has been defined the assigned budget of Table 1, assumes on-board fitting up the ramp or CDS (Correlated Double Sampling), with an average ramp length to saturation up-to few seconds for the AIRS channels and a following DCU data decimation. In particular, it is assumed that we sample up-the-ramp pixels in a non-destructive manner with a relative high frame rate ($\sim$5.8 Hz for AIRS-$CH0$, $\sim$15.8 Hz for AIRS-$CH1$), followed by destructive readouts after a defined number of samples, depending on the brightness of the target.

Indeed, the actual read-out mode to be used will vary between targets (as a function of their brightness) with the possibility of setting the ramp integration time in the range of few seconds. For each Ariel target, the expected flux will be used for refining the best readout scheme and obtaining the corresponding data rate. The adopted scheduling tool for Ariel observations, calibrations and data delivery to Ground, will also be used to show how the payload data rate may vary throughout the mission

[2] Remote Memory Access Protocol

ARIEL subsystem	Description	Requirement as output data rate to SVM (Gbit/week)
FGS	Science data + AOCS data stream + internal HK	64.2
ICU Science	Science data + internal HK	126.8
ICU/TCU PLM HK	Thermal monitoring + M2M TM + Cal Unit + others	2.3
CCE HK	Cooler HK & TM	0.8
TOTAL		**194.1**
Margin	System Margin (20%)	41.9
TOTAL with margin	Total ARIEL PLM allocation	**236**
AIRS -> CDPU	Allocation pre-compression from AIRS DCUs to ICU CDPU	**317.1**

Table 2 Overall Ariel Payload data rate budget. In red is highlighted the expected data flow from AIRS, prior ICU on-board compression

and to evaluate the expected maximum and average data rates, thus allowing for a finalised dimensioning of the on-board processing needs (along with the ICU buffering capabilities), prior to send data to the S/C Mass Memory Unit (MMU). As most of the expected data processing (e.g. compression) will be performed in quasi real time, no particular criticalities for data buffering are presently foreseen.

3.2 Other electrical design drivers

For the unit design definition and requirements specification it is also assumed that the Ariel S/C and P/L will adopt a grounding and isolation concept based on a single power supply distribution scheme for primary power lines from the SVM and an isolated DC/DC conversion at Payload level. Primary power shall be distributed via twisted pair set of wires and the spacecraft structure shall not be used as a current return path neither for power distribution nor for signal return paths. In particular, for the overall Payload and ICU power supply distribution and grounding principle, it is foreseen the adoption of the Distributed Single-Point Grounding (DSPG) scheme.

4 ICU electrical design

The ICU architecture is shown in Figure 6 as a block-diagram representation, valid at board-level for both a baseline and an alternative design. These differ among each other only for the DCUs and AIRS Thermal Control stabilisation System (TCS) design and implementation, following two possible scenarios:

- Adoption of a DCU design from CEA (baseline design), implementing an embedded TCS for AIRS;

- Adoption of a DCU design from INAF (alternative design), exploiting the NISP DCU design from OHB-Italy for the Euclid Mission, but implementing the AIRS TCS on the ICU Power Supply Unit (PSU).

While the ICU to SVM electrical I/F are the same for both architectures, the Unit internal electrical I/F and towards AIRS CFEEs will change only a little as a function of the final chosen implementation.

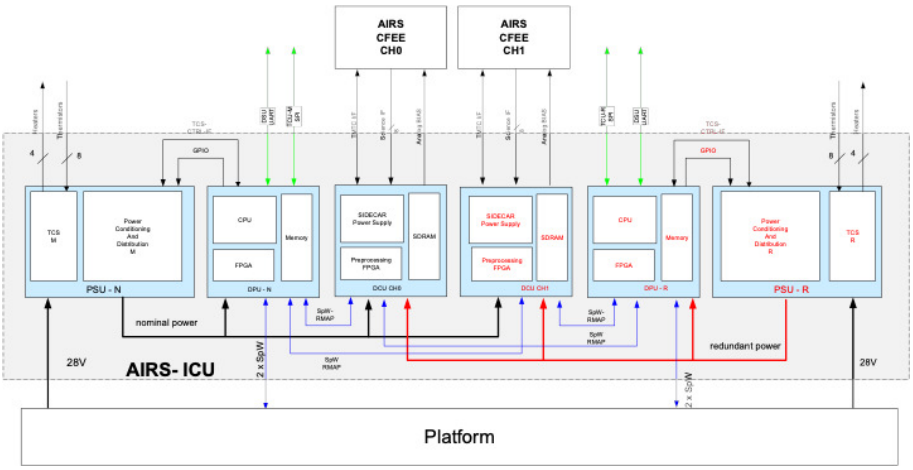

Fig. 6 Ariel ICU block diagram showing the electrical I/F towards the SVM (Platform) and Payload

It is worth noting again that the baseline design foresees the AIRS Thermal Control Stabilisation system implemented on board the AIRS DCUs, while in Figure 6 is reported within the PSU board. As the AIRS DCUs baseline design is integral part of the AIRS Spectrometer documentation here is shortly described only the viable alternative architecture exploiting the DCU design developed for the Euclid/NISP Instrument. As the NISP DCUs do not actually embed a TCS, in order to avoid any heavy modification to the original DCU design and its re-engineering it has been assumed a TCS implementation on the PSU board in the alternative design, as it offers the needed available space for EEE components placement and routing, still respecting the present allocated volume by ESA.

Independently of the DCU adopted design, the present ICU architecture is based on a partial cold-redundant and cross-strapped configuration, as shown in Figure 6. In particular, both DCUs are cross strapped and can work along with the N & R PSU+CDPU assemblies, although DCUs does not implement a redundant configuration.

As above anticipated, a very similar ICU architecture, exploiting DCUs as SIDECAR I/F (for biases, clocks and control signals), has been already designed and developed for the Euclid Mission (NISP Instrument) [18]. Each DCU controls and interfaces a single SIDECAR (as well as the related detector) and, in this sense, can be considered for the Ariel Payload a strong heritage and a viable backup solution.

Indeed, for the NISP design, an overall (DPU + DCU + SIDECAR + H2RG detector) chain/system reliability figure higher than 98% has been assessed and for this reason no redundancy for Ariel DCUs, as for the NISP case, has been considered by AMC. This is also due to the related increasing complexity and needed budgets (power, mass, volume) to implement a redundant section.

The DCU Technology Readiness Level (TRL) of the described alternative design has been demonstrated to be higher than 8, as 16 DCUs FM (Flight Models) have been already manufactured and fully tested. In addition, the NISP DCU EQM model has been previously manufactured and tested/qualified. Finally, a DCU/SIDECAR I/F simulator has been developed and used by the NISP Team. The same philosophy concerning the simulator (e.g. for re-use) may be adopted if needed (mainly for programmatic reasons) for the Ariel case, for both AIRS and FGS DCUs. Indeed, it is the baseline choice for the FGS instrument.

In the following Table 3 are reported the ICU Nominal and Redundant electrical I/F towards the SVM (in orange), towards AIRS (in green, for the alternative design) and to the TCU (in red). Also the Debug Support Unit I/F for CDPU is shown (in white). No cross-strapping is presently foreseen between the SVM warm units in charge of S/C Prime (OBC and MMU) and ICU. As anticipated, the electrical I/F to the SVM and TCU are valid for both the baseline and the alternative ICU designs.

4.1 PSU board design

The Power Supply Unit board adopts, for both the baseline and alternative designs, a typical scheme hosting DC/DC converters with a number of secondary sections needed to support the chosen cross-strapped and partially cold-redundant configuration.

In addition to the primary to secondary voltages conversion function, PSU is in charge of collecting currents, voltages on secondary outputs and temperatures HK (A/D converted internally to the Unit, exploiting the SPI HK I/F for signals and control lines to/from the ADCs). The Unit consumption monitoring is in charge of the platform, as well as its on/off switching (it happens for both PSU and CDPU boards at the same time, thanks to a sequencing logic owning to PSU), occurring once received the primary voltage from the SVM bus (from a p-type LCL[3]), without the need of discrete switching signals to the Unit.

The PSU design is mainly based on three sections (refer to Figure 7) with an additional one hosting the AIRS TCS for the alternative design:

1. Power conditioning section, performing the following tasks:
   - DC/DC conversion: main DC/DC for the generation of the secondary voltage levels to be distributed to the ICU boards, Aux DC/DC for internal logic powering, HK DC/DC for powering the HK section for the acquisition of voltages/currents/temperatures HK;
   - Inrush current limitation;
   - Polarity inversion protection;

[3] Latching Current Limiter

Electrical I/F	Type	Remarks
Primary power input N	28V not regulated	S/C PCDU link
Primary power input R	28V not regulated	S/C PCDU link
TMTC SpW N	SpW main link for TM/TC with the S/C	S/C OBC link
TM SpW N	SpW main link for science data	S/C SSMM link
TMTC SpW R	SpW redu link for TM/TC with the S/C	S/C OBC link
TM SpW R	SpW redu link for science data	S/C SSMM link
TCU N SPI	SPI link with TCU-M	P/L internal link
TCU R SPI	SPI link with TCU-R	P/L internal link
DSU UART N	RS422	Debug I/F
DSU UART R	RS422	Debug I/F
SIDECAR I/F Ch0	TMTC serial I/F – LVDS 8 bit parallel science I/F -LVDS Various analog bias	P/L internal link (partial cryo-harness from PIP to CFEE)
SIDECAR I/F Ch1	TMTC serial I/F – LVDS 8 bit parallel science I/F -LVDS Various analog bias	P/L internal link (partial cryo-harness from PIP to CFEE)
TCS I/F N	4 heaters 8 thermistors	P/L internal link (partial cryo-harness from PIP to CFEE)
TCS I/F R	4 heaters 8 thermistors	P/L internal link (partial cryo-harness from PIP to CFEE)

Table 3 ICU alternative design electrical I/F

- Under voltage protection and over current protection (TBC);
- Power-on sequence generation (sequencer logic);
- Unit power-on reset generation;
- EMI (Electro-Magnetic Interference) filtering.

Note : only a Main DC/DC converter is planned to feed CDPU and both DCUs, as presently it is assumed that it will comply with the overall required current and needed power. As alternative, a further DC/DC converter could be exploited to feed parts or subsections of the itemised boards, provided that both DC/DC can satisfy the required current sink and be accommodated on the same board.

2. Power distribution section with three built-in Output Power Controllers (OPC), implementing overcurrent and over-voltage protection functionalities on the secondary voltage/current distribution lines to CDPU and DCUs;
3. HK acquisition section with a multiplexed (8 channels) 12 bits ADCs for voltages, currents and temperatures measurements, collected by the processor via SPI (Serial Peripheral IF).
4. Thermal stabilisation Control System (TCS) section, able to drive and readout heaters and thermistors located in each subsystem of the AIRS Spectrometer.

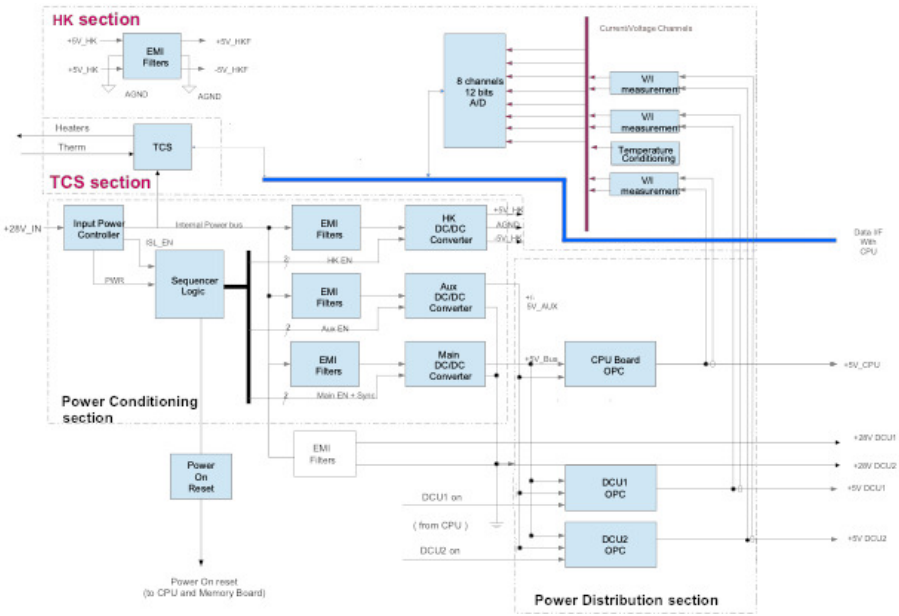

Fig. 7 Power Supply Unit block diagram

According to Table 4, each TCS module shall have the following interfaces (T = thermistor, H = heater):

- 2T supporting cross-strap for CFEEs
- 2T supporting cross-strap for Detector Modules
- 2T (N&R) for single Detector Module not cross-strapped
- 2T (N&R) for single OM not cross-strapped
- 2H supporting cross-strap for CFEEs
- 2H (N&R) for Detector Module not cross-strapped

and shall implement at least a signal conditioning chain dedicated to drive and readout of FPA/CFEE temperature sensors based on 4-wires measurement configuration. The block diagram of Figure 8 shows the proposed conceptual configuration.

In order to resolve 5mK in the range 110K-150K it is necessary to use at least a 20 bit converter. A viable solution is to adopt the ADS1282-SP from TI, delta-sigma A/D converter, able to perform at 24 or 32 bit.

To reach the required accuracy on the analog front end within the thermal environment of the Ariel P/L [5], [11], continuous calibration on high precision resistor is envisaged to monitor both offset and gain of the acquisition chain. Heaters power can be provided with a linear current generator implemented with suitable OPAMPs controlled by a DAC from the control logic. The AIRS TCS electronics can be finally placed on the PSU PCB (alternative design) and controlled from the CDPU board trough a suitable set of control signals, routed from an FPGA. The thermal control

Location	Type	Features
CFEE Ch0	1T cross-strapped	measurement range: [105 ÷333]K temperature accuracy : ± 0.005K over [110 ÷150]K
	1H cross-strapped	50mW max power
CFEE Ch1	1T cross-strapped	measurement range: [105 ÷333]K temperature accuracy : ± 0.005K over [110 ÷150]K
	1H cross-strapped	50mW max power
FPA Ch0	1T Main + 1T Red	measurement range: [20 ÷333]K temperature accuracy : ± 0.001K over [25 ÷50]K
	1T cross-strapped	measurement range: [30 ÷333]K temperature accuracy : ± 0.01K
	1H Main + 1H Red	5mW max power
FPA Ch1	1T Main + 1T Red	measurement range: [20 ÷333]K temperature accuracy : ± 0.001K over [25 ÷50]K
	1T cross-strapped	measurement range: [30 ÷333]K temperature accuracy : ± 0.01K
	1H Main + 1H Red	5mW max power
Optical Module(s)	2T Main + 2T Red	measurement range: [20 ÷333]K temperature accuracy : ± 0.001K over [25 ÷50]K

Table 4 AIRS heaters and thermistors and required features

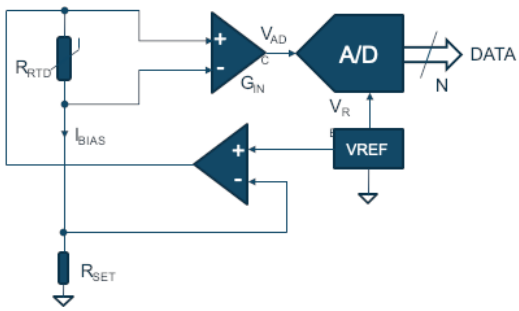

Fig. 8 AIRS TCS proposed signal conditioning chain

loop logic can then be implemented in the processor board to readout the temperature data and drive the heaters accessing the FPGA registers.

Each ICU electronic board is fed thanks to secondary power lines protected for over-voltage and overcurrent and locally are derived, by means of a Point of Loads (PoL), additional voltage levels needed by the hosted electronic components (e.g. memories, FPGA core etc.).

For the implementation of the baseline or alternative DCU design are foreseen the voltage levels reported in Table 5 (the CDPU/DCU electrical I/F for TM/TC

lines are the same for both the baseline and alternative designs and represented by cross-strapped SpW links with the adoption of the RMAP protocol).

Voltage level	Baseline DCU design	Alternative DCU design
+28V ANA	-	X
+5V DIG	X	X
+6V ANA	X	-
-6V ANA	X (TBC)	-

Table 5 Voltage levels needed to drive the DCU in the baseline and alternative designs

4.2 CDPU board design

The Commanding and Data Processing Unit is designed as a single board hosting a microprocessor (the GR712RC dual-core LEON3FT CPU from Cobham Gaisler, as baseline) and a co-processing FPGA, extending the CPU interfacing capabilities and peripherals. This choice is coherent with the FGS/FCU CPU selection, hosting the same processor and exploiting so commonalities within the Project, and with the AIRS Spectrometer design as well, relying on two parallel DCU channels that may be singularly managed by the two CPU cores. It also avoid the adoption of more complex internal buses architectures (e.g. cPCI) no more supported by some of the space qualified Operating Systems (e.g. RTEMS[4] last versions) and, along with the adopted FPGA in the reference architectural design, it guarantees the needed resources for the instrument management and data processing (e.g. SW and/or HW compression on AIRS data).

The GR712RC ASIC is a system on a chip (SoC) form Cobham/Gaisler with advanced interface protocols implementation, dedicated to high reliability, rad-hard space, aeronautics and military applications. This SoC includes two LEON3-FT microprocessors (SPARC V8 architecture) and its internal block diagram is represented in Figure 9.

The CPU architecture is built around the AMBA[5] Advanced High-speed Bus (AHB), to which the two LEON3-FT processors and other high-bandwidth units are connected. Low-bandwidth units are connected to the AMBA Advanced Peripheral Bus (APB) which is accessed through an AHB to APB bridge. The GR712RC can be delivered in three quality levels: flight, engineering and prototype (PROTO). It is provided in a 240-pin, 0.5 mm pitch high-reliability ceramic quad flat package (CQFP-240) and it is not subject to U.S. ITAR regulation.

The GR712RC dual-core CPU results one of the eligible on-board CPU for implementing both instrument control, data acquisition tasks and processing functionalities (e.g. for SW data compression) exploiting properly its dual-core nature w.r.t.

[4] Real-Time Executive for Multiprocessor Systems
[5] Advanced Microcontroller Bus Architecture

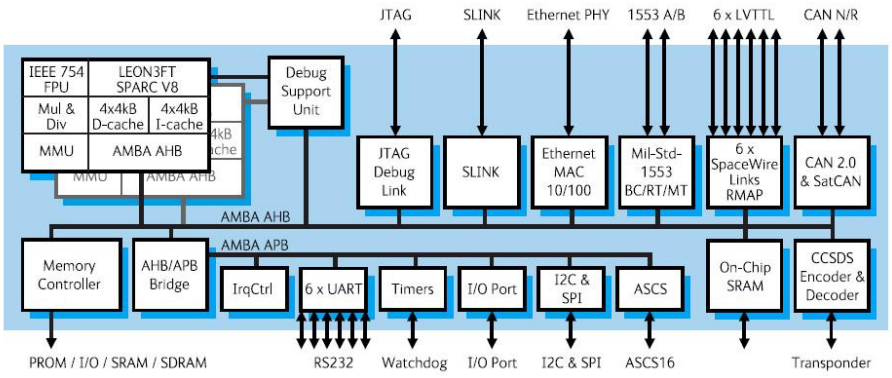

Fig. 9 GR712RC block diagram - courtesy Cobham/Gaisler

the AIRS symmetrical channels configuration. It guarantees up to 200 MIPS of peak performance when running at 100 MHz.

The GR712RC processor can be used in the so-called AMP (Asymmetric Multi-Processing mode) configuration (instead of SMP or Symmetric Multi-Processing mode) to allow different SW tasks to run asynchronously on the individual cores, configured to have separate memory addressable areas and hardware resources. This choice aims at obtaining a deterministic behaviour of the SW, because any hypothetical anomaly or overload of the running tasks in the additional core does not affect the effective working capability of the other one, granting a physical insulation of the running spaces.

In case of AMP operating mode, the multi-core design requires extra-work to manage the possibility of concurrent access to all the shared resources (interrupts, timers, peripherals, memory). In order to use a multi-core processor the software should be split up and distinguished into items that can run in parallel on the different cores. In this configuration, two instances of the RTEMS OS in AMP mode are executed. The RTEMS running on the first GR712RC core, the boot process managing processor, has the control over the primary resources and initialises the overall environment, while the RTEMS running on the second core has not access to the main resources but keep a full and independent control over its own threads scheduling, being the management of the other resources left to the developers choices.

It is worth noting that the GR712RC can exploit up to 6 embedded SpW I/F (4 with CCSDS/ECSS Telecommand decoders and Telemetries encoders and 2 RMAP I/F) if no SDRAM-type memory is directly interfaced, otherwise only 4 links are available. Moreover, the GR712RC device cannot run at 100 MHz if a SDRAM memory is used (due to the memory characteristics).

Therefore, two different architectural solutions are here described for the Ariel CDPU: a simpler one (Solution A), unlikely to be finally implemented, and a more complex one (Solution B) as the baseline. Let's start describing the simpler, first one.

Solution A: (refer to Figure 10) is the simpler solution, as accounts only for the GR712RC processor interfaced directly to SDRAM (e.g. 256 MB), without any FPGA extending the CPU I/F capabilities. Data incoming from the two DCUs are buffered by the SDRAM and two instances of the compression SW can run in parallel on the two processor's cores, taking care and managing data from the two AIRS channels. In this case 2 (RMAP) out of 4 available SpW links are adopted to interface DCU-0 and DCU-1, while TCU is interfaced by means of cross-strapped serial connections. 2 SpW CCSDS/PUS links are adopted for TM and TM/TC towards the SVM OBDH[6] system (SVM to ICU cross-strapping is presently not foreseen, as the actual OBC and MMU data routing configuration is under Prime and still unknown into detail).

Indeed, a simpler solution without using any SDRAM bank/chip may be selected if the incoming data rate could be managed (including compression) in near real-time by the processor and a SRAM memory.

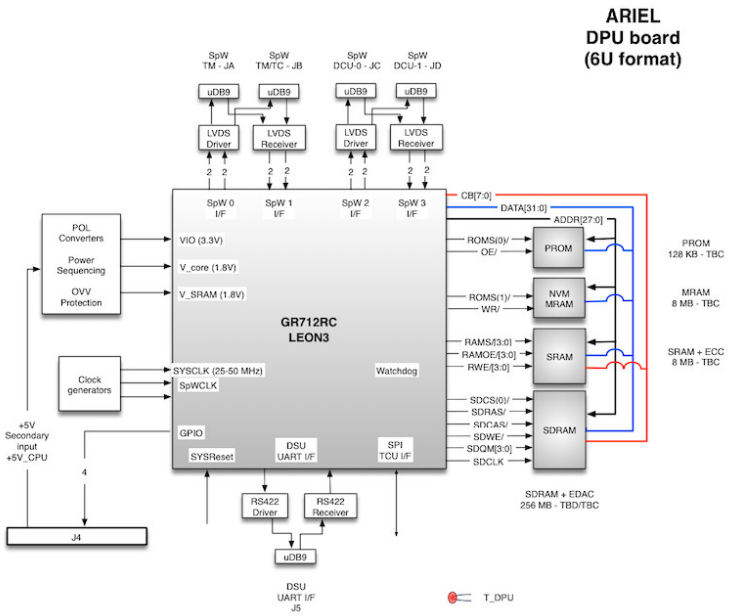

Fig. 10 CDPU board design, Solution A

Solution B: (refer to Figure 11) is a slightly more complex solution as it implements, along with the GR712RC processor running at the available max frequency, an FPGA (e.g. RTAX family 1K or 2K - TBD) to which is interfaced the SDRAM memory by means of a SDRAM controller implemented as a VHDL IP core inside the FPGA FW.

[6] On-Board Data Handling

With this solution the compression task can be achieved by means of SW, thanks to the CPU, or -alternatively- by HW, thanks to the FPGA. 2 (RMAP) out of 6 available SpW links are adopted to interface the FPGA, while both DCUs are interfaced by means of a SpW RMAP connection (baseline choice to harmonise the internal serial connections and protocols). Two SpW CCSDS/PUS links, as in Solution A are adopted for TM and TM/TC towards the SVM OBDH system.

Actually, an hybrid solution connecting both the GR712RC and the FPGA SDRAM and memories buses (shared bus) may be proposed, provided that the RMAP commands to the DCUs FPGA are anyway guaranteed exploiting the RMAP reading and writing capabilities on the memories buses (functionality under assessment).

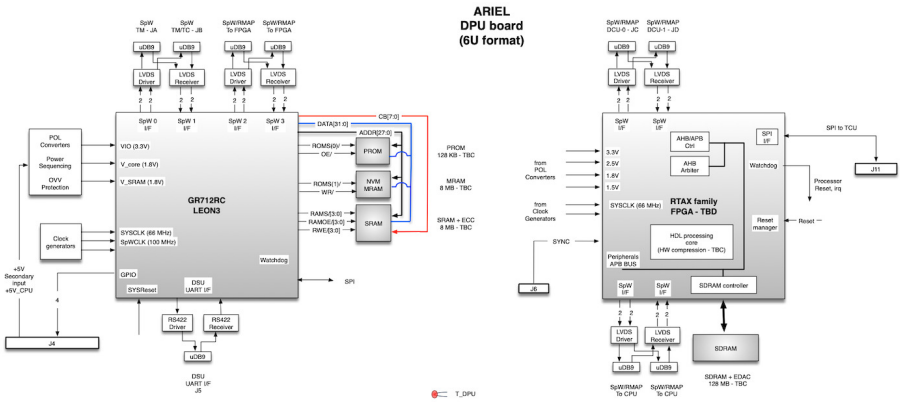

Fig. 11 CDPU board design, Solution B

Depending on the architecture either the two Leon3FT processor cores will run at high frequency (e.g. 80-100 MHz), without SDRAM or at a lower frequency (e.g. 25-50 MHz TBD) with SDRAM.

Memories for:

- booting (PROM), 128 KB
- storing the ASW (E2PROM or NVM e.g. MRAM), 8 MB
- data buffering and processing (e.g. SDRAM), 128 MB
- Boot SW, ASW deployment and data processing (e.g. SRAM, SDRAM), 8 MB

are foreseen (65% margin included) in both designs, in a TBD final configuration, waiting for a better assessment of the compression task performance and implementation requirements. 8 bits BCH (Bose–Chaudhuri–Hocquenghem) EDAC for SRAM and PROM is adopted, while Reed-Solomon 16 bits EDAC is adopted for the SDRAM memories as baseline (32 bits of data bus + 16 bits for EDAC) in order to guarantee a better immunity to SEE effects (mainly SEFI) related to the radiation environment.

The GR712RC IC requires two power supply voltage levels; +1.8V DC voltage for the IC Core and a +3.3V DC voltage for the IC I/O signals. Power conversion

from the +5V supplied by the PSU is done on-board each CDPU (N & R) by means of PoL to guarantee clean and stable voltage values for the EEE components and minimise voltage drops at the same time.

4.2.1 CDPU data handling and processing

The CDPU science data handling functionalities mainly concern the AIRS spectrometer digital data (16 bits/pixel) acquisition, buffering and processing. A task of lossless compression (e.g. adopting the RICE/small RICE algorithm, providing an average compression ratio $< CR >$ of at least 2-2.5) is planned along with a baseline processing task (CCSDS/PUS[7] science data and HK packetisation, TC and digital I/F management). The compressed data are packetised according to the PUS protocol format over Spacewire and sent to the S/C DHS for storing and later downloading to Ground. Pre-processing and compression tasks can be disabled in case of raw data request from the Spacecraft/Ground (mandatory requirement).

As anticipated in the previous paragraph, the GR712RC processor can exploit, in principle, the Asymmetric Multi-Processing mode configuration to allow different or very similar SW tasks to run asynchronously on the individual cores, configured to have separate memory addressable areas and hardware resources to independently manage both channels. Also a mixed approach may be, in principle, pursued, where the compression task is devolved to one core only or, better, managed by the HW (FPGA) interacting with one or both cores. These SW architectural choices will be assessed and defined during the next design phase (B2), prior Payload and Units PDR.

The data handling functionalities will be implemented, as baseline, in the ICU application software (ASW running on the CDPU processor), to be considered as the AIRS Instrument managing Software. It handles all the ICU/Spectrometer and ICU/TCU digital interfaces and implements the following instrument monitoring and control functionalities: verifying and executing the telecommands received from the S/C, handling the switching on/off of the DCU and TCU operational modes transitions, configuring and commanding the spectrometer sub-units, monitoring the ICU and AIRS units, reporting housekeepings and events, supporting the payload hierarchical FDIR[8] operated by the S/C and the P/L functional modes, managing the on-board time through a combination of the absolute time (received from the S/C through the SpW PUS protocol and Time Codes) and the internal time (based on a HW clock).

All the listed functionalities will be implemented by means of the CCSDS/PUS services. All the mandatory PUS services (refer to Table 7) will be guaranteed along with a set of services specific to the Ariel Mission (private services under assessment).

From the point of view of the CDPU processor, we assume to perform on-board the following basic tasks: AIRS spectrometer (Instrument) managing and commanding, data processing (compression only) buffering and packetisation, before sending science data to the S/C MMU.

[7] Consultative Committee for Space Data Systems / Packet Utilisation Standard
[8] Fault Detection, Isolation and Recovery

Assuming, as baseline, a SW (or mixed SW/HW – TBD) $< CR >$ of 2.5 and an ICU allowed science + HK data rate towards the S/C of 126.8 Gbit/week, the expected weekly data volume from AIRS DCUs is 317.1 Gbit/week (45.3 Gbit/day), as uncompressed data volume. This lead to an average input data rate to the ICU/CDPU board of 65.5 Kbytes per second without margin. Considering a margin of 20%, the average input data rate assumed for CDPU SS sizing is 78.6 or 80 Kbytes/s.

To size the CPU clock frequency, it is necessary to evaluate which is the expected number of elementary operations needed to execute the most demanding onboard SW activity, i.e. SW compression.

Waiting for a more detailed assessment of the SW compression core performance on a realistic set of data (AIRS spectral samples), it is possible to make some assumptions based on previous experiences[9] with standard implementations of lossless (and lossy) compression algorithms. In particular, adopting a conservative approach, 120 basic operations per sample (pixel) or 60 operations/byte (pixel depth @ 16 bits) can be considered. This figure is related to the compression algorithm, and can be decreased on the basis of the algorithm that will be finally chosen.

Assuming that each basic operation can be performed with an average of three CPU clock cycles, it is possible to estimate a total of 180 clocks/byte for the SW compression task. Within these assumptions, a CPU running at 25 MHz dedicated to the SW compression task only can sustain/process an input data rate of:

$$25 \text{ Mclocks/s} : 180 \text{ clocks/byte} \sim 140 \text{ Kbytes/s}$$

or about twice the expected input data rate (65.5 Kbytes/s at a rate of 180 clocks per byte provides a rate of at least 11.8 MHz, margin excluded). This very preliminary result suggests that exploiting a faster CPU clock, the CDPU board could avoid a large SDRAM buffer, implementing only a faster SRAM memory to process the incoming data flow in a real time fashion.

Given the characteristics of the GR712RC dual core processor and the possibility to run it in the AMP mode, a single core could be devoted to the compression task only and the other core to the Instrument management tasks. This possible solution will be further studied during the next months, taking into account the complete set of processing tasks to be accomplished by the CDPU processor.

In order to reduce the computational load on the CPU, as alternative solution to the SW-based compression, an HW compression engine could be implemented in the companion FPGA on the CPU board. In particular, the adoption of the CCSDS121 IP core extracted from ESA Shyloc could be envisaged.

The RTAX FPGA implementation of this IP compression core can exceed the 1Mpixel/s performance on packets with 300 x 64 pixels, as shown by the results from the preliminarly performed simulations.

In this case the ICU architecture will be modified in order to:

- Perform the complete image pre-processing on the DCU FPGA;
- Send image data to be compressed to the HW compression engine in FPGA;
- Perform compression on packets + ancillary data provided by the CPU;

[9] Refer to the Metis coronagraph on-board Solar Orbiter and PLATO ICU compression algorithms

- Send compressed data to the S/C.

Similar architecture has been already adopted on the Imaging X-ray Polarimetry Explorer (IXPE) data processing unit based on a LEON 3FT single core processor complemented by an image processing engine implemented in HW.

More generally, the Ariel/ICU architectural design choices are based and rely on prototyping activities and model philosophies adopted, already implemented or ongoing implementation, by INAF and its Industrial Partners.

4.3 DCU board design

The AIRS Detector Control Unit design description is part of the AIRS Instrument literature [19], so here we will briefly present only an overview of the two main options for the CFEE designs assessment currently under study at CEA, Saclay (FR).

As anticipated, one is based on the adoption of the SIDECAR ASIC from Teledyne, as an heritage from the JUICE/MAJIS instrument design (and so for the DCU in particular), while the second one is based on discrete EEE parts selection, rather than the ASIC, leading to a customised DCU hosting on-board the A/D conversion function. In this case only the preamplifier for the ROIC output video signal is implemented into the CFEE. Others functions, along with the A/D conversion, such as the readout clock sequencer and bias generators are moved into the warm electronics, as shown in Figure 12.

The former DCU design for the SIDECAR CFEE option (refer to Figure 13), was instead similar to the MAJIS science channels processing electronics (PE) design and based on the heritage of the design adopted for the detector control units of the NISP instrument on-board the ESA Euclid Mission. In NISP the same kind of detectors have been used along with the same CFEEs (SIDECARs). An alternative architecture based on this heritage and higher TRL would allow the minimisation all the risks concerning the design, development, performance characterisation and testing activities of a unit presently under technology development.

This DCU alternative architecture hosts a FLASH-based reprogrammable FPGA (PROTO version) to offer maximum flexibility also in case of late top requirements specification (or modification) from the AIRS and Ariel Science Team. The selected FPGA, as baseline, is a Microsemi ProASIC3-type device offering the capability to embed a HDL FSM[10] with some programmable Science data pre-processing blocks (e.g. ramp slopes computing etc.) by means of a flexible parameters configuration that can be reprogrammed up to the EQM/FM unit. The FPGA also hosts a SDRAM memory controller to manage 128 MB of on-board memory used as a buffer to support the HDL-based pre-processing tasks.

Alternatively a Microsemi RTAX-family FPGA (in anti-fuse technology and so not reprogrammable, once burned, as OTP[11] logic) could be adopted in case of an early, exhaustive and clear requirements specification and CFEE selection.

[10] Hardware Description Language Finite State Machine
[11] One Time Programmable

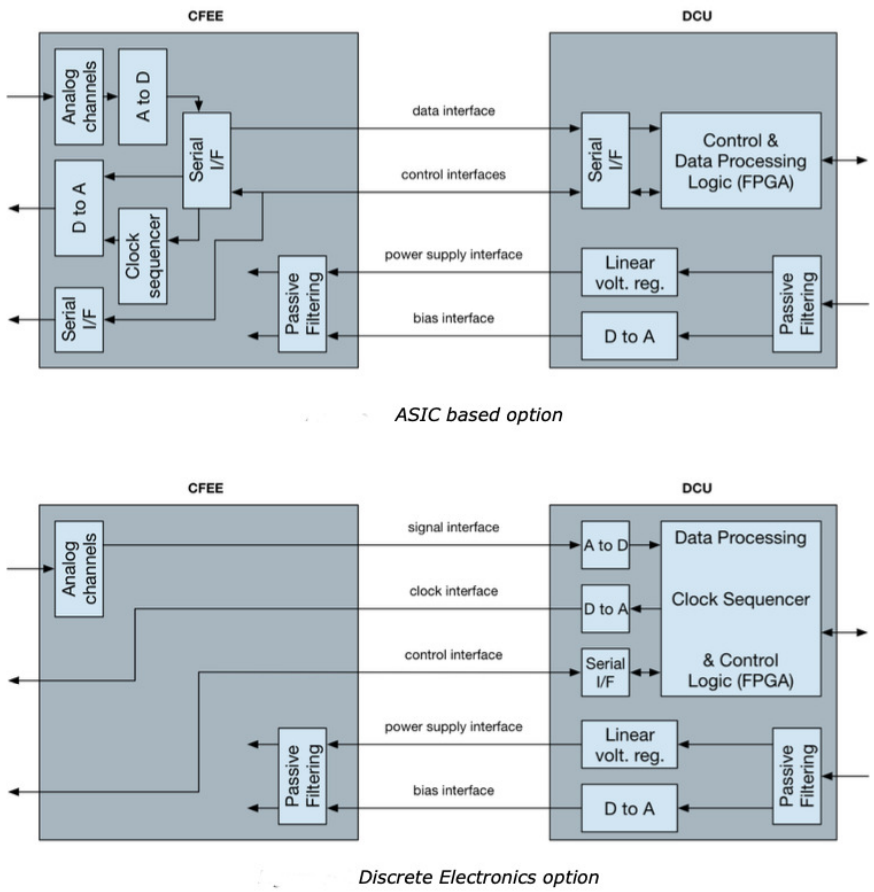

Fig. 12 CFEE to WFEE options, based on ASIC or discrete EEE parts - courtesy CEA, France

It is worth noting that for the NISP case the use of a reprogrammable FPGA for the logic device implementing the interface towards the CFEEs and detectors has been preferred for the following reasons:

- Request of maximum flexibility from the Euclid/NISP Team along with the DCU development process;
- Lack of knowledge of the actual behaviour of the logic interface to the SIDECAR: unexpected behaviour could also have required mitigation in the FPGA not known a-priori during the assessment phase;
- Risk of likely late modifications required on the FPGA design (e.g. concerning the implementation of updated high-performance pre-processing tasks): the chosen RTProASIC3 FPGA allows for the modification of the design via a JTAG port without opening the unit box and changing/removing the device.

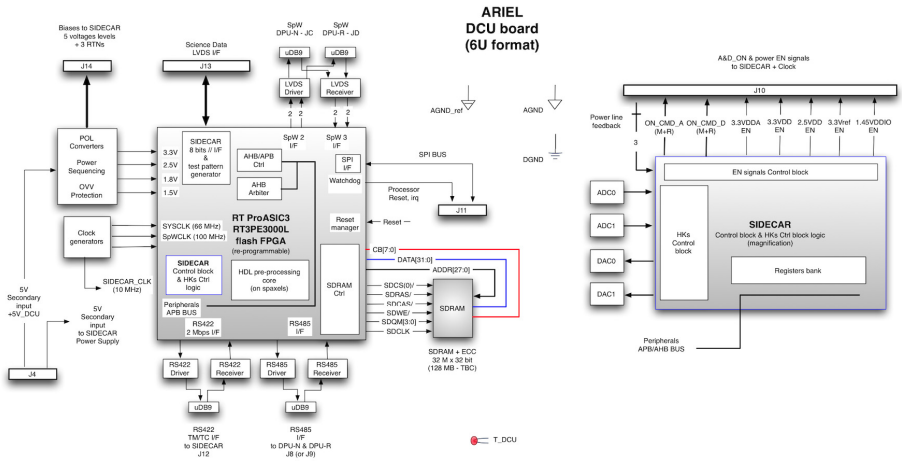

Fig. 13 Detector Control Unit block diagram

On the other hand, the use of a flash reprogrammable FPGA has the disadvantage of a lower level of immunity to radiation effects with respect to a FPGA based on anti-fuse technology (e.g. Microsemi RTAX-S family) and its radiation-hard design improvement requires a not negligible effort (e.g. I/O, at RTL level, logic placement, etc.), although for L2 radiation environment facing 50 Krad of Total Ionising Dose (TID) within the SVM can be assumed as a typical rad-hard requirement[12].

For this reason, the standard rad-hard FPGA flight-grade design flow should be modified with the introduction of radiation mitigation activities up to the validation with EM and EQM models, but this risk can be properly assessed and addressed by the Ariel Consortium, as the Industry involved in the NISP development already acquired all the needed knowledge and competences to interface and drive the Teledyne SIDECAR + H1RG detector system.

The DCU board is in charge of SIDECAR clocking (at least a master clock is needed for the ASIC) and feeding (secondary finely regulated voltages produced by an on-board PoL) and it collects digitised scientific data and HK (currents, voltages and temperatures) describing the ASIC status. The needed enabling and control signals for SIDECAR management are represented in Figure 13, on the right magnification of the blue box inside the FPGA block diagram. Three different grounding references (analog and digital) are foreseen for a clean power supply feeding.

In particular, in the NISP data acquisition chain, the SIDECAR Science I/F is based on an 8 bits LVDS parallel I/F (with data buffering and packets CRC) and a TM/TC I/F running at 2 Mbps (serial syncro) plus a master clock line running at 10 MHz. The CDPU I/F shall be based instead, on SpW for Science data TM along with a RS485 serial I/F offering the capability to manage and configure the DCU

[12] Indeed this value is a function of the SVM shielding material and here is reported only as a worst case for a SVM bench based on CRFP (no or only partial Al shielding)

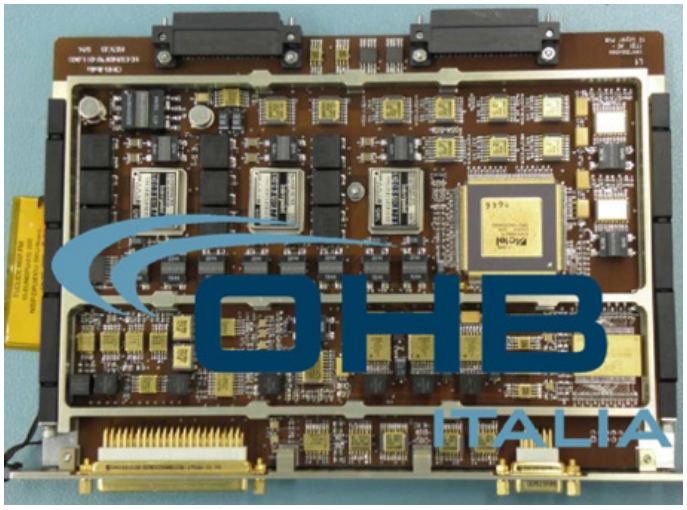

Fig. 14 DCU FM model SN10 board for Euclid/NISP

FPGA from CDPU. Alternatively, the FPGA registers could be managed thanks to the RMAP protocol running on SpW.

An important issue of the electrical I/F to the SIDECAR ASICs is the harness, electrically and thermally linking the WFEE part of the electronics (working at the Service Module temperature of 270-300 K) and the CFEE part (that should work at an optimal T < 60 K, on the Payload's optical bench). For this kind of harnessing it is foreseen, as in NISP, to split the electrical connections in different parts, or mated cables, characterised by different thermal conductivities (e.g. copper, constantan or manganine, phosphor bronze, stainless steal, etc.) in order to be properly connected to the three V-grooves heat sinks, cooled down passively at decreasing temperatures.

			Nominal Value
VDDA	SCS 3.3V analog power output voltage	Power supply with remote sensing. Referenced to AGND	3.3V
Vref	SCS reference voltage	Referenced to AGND_Ref	3.3V
VDD3V3	SCS 3.3V power output voltage	Referenced to DGND	3.3V
VDD2V5	SCS 2.5V power output voltage	Referenced to DGND	2.5V
VDDIO	SCS IO power output voltage	Referenced to DGND	1.45V
VSSIO	SCS IO power output voltage	Referenced to DGND	0.9V

Table 6 Voltage references and grounding for SIDECAR ASIC power feeding

The Euclid/NISP DPU/DCU FM unit (refer to Figure 15) includes 8 DCU boards; 2 DPU/DCU units [18] have been already successfully tested in a thermo-vacuum chamber at LAM (Laboratoire d'Astrophysique de Marseille, France), integrated with a focal plane composed by 16 SIDECAR + 16 H2RG detectors.

Fig. 15 Euclid/NISP DPU/DCU FM unit

In a nutshell, the Ariel DCU (as a clone of the NISP DCU) has the following characteristics:

- TMTC I/F with SIDECAR for commanding and telemetry acquisition
- 8 bit parallel science I/F with SIDECAR
- Detector clock generation and synchronization among the different DCUs
- 5 very low noise power supplies + voltage reference generator with power sequencing, voltage adjustment via DAC and return current isolation, overvoltage and overcurrent protections
- Very clean grounding scheme
- 128 MByte local SDRAM buffer EDAC protected for storage of incoming frames to be processed
- Reprogrammable FPGA for data preprocessing
- Low total power consumption (< 3.5W)
- 2 DCU power supplies: +5V for digital part, isolated +28V primary supply for SIDECAR power generation
- Double Eurocard form factor
- Controlled via SpW RMAP links

The Ariel DCUs, both baseline and alternative designs, are conceived to be cross-strapped with two cold redundant assemblies composed by a power supply unit (PSU) and a main controller (CDPU). The Ariel DCU alternative design is based instead on the design qualified for EUCLID/NISP with minor modifications limited to the embedded FPGA firmware and the implementation of the RMAP I/F protocol.

4.4 TCU short description

The Telescope Control Unit will be in charge of accomplishing the following tasks, during Ariel Science and Calibration modes:

- Drive the M2 Mechanism
- Drive the IR calibration sources
- Monitor thermal state of several elements of Ariel telescope
- Control thermal stability of the primary mirror (M1) during observations
- Communicate with ICU's CDPU and transmit HK data from sensors, calibration source, M2M, etc.

TCU, as a slave subsystem of the Instrument Control Unit (ICU), will be based on a cold redundancy philosophy: all subsystems and sensors will have a redundant counterpart, where nominal elements will be connected to nominal ones, and redundant elements will be connected only to redundant ones. No nominal board will be able to read or control a redundant sensor/actuator, since they will be electrically isolated. With this configuration, cross- strapping inside the TCU box is avoided, reducing system complexity, mass and power consumption.

The selection of N or R systems will be performed by the S/C by providing the required power (+28V) to one or the other by means of a dedicated harness.

The ICU will control TCU and share information with it by means of a cross-strapped LVDS SPI bus to the TSIRC (Thermal Stabiliser and Infrared Calibrator) board hosting a rad-hard FPGA with a Finite State Machine (FSM) to switch between states that perform specific tasks.

A 6U PCB will host the PLM thermal monitoring and its multiplexing stages, M1 heaters driver, Calibration lamp driver and the digital system in charge of managing the whole TCU. For the driver electronics of the M2 mechanism, an upgraded version of Euclid's M2MM is foreseen: the driver will require a separate 6U board for both nominal and redundant systems.

In order to provide the proper voltage levels to all TCU boards from the main +28V power bus coming from the S/C, a Power Supply Unit is foreseen in the TCU's design. The TCU-PSU design will be based on the Sener-Spain heritage of past successful power units, with special attention to M2M power requirements. It will distribute power to all TCU board and communicate with the TSIRC board by means of a backplane. The digital system in TSIRC will gather its HK telemetry while enabling and disabling power rails depending on the systems state (e.g. disable M2MD DC/DC if not in "Calibration" state).

The digital system of TCU will consist of a FPGA (RTAX2000SL, as baseline) with an HDL FSM hosting a firmware that will be devoted to control all TCU boards as a slave system of ICU, in order to simplify the overall P/L SW architecture and database. The FPGA will be hosted in the TSIRC board as well as its PoL converters to generate the proper voltages for GPIO interfaces and internal cores.

5 ICU On-Board Software and data handling functionalities

In the following, a summary of all the ICU data handling functionalities is provided, with an indication of the involved unit:

- **CDPU**: Telecommands handling, Instrument (AIRS) commanding and control, science data acquisition and compression (lossless algorithm, SW or mixed HW/SW implementation), ICU and P/L HK acquisition and monitoring, instrument FDIR implementation, data packetisation and TM flow management;
- **DCU**: AIRS detectors and CFEEs ($CH0$ and $CH1$) management, data flow control by means of algorithms based on a HW implementation (FPGA-based);
- **PSU**: no data handling functions are implemented on-board, HW HK data only (ICU internal currents, voltages and temperatures) will be collected and converted in digital format, to be sent to CDPU for active monitoring.

In particular, the Ariel On Board Software (OBSW) running on the CDPU board will be composed of the following three main components:

1. Boot Software: it is installed on the PROMs of the ICU CDPU board and allows loading/deploying the ICU Application Software in RAM. It comprises all the low level drivers for the CDPU board and its related interfaces involved in the bootstrap process.
2. Basic Software, or Basic Support Package (BSP): basic I/O SW, Service SW & Peripheral Drivers; it is a hardware-dependent Software including the Software Drivers for all the internal and external ICU digital interfaces. This SW is used by the Application SW and can depend on the selected operating system (OS).
3. Application Software: it is composed by two parts:
   - the Instrument Control & Configuration Software: it implements the Ariel scientific payload handling, TCU included. It controls the AIRS spectrometer, implements the operating modes, monitors the instrument health and runs FDIR procedures. It implements the interface layer between the S/C and the instrument.
   - the AIRS Data Processing and Compression Software [15]: it implements all the necessary on-board processing functionalities, included the on-board lossless compression. After the compression the SW prepares CCSDS packets for the transmission to the S/C Mass Memory Unit (MMU).

Boot SW and HW-dependent SW are strictly related to the ICU HW. Their development will be part of the activities included in the industrial contract for the ICU provision. The criticality analysis for these SW components will be part of the documentation to be provided by the industry, which will be selected as ICU Prime Contractor. For this part of SW components the ICU Prime shall also consider the ESA-SAVOIR[13] guidelines and alternatives.

The Real time operating system will be purchased as a commercial off-the-shelf (COTS) part.

[13] Space AVionics Open Interface aRchitecture

5.1 Boot Software

The boot software will be stored in a PROM device, while EEPROM (or similar non-volatile memories) will be used to store two or more images of the Application Software. The boot software will be started automatically at the ICU power on and will be in charge of loading and starting the Application SW. The boot process is driven by commands produced by the Spacecraft.

The boot SW will be designed to load and start either one of the ASW images stored in EEPROM or a new ASW image received by means of specific Telecommands; in particular, a series of memory management Telecommands ("memory load") can be used to store in RAM a complete new ASW image, which is then started at the reception of a specific command to jump to the ASW starting RAM address.

The boot procedure described above offers good reliability arguments because:

- If the EEPROM is corrupted, the boot can still load an ASW image via "Memory Load" Telecommands.
- If any RAM cells in the area to be occupied by the ASW are damaged, a new image, which does not use that memory locations, can be built on ground and uploaded via specific Telecommands.

This procedure does not eliminate the risk of a memory damage in PROM (on one or more cells used to store the Boot SW) or in the portion of RAM used by the boot SW. In this case, unrecoverable failures of the boot process will be triggered and a switching off of the nominal CDPU and a switching on of the redundant one is mandatory.

There are some drawbacks related to the implementation of this kind of boot procedure. In particular, the boot program will be quite complex, needing to handle the exchange of SpW packets with the S/C (even if only a very limited set of packets is to be supported), and the size of the code could be quite big if compared to the simplest boot programs, making it challenging to fit it into a PROM device. Nevertheless, this approach has been selected based on the heritage of many previous projects (e.g. the ESA Herschel mission, with three payload instruments; the ESA Euclid mission, VIS and NISP instruments) as it added flexibility and increased the overall robustness of the unit against failures, allowing to perform many analysis also at boot level.

5.2 Application Software

The Ariel payload commanding and control functionalities will be guaranteed by the implementation of the ESA Packet Utilisation Standard (PUS) services specified in ECSS-E-ST-70-41C.

In Table 7 the list of PUS mandatory services, as defined in ECSS-E-70-41C and required by the Ariel Mission, is reported.

These services will be fully implemented. In addition, the Function Management service (Type 8) will be used to implement the Instrument Commanding (TBC). This choice is based on the heritage of what implemented on board the ESA Herschel

Type	Service Name
1	Telecommand verification service
3	Housekeeping & diagnostic data reporting service
5	Event reporting service
6	Memory management service
9	Time management service
12	Onboard monitoring service
17	Test service
20	Parameter management service
≥128	Science

Table 7 ICU mandatory PUS services

and Euclid missions: the Function Management Service provides all means for implementing an efficient and effective system of instrument Commanding and control Telecommands (TC). The Telemetry Packets (TM) necessary for monitoring the on board activities will be defined as part of the housekeeping and diagnostic data reporting service. The Application Software (ASW) will be developed on top the selected real time operating system and will make use of the hardware related basic software drivers libraries.

The ASW development plan, with the related SW reviews and deliveries, will be driven by the Ariel Consortium needs, on one side, and by the availability of all external items needed for the SW testing activity, i.e. the S/C simulator, the Central Checkout System (CCS) simulator and the Telescope (thermistors, heaters, etc.) and Spectrometer detectors (and CFEEs) simulators. In parallel, an ICU SW simulator shall be delivered to the Institutes in charge of the SW and FW development for the other units, if required.

6 Power and mass budgets

The ICU power and mass budgets (refer to Table 8) are provided as a worst case, based on the architecture hosting the baseline DCU design.

These budgets assessments are based on the DCU architecture proposed by CEA, whose expected power consumption in nearly the same of the NISP DCU design, interfacing the AIRS CFEEs based on a design exploiting discrete EEE components and exploiting the Solution B for the CDPU board (hosting an FPGA along with the processor).

ICU alternative solution with discrete electronics as CFEE							
ICU subsystem	Subsystem/electronics component	Consumption W	Boards #	Total W	Mass Kg	Boards #	Total Kg
CDPU						(6U format)	
Note: consumption based on an actual CDPU board on Science Mode	GR712RC @ TBD MHz FPGA (RTAX1k-type - TBD/TBC) 8 MB SRAM (TBC) 8 MB NVM (MRAM or NOR FLASH) 128 KB PROM TBD Mbytes SDRAM (TBC)						
	Total	7,90	1	**7,9**	0,65	2	**1,30**
	Applicable margin			0,10			
	Total with margin			**8,69**			**1,43**
DCU						(6U format)	
CEA estimate	FPGA Memory Other components						
	Total	4,30	2	**8,6**	0,75	2	**1,50**
	Applicable margin			0,20			
	Total with margin			**10,32**			**1,80**
PSU						(6U format)	
	Static power	2,50					
	Sequencing section	2,20					
	DC/DC efficiency (70% @ 28V Vin - TBC)	9,09					
	Total	13,79	1	**13,79**	0,8	2	**1,6**
	Applicable margin			0,15			
	Total with margin			**15,85**			**1,84**
Box							
	Chassis				2,15	1	2,15
	Back panel				0,2	1	0,30
	Total						**2,45**
	Applicable margin			0,20			
	Total with margin						**2,94**
	Grand TOTAL (margins included)			**34,86**			**8,01**

Table 8 ICU baseline architecture Power and Mass budgets (for the expected worst-case configuration accounting for parameters, like system clock(s), still to be finally defined; additional system margin for the Ariel warm units, not shown here, is available)

7 ICU Thermo-Mechanical design and analyses

7.1 Mechanical design

The ICU 3D mechanical design is shown in Figure 16. It foresees a set of six drawers (refer to Figure 17) plugged into a back-plane supported by the bottom panel, hosting the connectors for the following PCBs:

- 2x PSU (N & R) boards
- 2x CDPU (N & R) boards
- 2x DCU (both N) boards

The present allocated dimensions by ESA for the box envelope are 320 mm x 185.1 mm x 220 mm (length x width x height). Presently, the ICU dimensions from CAD design are 292.5 mm x 158.6 mm x 197.6 mm, so some margin (more than 10 mm/dimension) is still available for a better accommodation of PCB, EEE components and tracks routing during the PCBs executive design phase.

The present dimensions for the ICU box design concern the implementation of the NISP version of the DCU design, while for the CEA customised design implementation an increase in height is expected up to 270 mm in order to include the AIRS TCS

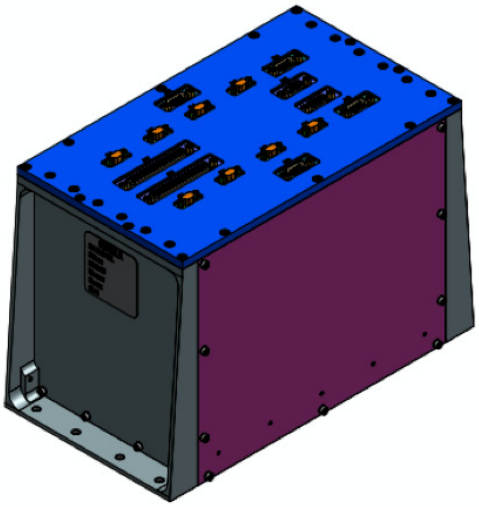

Fig. 16 ICU box mechanical design

on-board DCU. The definition of the electronic boards dimensions and box height is still under assessment and shall consider the possibility to adopt a piggy-board configuration (refer to Figure 18).

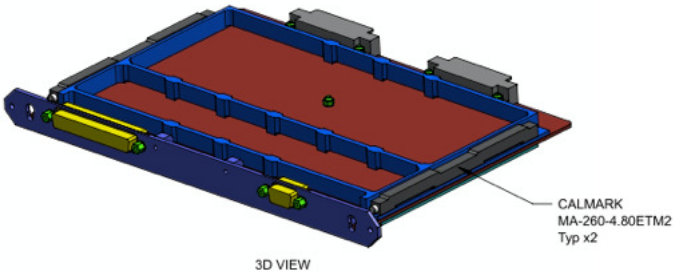

Fig. 17 3D view of a PCB with its mechanical frame and card-lock retainers for stiffness improvement and a proper thermal dissipation to the box and to SVM bench

The panels of the ICU box will be manufactured in an Aluminium alloy and then externally painted in black (except the bottom panel) if needed to improve radiating exchange with the environment, while assuring a proper thermal conduction towards the SVM bench.

The ICU box will internally host the grounding reference point along with a bounding stud and at least a N and a R TRP (Temperature Reference Point) for moni-

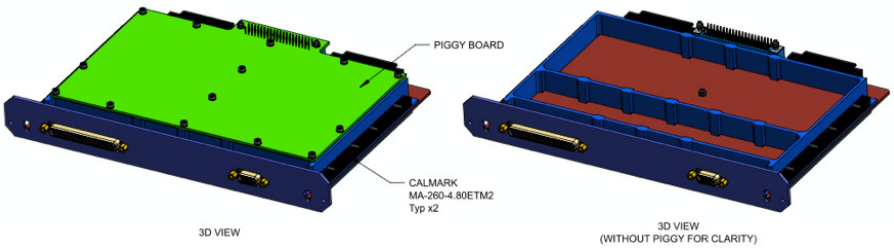

Fig. 18 3D view of a customised PCB hosting a piggy-board

toring the Unit temperature (in charge of S/C). The drawers thermo-mechanical coupling with the box structure will be done thanks to the adoption of card-lock retainers, ensuring a proper thermal conduction and heat dissipation toward the SVM bench by means of the lateral panels and ribs. Connectors shown in the mechanical design are not fully representative, but it is expected to adopt MDM micro-d type, 9 poles, for SpW TM/TC and SPI signals; DSUB, 9 poles, for power signals).

7.2 Structural model and analyses

The ICU structural analysis has been carried out with a NASTRAN model, whose expected FEM mass is 6.7 kg (20% of mass contingency excluded). The main result of the structural analysis, the 1st eigenfrequency equal to 189.77 Hz, is larger than the required value of 140 Hz, as shown in Table 9.

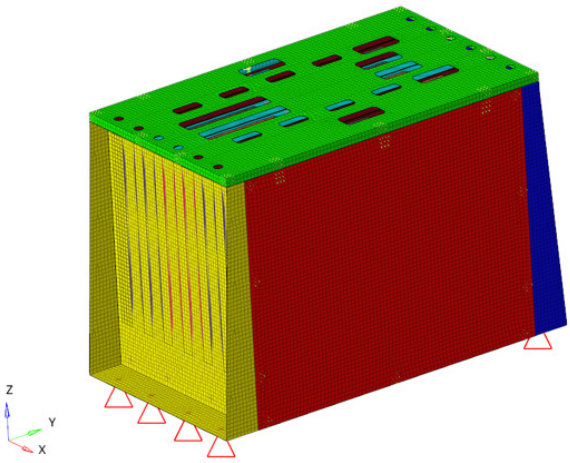

Fig. 19 ICU 3D NASTRAN model

MODE N.	FREQ. [HZ]	EFF. MASS TX	EFF. MASS TY	EFF. MASS TZ	EFF. MASS RX	EFF. MASS RY	EFF. MASS RZ
1	189.77	**67.14%**	0.00%	0.02%	0.01%	**66.82%**	**30.60%**
2	261.25	0.00%	0.00%	1.00%	0.41%	0.29%	0.00%
3	274.45	0.03%	0.00%	0.00%	0.00%	0.27%	0.01%
4	292.11	0.00%	0.00%	0.00%	0.00%	0.05%	0.00%
5	301.46	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%
9	309.36	0.00%	0.00%	**5.57%**	2.29%	1.64%	0.00%
11	374.08	0.00%	**53.53%**	0.00%	**58.67%**	0.00%	**12.59%**
12	406.60	0.00%	0.00%	**90.61%**	**36.18%**	**25.16%**	0.00%
47	761.21	0.00%	**38.06%**	0.00%	0.25%	0.00%	**9.26%**
105	1122.84	0.00%	0.00%	0.00%	0.00%	0.00%	**7.77%**

Table 9 ICU eigenfrequencies

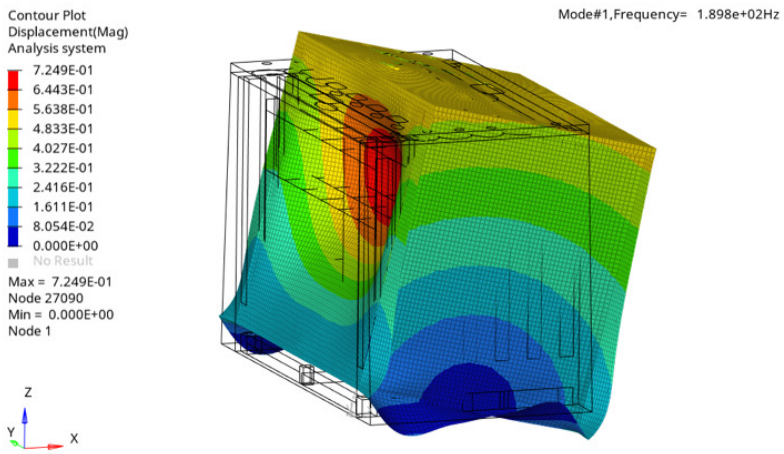

Fig. 20 First eigenfrequency mode displacements

DLL (Design Limit Loads) stresses have then been applied to the unit (20g in-plane, 25g out-of-plane) and resulting stresses have been extracted, showing that all Margins of Safety (MoS) are positive (refer to Table 10).

ITEM	LOAD CASE	Fty [MPa]	Ftu [MPa]	Limit Stress [MPa]	SF_Y	Sf_U	MoS_Y	MoS_U
Aluminum parts	101	386	462	48.1	1.10	1.25	6.30	6.68
PCB	101	NA	482	5.99	NA	1.25	NA	63.37

Table 10 Finite Element Analysis MoS

7.3 Thermal model and analyses

The ICU thermal analysis has been firstly developed considering only the conductive processes through the baseplate during the heat exchange with the environment. Both the conductive and the radiative processes have been taken into account for the internal heat exchange with the following values:

- Mechanical elements: Al7075 k = 130 W/mK, $\varepsilon = 0.03$
- PCB: Copper k = 400 W/mK (equivalent thickness), $\varepsilon = 0.8$

and a qualification temperature of 50 °C at TRP (Temperature Reference Point).

EEE components heat dissipation has been considered evenly distributed on PCB modules as reported in Table 11, showing the expected heat loads on each electronic board (Nominal, Redundant and cross-strapped)

Board	Heat Load [W] (20% contingency included)
PSU Main	14.4
CDPU Main	9.42
DCU CH0	3.96
DCU CH1	3.96
CDPU Red	OFF
PSU Red	OFF
Total	**31.74**

Table 11 PCBs heat loads. Note that these values are slightly different of those reported in Table 8, resulting from the latest power budget available update

The thermal analysis has shown the following results (predicted temperatures):

- Max calculated Tcalc= 69.4 °C on active PSU PCB
- Max predicted Tpred = Tcalc + uncertainty = 69.4 + 10 = 79.4 °C

showing no issues for the operability of the selected main EEE components.

8 Conclusions

With this paper, the role of the Instrument Control Unit within the Ariel Payload along with its updated electrical and thermo-mechanical design, following the ESA's P/L System Requirements Review (pSRR), have been presented. Some design options are still open, in particular concerning the DCU architecture driving the AIRS

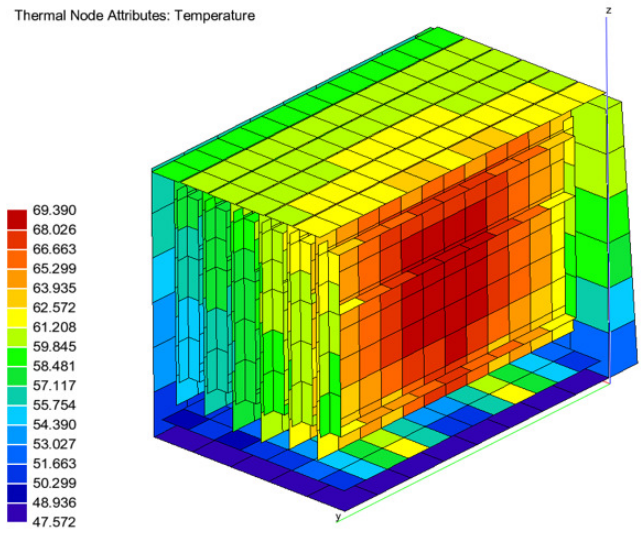

Fig. 21 PCBs predicted temperatures

cold front-end electronics (SIDECAR ASIC or based on discrete EEE components) that, regardless of its final implementation, requires particular care for the components selection, its thermal stability and the capability to provide noise-free and very stable voltage levels towards the CFEEs. These thermo-electrical stability requirements shall be further assessed prior and after the Mission Adoption Review (MAR), presently expected by November 2020, once better know the Ariel Mission operational scenario (e.g. S/C pointing, slews, etc.) and the ICU thermo-mechanical environment and constraints, as defined thanks to the next co-engineering sessions with ESA and the Spacecraft Prime, whose selection and negotiation phase is expected in summer next year, following the MAR and Invitation To Tenders (ITT) processes.

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