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WP3: Baseband processing and Beamforming

D3.1: Antenna array system based on classical GNSS antennas

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Abstract:

This document shows the structure of the antenna array SM103DS. This module consists of an RF front-end section and an antenna section. The module enables the study of beam-forming techniques on an array with up to nine freely selectable antennas.

Keyword list: ***GNSS receiver, reconfigurable antenna, beamforming techniques***

Executive Summary

This document provides a description of the work performed in the frame of GRABEL (WP3) with respect to the RF section and the antenna beam-forming array. In this document the RF section prototype for the GRABEL receiver is described. This RF section consists of a carrier board holding the antennas and the RF front-end modules, and containing interface and control functions. With this prototype the antenna array can be reconfigured by plugging antenna modules onto the carrier board in appropriate positions, to form various square, hexagonal or cross and 'T'-shaped beam-forming antenna arrays. Its purpose is to evaluate various antenna configurations in order to find the most appropriate one for GRABEL, from the point of views of beam-forming performances and size of the array. For the hexagonal array a prototype with solid copper ground plane was constructed. The antenna module is based on a standard patch antenna and includes an optional LNA. The RF front-end is designed around an ASIC (SY1006A) and can receive both GPS L1 (C/A-code) and Galileo BOC(1,1) signals. An interface to the base-band processor and to the CSEM reconfigurable antenna completes the system.

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1 Introduction and high-level description

The GRABEL receiver requires an antenna array in order to implement beam-forming. The best beam-forming performances (sharpest lobe, highest gain) are in general achieved by using a large antenna array. Since the GRABEL receiver - and thus its antenna array - must also have 'practical' dimensions that fit the intended applications, there is a necessity to find a good trade-off between beam-forming performances and size of the receiver.

The main objective of this work is the implementation of a system allowing the evaluation and test of various beam-forming configurations, using a specifically designed breadboard. The built breadboard is able to implement different antenna array configurations, such as square, hexagonal, cross and 'T'-shaped, such that they can be directly compared and evaluated. For the hexagonal configuration a prototype with solid copper ground plane was then constructed.

Obviously the breadboard configuration has necessarily a size that is larger than necessary, but the different possible configurations can be used to determine the most desirable solution, which should hopefully confirm the theoretical and simulated results, further enabling the implementation of an efficient and stable prototype.

2 RF System Organization

In order to allow reconfigurability of the antenna array, a modular rather than a single board approach has been selected. The system therefore consists of a carrier board - named SM103 - on which antenna modules - named SM101 - can be plugged in various positions to form the desired antenna arrays. On the same board up to 9 RF front-end modules - called EB1006A - can be plugged and controlled. The module SM101 is based on conventional GNSS patch antennas. Figure 2.1 shows a photograph of the complete system, with 9 EB1006A and 4 SM101 modules inserted on the SM103.

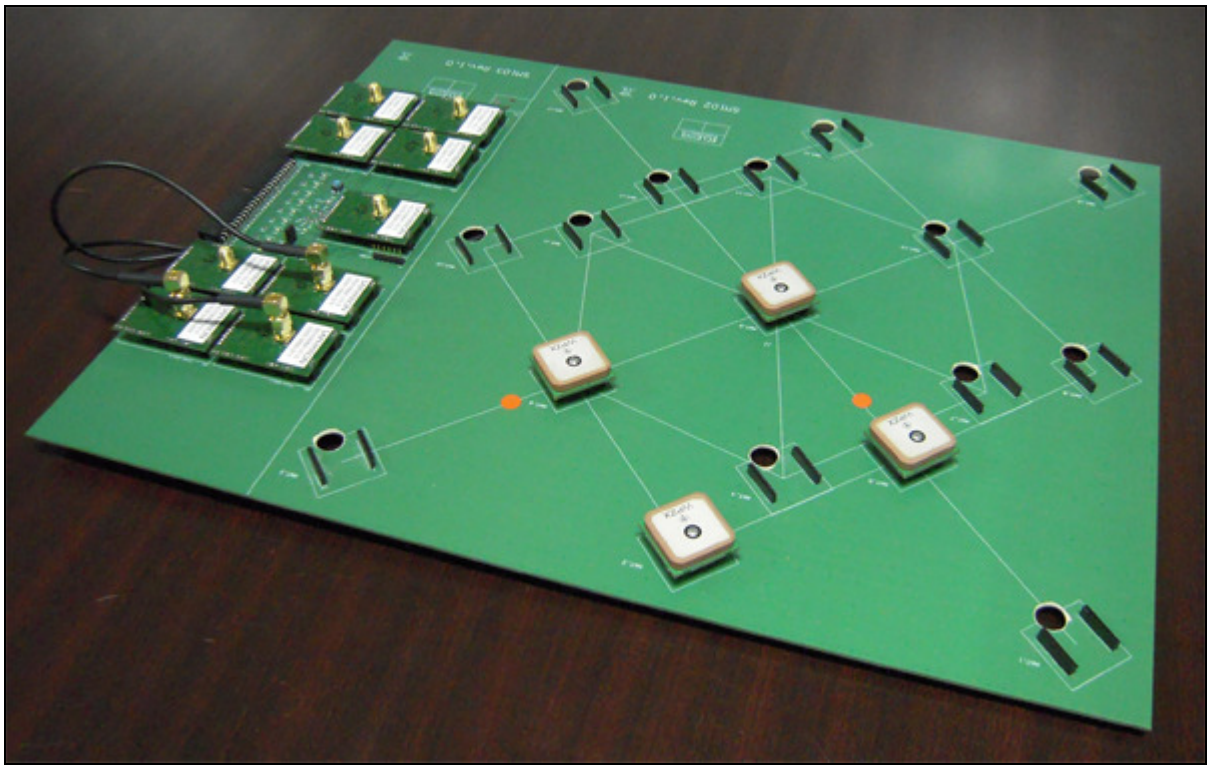

Figure 2.1: SM103 module

2.1 SM103 Carrier Board

The SM103 carrier board consists of 2 sections: the first section contains all electronics, i.e. the reference clock distribution, voltage regulators, interfaces and control logic, and carries up to 9 EB1006A RF front-ends. This section, which is shown in Figure 2.2, can be separated from the antenna array if desired. Using separate RF boards, rather than designing the RF front-ends on the SM103 board, has been preferred since all critical RF wiring is kept on a small easy to align module, while possible interference especially from the digital logic on the main board is minimized. The cost is just a small increase of complexity. The block diagram of the SM103 appears in Figure 2.3.

All digital signals are brought out on a single header that is typically connected to the base-band processor. On the header there are 9 data interfaces (sign, magnitude), the clock (provided by the base-band processor), the I2C interface (data and clock), the output interrupt signal, and the 5V and I/O (from 2V to 3.6V) power supplies. Interface to the reconfigurable antenna (CSEM) is brought out on a RJ10 connector, which provides both the I2C bus and the power supply (5V).

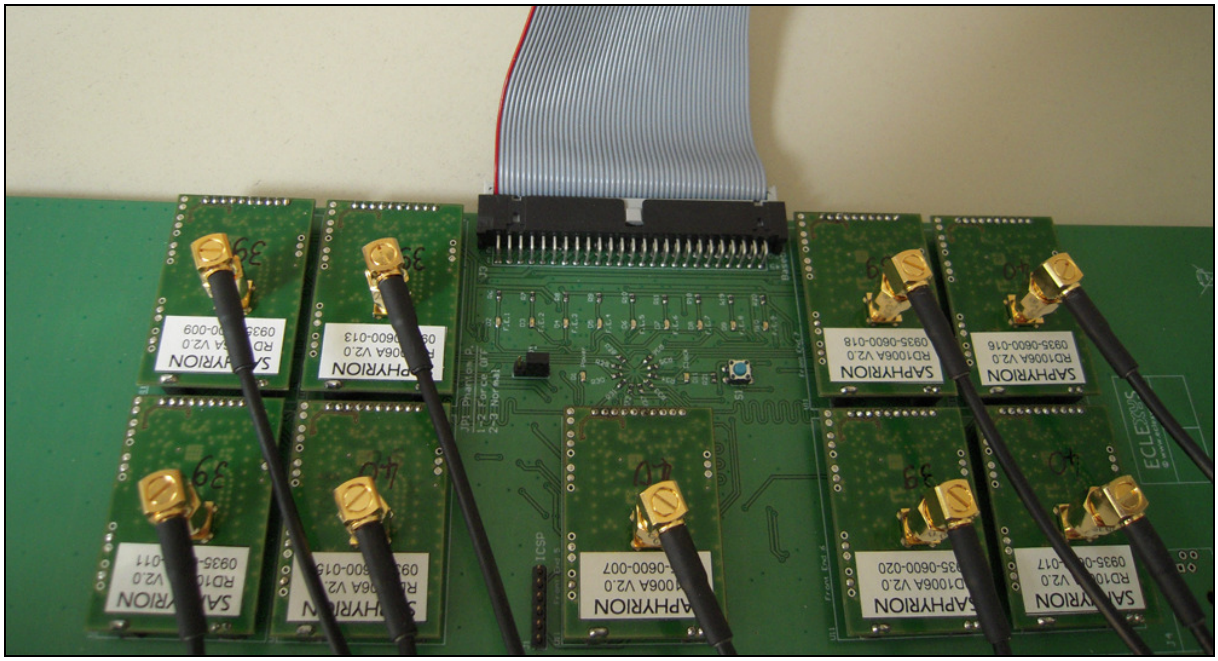

Figure 2.2: Detail of the SM103 module, front-ends

The second section of the SM103 is the actual antenna array. This section is just a carrier for the SM101 antenna modules and does not contain any electronics. Connectors (with all pins grounded) provide mechanical support for the SM101 antenna elements. Up to 9 SM101 can be plugged in 17 different positions to form different spatial configurations.

The dimensions and positions of the antennas is dictated by simple physics, not by technology. Ideally the distance between the phase centers of the antennas shall be l/2. In fact:
If the distance between phase centers is much less than l/2 the antenna array basically operates as a single antenna and no beam-forming will be possible.
If the distance is much larger than l/2 secondary lobes and interference zeros will form due to spatial aliasing. Interference zeros will occur at any l/2 distance and have a hyperbolic shape, while secondary lobes can have the same magnitude as the desired main lobe.
A spacing of l/2 at the L1 frequency (1575.42MHz) - i.e. 9.5cm - has therefore been chosen for the design of the SM103 antenna array.

It is important to stress again that this spacing is *dictated by physics* and has *nothing* to do with technology, performance of the antennas or the control algorithms used. Better antennas or improved control algorithms cannot change physics, therefore it will always be impossible to miniaturize the antenna array any further (or also use larger antenna spacings for instance).

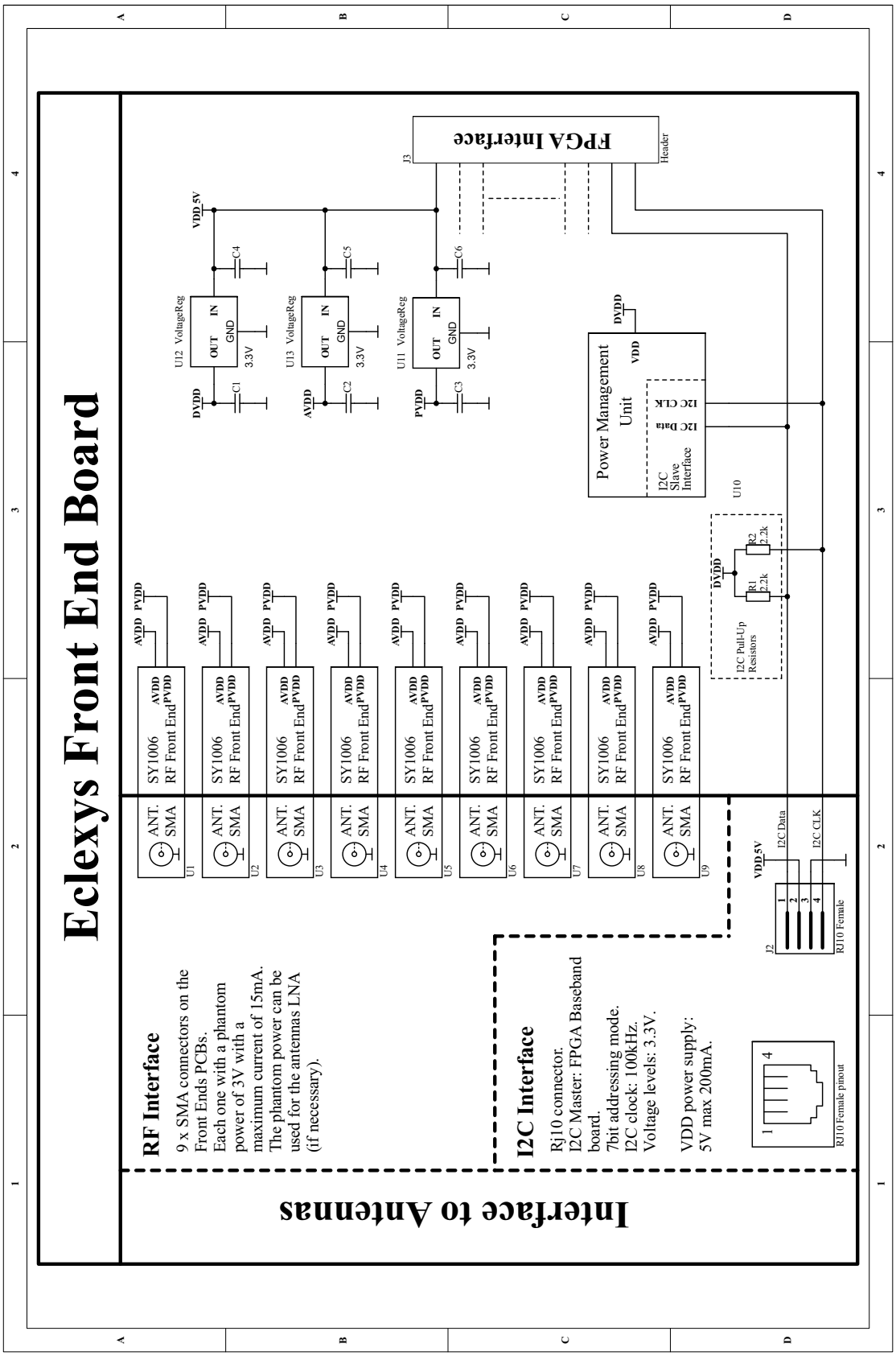

Figure 2.3: SM103 Block diagram

2.2 SM101 Antenna Module

The SM101 antenna modules are based on a standard patch antenna and contain an optional LNA. Figure 2.4 shows a photograph of two SM101 antenna modules.

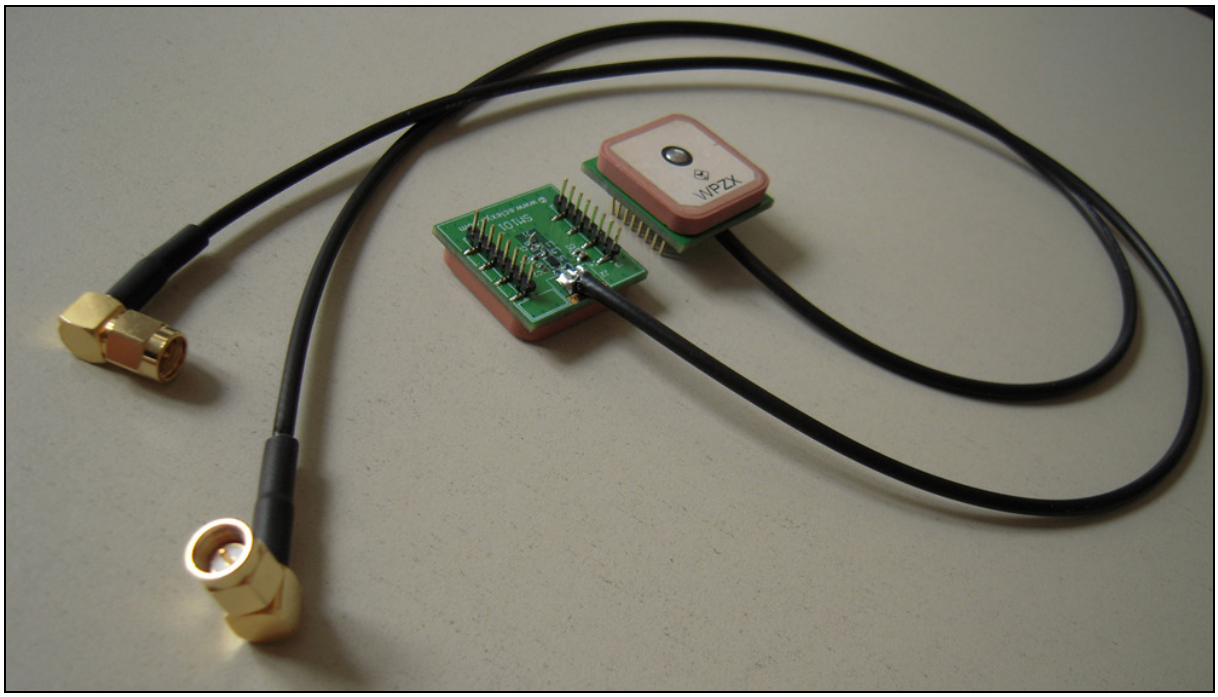

Figure 2.4: SM101 patch antenna test modules

The antenna selected is a standard patch antenna for GPS, and is manufactured by On-Shine Co (Ltd) Taiwan, under part number DAS1575R25. It is a square patch antenna, with RHCP polarization and a size of 25mm x 25mm x 4mm. Its gain is up to +4.5dBi at the zenith when mounted on a large ground plane (7cm x 7cm or bigger).

Since a large ground plane is obviously not possible in this application (space would be insufficient) a ground plane of 26mm x 26mm was used instead, i.e. the smallest recommended ground plane size according to the antenna manufacturer. The patch antenna was then tuned by the manufacturer itself for that ground plane size (this is a standard service that all patch antenna manufacturers offer). The antenna mounted on the 26mm x 26mm ground plane has a gain at the zenith of about +2dBi, has a slightly sharper main radiation lobe and has a small spurious LHCP lobe pointed backwards.

In order to compensate for the losses of the cable (when necessary) an LNA has been placed on the back side of the antenna ground plane. For the LNA a standard 6 pins SC70 footprint has been used. The majority of IC LNAs conform to this footprint, thus the use of various brands and types of LNA is possible. The LNA is phantom powered and - if sufficiently short cables are used - it can be omitted completely.

2.3 EB1006A RF Front-End Module

The EB1006A is an RF front-end module for the GNSS L1 band, which was actually designed as an evaluation board for the SY1006A front-end IC and which allows all functionality of the SY1006A to be tested and evaluated. This module implements a superheterodyne RF front-end with 1st IF at 20.46MHz, 2nd IF at 4.092MHz and a signal bandwidth of about 3.5MHz. Thanks to its relatively small size and good configurability (signal bandwidth, clock frequency) it suits very well the GRABEL receiver application.
A photograph of the EB1006A is shown in Figure 2.5. It includes the SY1006A which implements the complete RF receiver and a voltage regulator that supplies the clean power supply to the analog section of the SY1006A. Channel filtering is provided by a SAW filter and a 4th order LC filter.

Connection to the external world is via an SMA connector for the RF input and a single header for the digital interface. Two small headers with the pins grounded provide mechanical support. The EB1006A pictured without shield in Figure 2.5 also shows the configuration jumpers and the reference TCXO. These parts were omitted on the EB1006A modules prepared for GRABEL.

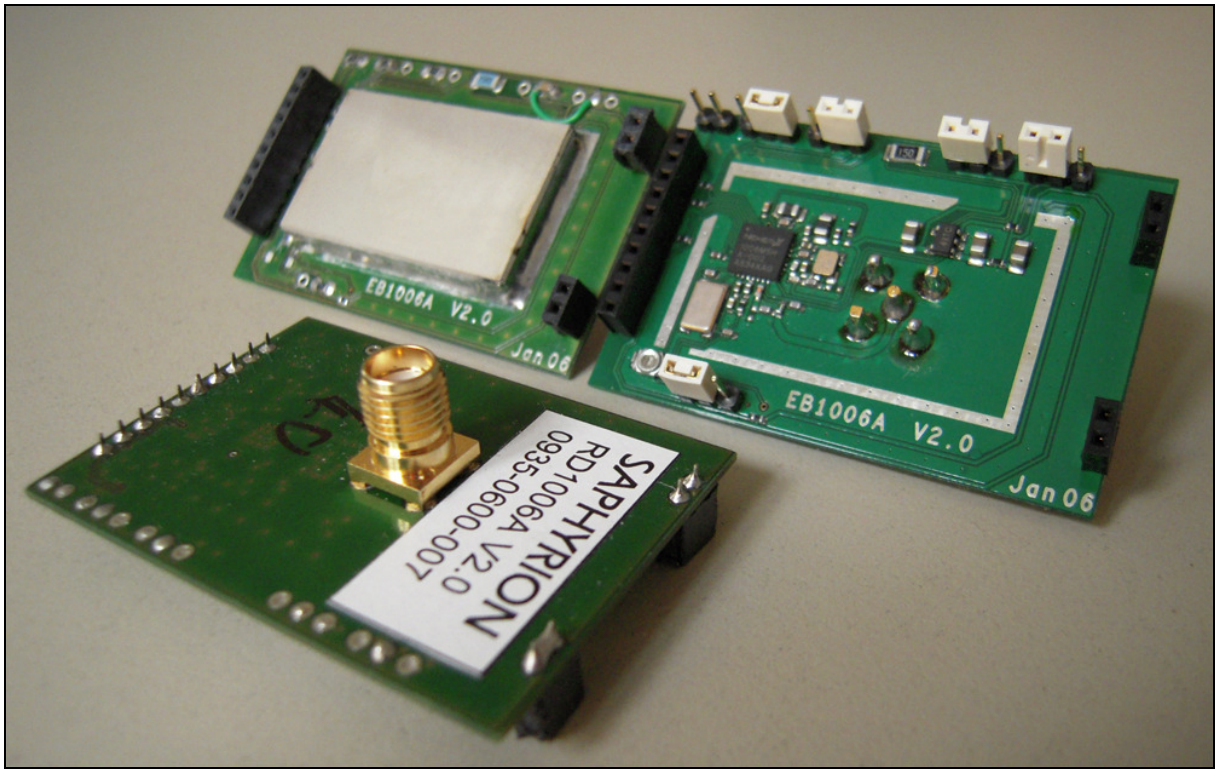

Figure 2.5: SY1006 RF front-end

The SY1006A IC mounted on the EB1006A is a highly integrated, low noise RF front-end for GNSS receivers targeted towards portable and automotive applications. The block diagram of this device is shown in Figure 2.6.
The SY1006A is a double super-heterodyne receiver for the GPS L1 band. It includes the complete signal path, consisting of an LNA with a noise figure around 1.6dB to accept either passive or active antennas, a single-balanced mixer which converts the RF signal to the 1st IF of 20.46MHz and an IF-strip with AGC. A 2-bit AD-converter converts the IF signal to digital and performs the 2nd frequency conversion to 4.092MHz by sub-sampling the IF signal at a sampling clock of 16.368MHz.
A PLL and a crystal oscillator are also provided. Reference frequencies of 16.367 MHz, as well as all frequencies commonly used in cell-phones are supported. The crystal oscillator may also be used as buffer for low amplitude TCXOs or may be disabled completely if desired.
An active antenna monitor is available as a support function for systems requiring active antennas, such as automotive applications. It provides power to the antenna, it is able to detect an open or a shorted active antenna and provides current limiting to protect both the antenna and the SY1006A from any damage. For the GRABEL application the antenna monitor circuit has been configured to provide 3V phantom power with a current limit of 25mA. The complete specification for the SY1006A can be found in RD1.

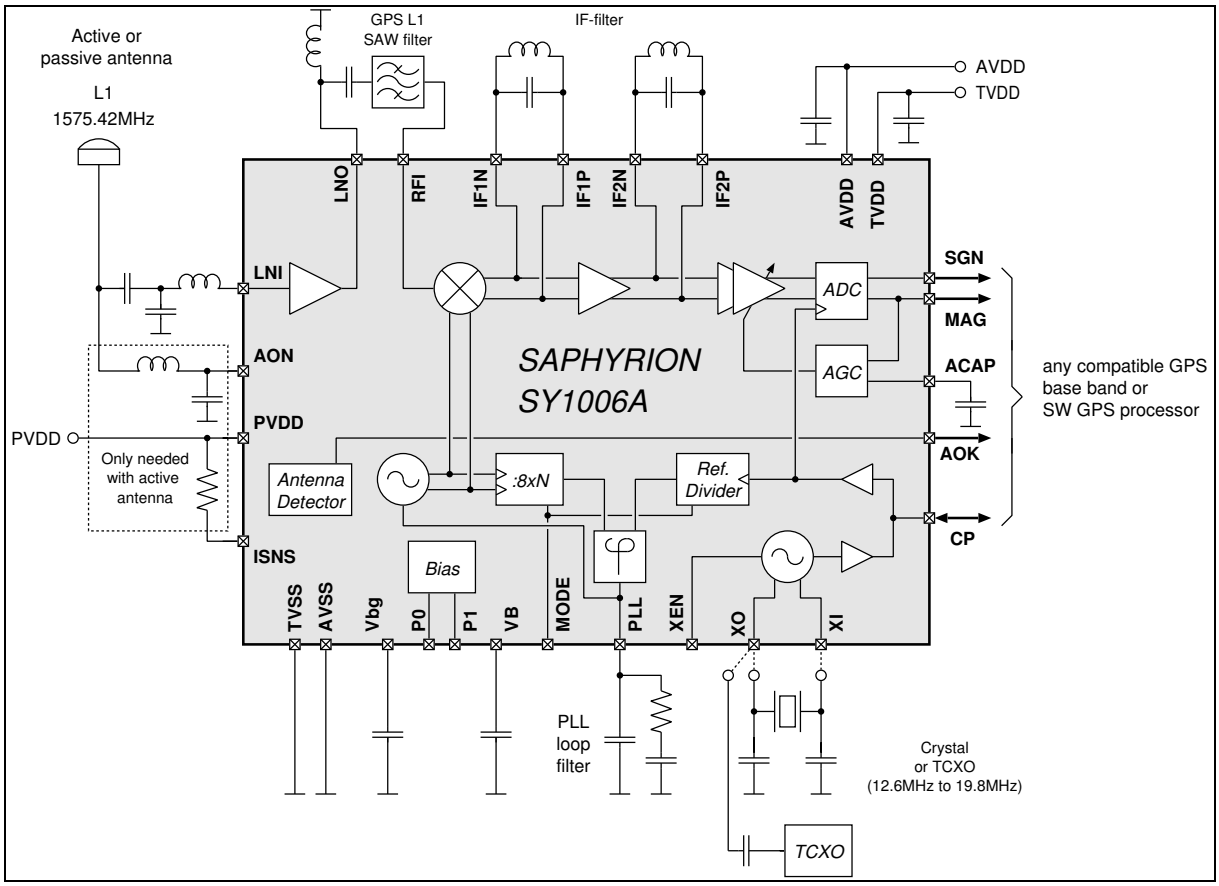

Figure 2.6: SY1006 RF front-end block diagram

2.4 Hexagonal Antenna Array

After evaluating several antenna array configurations, the hexagonal centred array came out as perhaps the best trade-off between size and performance. In particular its symmetry permits to generate beams whose shape is almost independent from their direction. In this configuration the central antenna is used as reference, while the six peripheral ones are adjusted in phase to generate the beams.
In order to get an hexagonal antenna array that is more stable and with better performance than the configurable SM103 allows, the prototype array shown in Figure 2.7 was constructed. This array consists of 7 patch antennas mounted on a solid copper ground plane.
The antenna type selected is again a standard patch antenna for GPS, and is manufactured by Inpaq (Ltd) Taiwan, under part number PA1575MZ5014G-XX-17. It is a square patch antenna, with RHCP polarization and a size of 25mm x 25mm x 4mm. Its gain is +5dBi at the zenith when mounted on a large ground plane (7cm x 7cm or bigger). This antenna type - which was tuned on a 7cm x 7cm ground plane – was already well centred when mounted on the hexagonal ground plane and did not require any particular tuning.

No LNA has been designed in this antenna array. The sufficiently short cables - about 50cm of RG174 cable with insertion loss of about 0.6dB – together with the good noise figure of the EB1006A allowed good performances without using any external LNA.

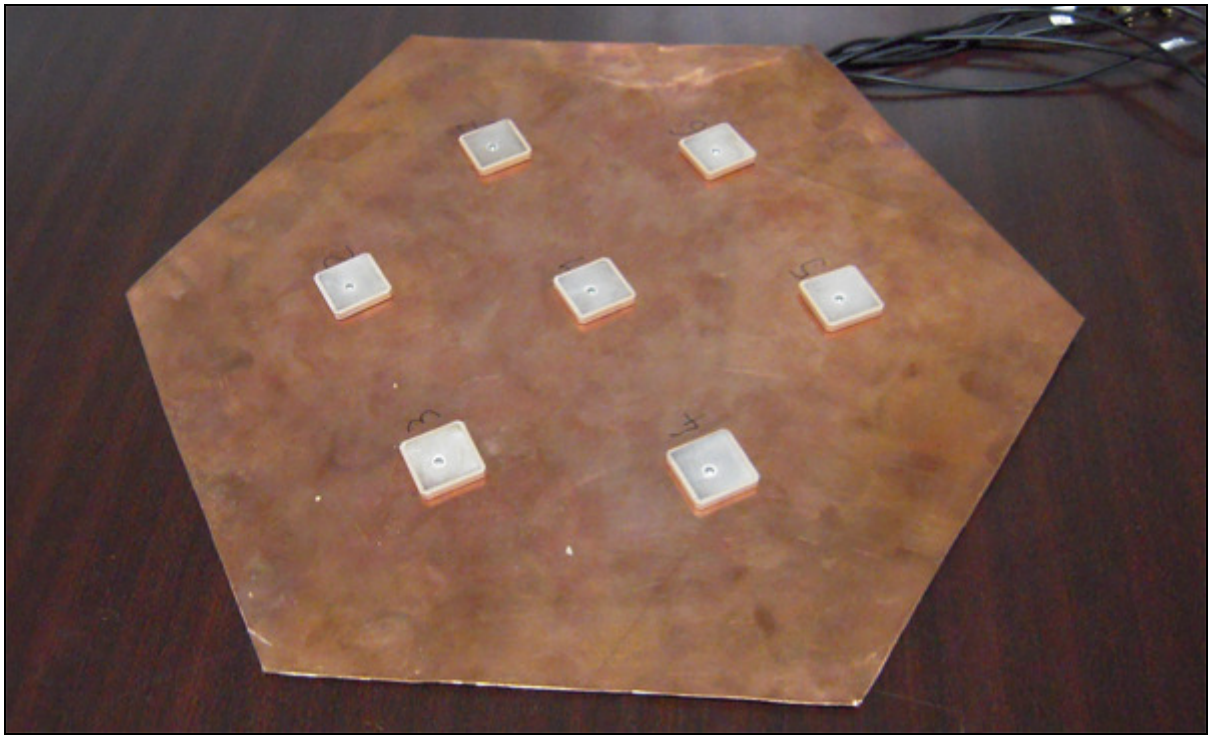

Figure 2.7: Antenna test board

3 Device interface

3.1 I2C protocol specifications

3.1.1 Device Address

Table 3.1: SM103 device address

Slave Address							
b7	b6	b5	b4	b3	b2	b1	**R/W# bit**
0	0	1	1	0	1	0	**R/W#**

3.1.2 Command byte

The command byte is the first byte to follow the address byte during a write transmission.

It is used as a pointer to determine which of the following registers will be written or read.

Table 3.2: SM103 internal registers

Command (Hex)	Register
0x11	Front-end 1 settings
0x12	Front-end 2 settings
0x13	Front-end 3 settings

0x14	Front-end 4 settings
0x15	Front-end 5 settings
0x16	Front-end 6 settings
0x17	Front-end 7 settings
0x18	Front-end 8 settings
0x19	Front-end 9 settings
0x30	Phantom Power and clock settings
0x50	Interrupt status register (source of the interrupt)
0x51	Interrupt enable register

3.1.3 Register 0x11 to 0x19: Front-end settings

This register reflects the settings of the front-ends.

- b1-b0:
  These bits reflect the P1 and P0 power state of the front-end. They can be read or written.
- b2:
  This bit shows if the front-end is physically present ('1' if present, '0' if not). It can only be read.
- b3:
  This bit reflects the antenna OK status ('1' if antenna OK, '0' if not). It can only be read. Antenna ok status is valid only when the front-end is fully active and present (P1-P0 states = '10', Presence = '1').
- b4:
  This bit select the write mode of the P states: if '1' the P1 and P0 states are saved in the EEPROM and the setting will be restored after the board is power cycled. If '0' the states are stored only in the volatile memory and the setting is lost when the board is powered off.

Table 3.3: Front-end settings

Front-end settings					
b7-5 (N/A)	b4 (-/W)	b3 (R/-)	b2 (R/-)	b1 (R/W)	b0 (R/W)
-	P states permanent	A=K	Presence	P1	P0

3.1.4 Register 0x30: Phantom Power and clock settings

This register reflects the settings of the phantom power and the clock status.

- b0:
  This bit reflects the Phantom Power setting ('1' if enabled, '0' if not). It can be read or written. The effective Phantom Power setting can be forced off with the JP1 jumper. In this case, even if the b0 is '1', the phantom power is off.
- b1:
  This bit reflects the clock status ('1' if the baseband clock is present, '0' if not). It can be only read.
- b4:
  This bit select the write mode of the Phantom power setting: if '1' the setting is saved in the EEPROM and will be restored after the board is power cycled. If '0' the setting is stored only in the volatile memory and the setting is lost when the board is powered off.

Table 3.4: Phantom power and clock

Phantom power and clock settings				
b7-5 (N/A)	b4 (R/-)	b3-2 (N/A)	b1 (R/-)	b0 (R/W)
-	Phantom Power Permanent	-	Clock Status: 1: present	Phantom Power Enable

3.1.5 Register 0x50: Interrupt status register

This register reflects the source of the interrupt request.

- b9-b0:
  When an event change the value of a register, the respective bit in the interrupt status register goes to '1'. For example if the “Antenna OK” status of the front-end 4 change, the bit 3 of the interrupt status register goes to one. The user can read the interrupt status register to know who as generated an interrupt and then read the updated register. The bit is reset to 0 when the respective register is read.

This register is always updated, even if the respective bit in the interrupt enable register is '0'.

Table 3.5: Interrupt status register

Interrupt status register										
b15-9 (N/A)	b9	b8 (R/-)	b7 (R/-)	b6 (R/-)	b5 (R/-)	b4 (R/-)	b3 (R/-)	b2 (R/-)	b1 (R/-)	b0 (R/-)
-	CLK (0x30)	F. E 9 (0x19)	F. E 8 (0x18)	F. E 7 (0x17)	F. E 6 (0x16)	F. E 5 (0x15)	F. E 4 (0x14)	F. E 3 (0x13)	F. E 2 (0x12)	F. E 1 (0x11)

3.1.6 Register 0x51: interrupt enable register

This register controls the events that enable the interrupt output pin.

- b9-b0:
  If the value is '1' , when the respective event occurs, the interrupt output pin goes to '1'. The interrupt output pin returns to '0' when all the active events enabled in the interrupt enable register are reset (by read the respective registers). The interrupt output pin can inform the user that in one of the enabled register at least one event is occurred.
- b15:
  This bit select the write mode of the Interrupts enabled bits (b9-b0): if '1' the settings are saved in the eeprom and they will be restored after the board is power cycled. If '0' the settings are stored only in the volatile memory and the settings are lost when the board is powered off.

Table 3.6: Interrupt enable register

Interrupt enable register											
b15 (-/W)	b14-9 (N/A)	b9 (R/W)	b8 (R/W)	b7 (R/W)	b6 (R/W)	b5 (R/W)	b4 (R/W)	b3 (R/W)	b2 (R/W)	b1 (R/W)	b0 (R/W)
Permanent	-	CLK (0x30)	F. E 9 (0x19)	F. E 8 (0x18)	F. E 7 (0x17)	F. E 6 (0x16)	F. E 5 (0x15)	F. E 4 (0x14)	F. E 3 (0x13)	F. E 2 (0x12)	F. E 1 (0x11)

3.2 I2C Bus transactions

3.2.1 Writing to the registers

Data is transmitted to the SM103 module by sending the device address and setting the least significant bit to a logic '0'. The command byte is sent after the address and determines which register will receive the data following the command byte.

The front-end registers (from 0x11 to 0x19) within the SM103 module are configured to operate together. After sending data to one register, the next data byte will be sent to the next register (see figure 3.1, in this example front-end register 4 and 5 are updated). After the data for the front-end 9 are written, the internal pointer returns to the front-end 1. There is no limitation on the number of data bytes sent in one write transmission. In this way, each 8-bit register may be updated independently of the other registers. If more data bytes are sent to the registers other than the front-end ones, the other bytes are simply ignored. 16 bits registers (register 0x50 and 0x51) must be written in two consecutive bytes with the LSB byte first.

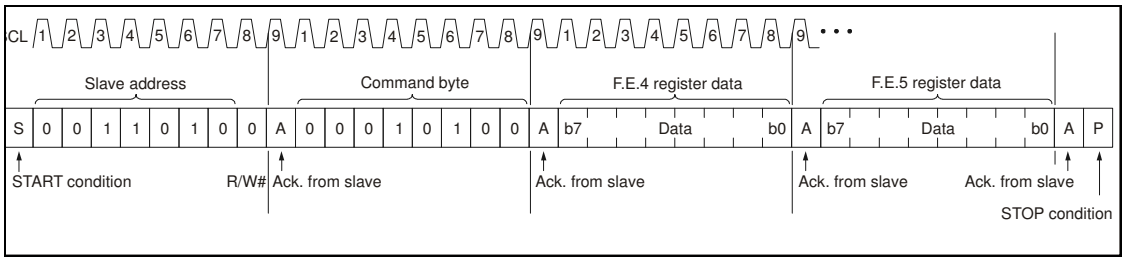

Figure 3.1: I2C write example

3.2.2 Reading the registers

In order to read data from the SM103 module, the bus master must first send the SM103 address with the least significant bit set to a logic ‘0’. The command byte is sent after the address and determines which register will be accessed. After a restart, the device address is sent again, but this time the least significant bit is set to a logic ‘1’. Data from the register defined by the command byte will then be sent by the SM103 module(see figure 3.2, in this example front-end register 4 to 'N' are read).

The front-end registers (from 0x11 to 0x19) within the SM103 module are configured to operate together. A pointer is automatically updated after the read of the current register.

After receiving data from one register, the next register data byte will be received. After the data for the front-end 9 are sent, the internal pointer return to the front-end 1.

There is no limitation on the number of data bytes received in one read transmission but the final byte received, the bus master must not acknowledge the data. If more data bytes are read from the registers other than the front-end ones, the other bytes are filled with '0'. 16 bits registers (register 0x50 and 0x51) are sent in two consecutive bytes with the LSB byte first.

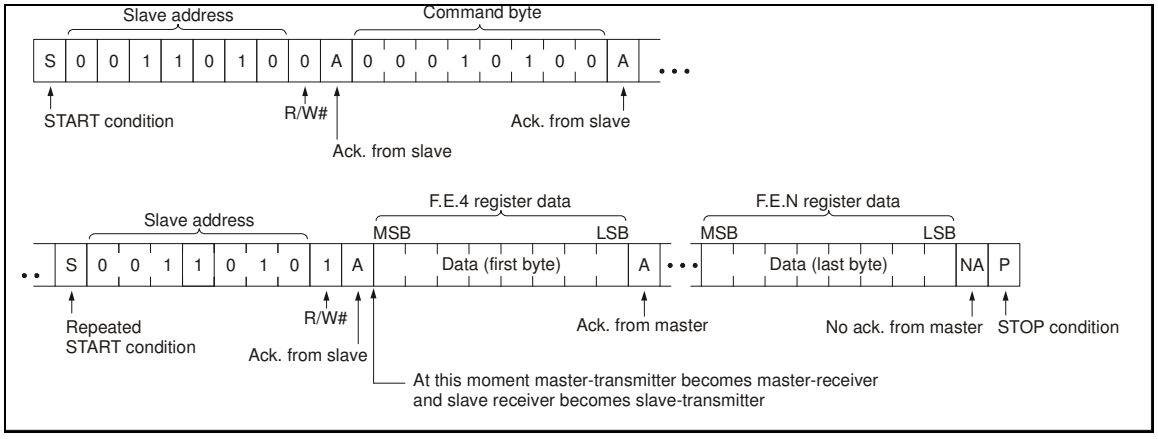

Figure 3.2: I2C read example

4 Reference Documents

Table 4.1: GRABEL reference documents

Ref.	Title	Doc.-ID	Version	Date
[RD1]	text	text	xx	21.04.2009
[RD2]				

5 Bibliography

Table 5.1: Bibliography

[Ref.Y]	Complete reference
[1]	NJ1006A datasheet, NemeriX S.A., rev 1.5, September 2005
[2]	

- End of document -