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GNSS Reconfigurable Antenna Based Enhanced Localization

FP7 GRABEL_232016 {REF RTD REG/T.4(2008)D/566378}

WP3: Baseband processing and Beamforming

D3.3: Efficient baseband Processing for GNSS Localization

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Abstract:

In this report we describe the beamforming capable GNSS base-band processor SY1031 developed and extended for the GRABEL project.

The SY1031BF is a 16 channel GNSS receiver written in VHDL and implemented on a Xilinx Virtex4 FPGA capable to generate and control up to 16 independent GNSS beams using up to 9 GPS L1 antenna inputs. The design has been based on Saphyrion's SY1031 GNSS processor.

Keyword list: ***GNSS receiver, base band processing, reconfigurable antenna, beamforming techniques***

Executive Summary

This deliverable presents the results of the development of a 16 channels, 9 antenna beamforming GPS L1 GNSS base-band processor for the GRABEL hardware platform.

The SY1031 GRABEL baseband processor is connected to the beamforming antenna through the RF front-end module and performs the beamforming signal combination generating 16 independent L1 IF GNSS streams connected to correlation channels.

The main functional blocks of the SY1031 are:

- an N antenna beamforming (phase control only) module,
- a 16 channel GNSS L1 correlation engine,
- a SPARC V8 32 bit CPU,
- the GNSS embedded SW to control the beamformer, the correlation engine and compute the receiver position.

The processor, written in VHDL, has been synthesized and tested on a Xilinx Virtex-4 FPGA.

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1 Introduction

1.1 GRABEL SY1031BF System Architecture

As already exposed in D2.3, the following activities represent the baseline for the task T3.3:

- Extend a pre-existing L1 GPS baseband processing unit to the GRABEL system.
- Implement the control of the beamforming antennas by adapting the GRABEL system's FPGA based baseband.
- Final evaluation of the integration activities realizing an extended baseband for the implementation of beamforming algorithms and the controls needed to manage the antenna array.
- Preparation of the selected and refined algorithms for their implementation into the GRABEL system prototype.
- Implement a message structure and a set of instructions to be used from the hosted application.
- Investigation of all the technological components of the activity for a first estimation of the system characteristics and performances (after completion of tasks T2 and T3.1 to T3.3).

In addition to the planned activities, coupling with a magnetometer to enable usage in dynamic mode turned out to be necessary.

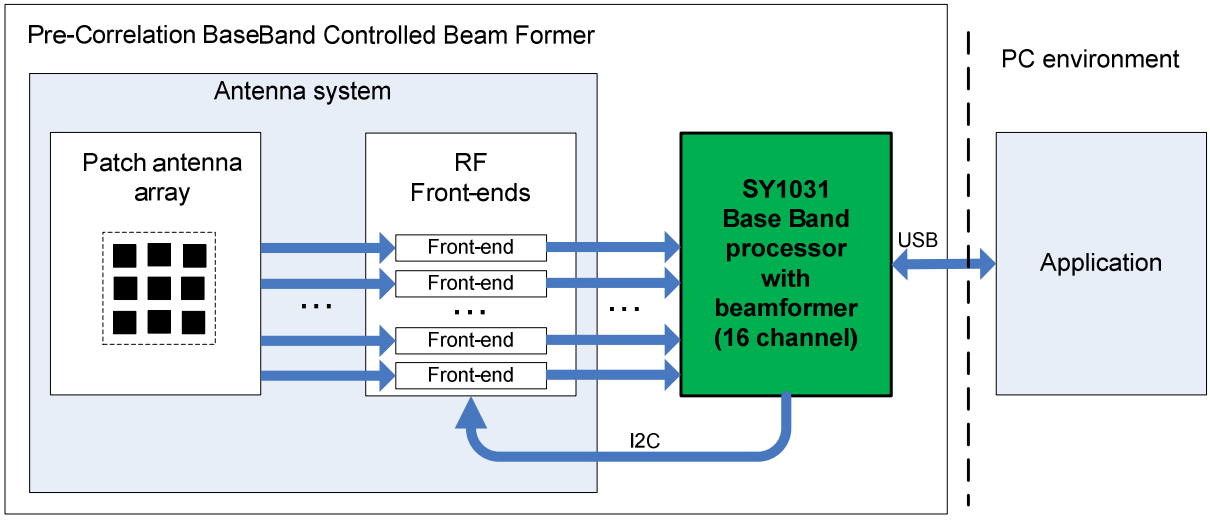

Figure 1.1: SY1031 System architecture

1.2 Pre-Existing SAPHYRION Baseband

During the past years, SAPHYRION designed a GPS L1 baseband processor, called SY1031, and implemented it on a FPGA.

The Saphyrion SY1031 IP is a GPS baseband processor targeting GPS/WAAS/EGNOS and Galileo L1 low power applications. It is based on the Saphyrion SP1016 GPS correlation core combined with a 32-bit IEEE1754 (Sparc V8) compatible CPU core, auxiliary on-chip memory, and peripherals. Flexible configuration of system performance and memory architecture allow the SY1031 to be used as a low power GPS receiver delivering formatted navigation information (NMEA protocol with Saphyrion extensions) or as a flexible GPS enabled microcontroller.

The GNSS correlation is carried out by the Saphyrion SP1016 correlator core, which is optimized for high efficiency and low power consunption. While supporting any GPS RF front-end device with 1 bit or 2 bit output, the SY1031 is optimized to work with the Saphyrion SY1006 RF front-ends. In particular the specific power management modes of the SY1006 are directly controlled. Flexible clocking schemes are implemented, making use of internal or external clock sources.

The CPU is a 32-bit RISC IEEE1754 (SPARC V8) compatible core with configurable 2...64 KB fast access (scratchpad) RAM, 8KB instruction cache and 1KB data cache. An on chip SRAM block of 2...64 KB is available

External memory and I/O space is accessed via a 32-bit external bus interface (EBI), which supports up to 4 banks of SRAM or Flash memory of 16MB each. One UART, an I2C master, plus optionally a master or slave SPI interface, a second UART and a general-purpose interface (GPIO) are available.

1.2.1 Features

- Fully configurable VHDL IP, stand-alone GPS baseband processor
- Low power architecture
- Scalable 16 channel low power correlation engine
- Scalable 9 channel beamforming front-end with up to 9x2-bit sign and magnitude GPS IF inputs
- WAAS/EGNOS support
- 32-bit, processor (Sparc V8 compatible)
- 64 kB of SRAM
- 64 kB fast-access RAM
- real time clock (no backup functionality for FPGA implementation)
- UART and a selectable UART/SPI/GPIO/I2C interface
- 32,16 or 8 bit external bus interface (EBI)

1.2.2 GPS Performance

All performance data refer to a SY1031 used with one single SY1006 RF front-end and external backed up RTC and NVRAM.

Table 1.1: GPS Performances

Item		Values		Conditions/Notes
Initial Acquisition Time		Average		Open-sky, 24hrs statistic, active antenna (signal range is between 30 to 49dB/Hz).
	Cold Start	46s		
	Warm Start	34s		
	Hot Start	5s		
Fix Time After Obscuration	Obscuration Time 1s to 100s	< 3s		Maximum Sensitivity -147dBm
Acquisition Sensitivity (fix not available)	TTFF [Hot] with all signals at –138dBm	30s		Simulator Test, all signals at specified power level.
	TTFF [Hot] with all signals at –141dBm	41s		
Acquisition Sensitivity (fix available)		–147dBm		Estimated.
Tracking Sensitivity		Better than –150dBm		Simulator Test, continuous fix with all signals at specified power level.
Static Accuracy	Static CEP 50	1.2m	0.8m (WAAS)	Open-sky, 24hrs statistic, active antenna (signal range is between 30 to 49dB/Hz).
	Static CEP 95	3.0m	2.0m (WAAS)	
	Static Altitude 50	1.3m	0.8m (WAAS)	
	Static Altitude 95	3.8m	3.0m (WAAS)	
Maximum Speed		515m/s		
Maximum Acceleration		2 g		
Maximum Altitude		18000m		

1.3 Beamformer Integration in the GNSS Hardware: Preliminary Study

A first analysis concerning the integration of the beamforming network in the GRABEL GPS base-band processor board has been taken into consideration.

The purpose of the accuracy improvement of the GRABEL receiver can be achieved reducing the antenna gain at low elevation angles (from which multipath signals and the strongest radio frequency interferences generally arrive) and/or increasing the antenna gain in the direction of the satellites. So the beamforming technique has to be used having this aim but, in order to be really effective, it should be applied in a satellite-by-satellite way. In other words it is necessary to implement as many beamforming networks as the satellite signals (to be received) are. So the idea is to integrate in the same baseband board a beamforming network for every tracking channel (16) that can work in parallel and independently. This means that 16 independent radiation patterns can be generated using a single antenna array, i.e. one for every tracked satellite.

The down-converted signals from the antenna array are fed to the beamformers and each beamforming network is connected to the correlation engine as shown in figure 1.2.

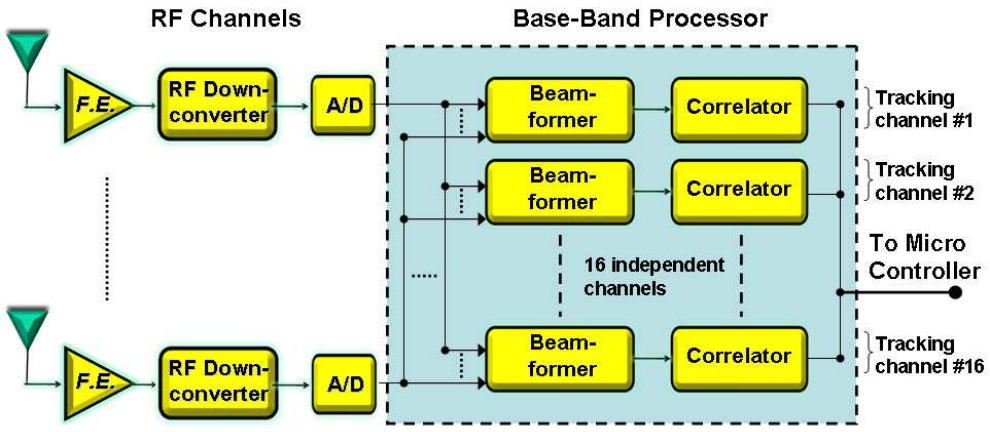

Figure 1.2: architecture of the GRABEL GPS Base-Band Processor

With this particular architecture it is therefore possible to have simultaneously:

- a single lobe towards the tracked satellite;
- a low radiation pattern at low elevation angles.

Since only a single lobe has to be generated by every beamformer, the complexity of the antenna array can be kept low.

MVDR beamforming algorithm requires the handling of matrices, even if with a small number of elements; therefore it is recommended that all the operations with matrices need to be processed in a dedicated beamforming Engine of the micro processor. Anyway the multiplications of the signals by the beamformer coefficients and the final sum can be conveniently managed by the FPGA device.

1.4 The GRABEL SY1031BF and SP1016BF

The baseband extension of the SY1031 developed in the frame of the GRABEL project is called SY1031BF and aims at the design and development, at FPGA and breadboarding level, of the proven technologies which are included in the SY1031.

SY1031BF and SP1016BF are extensions of SY1031 and SP1016 respectively, adding support for IF beamforming.

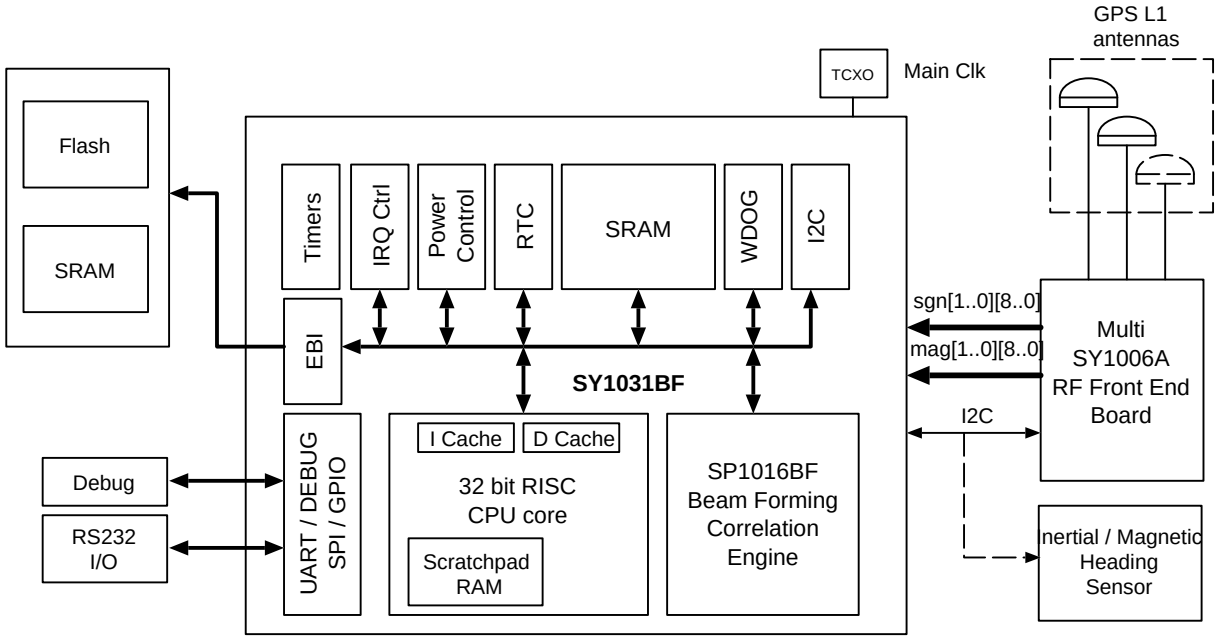

Figure 1.3: SY1031BF System architecture

2 Architectural Overview

This chapter briefly describes the main building blocks of the SY1031BF. A more detailed description of all blocks and their sub-blocks can be found in the following chapters. The on-chip SRAM content is cacheable (both instructions and data). This memory supports 8, 16 and 32bit access modes.

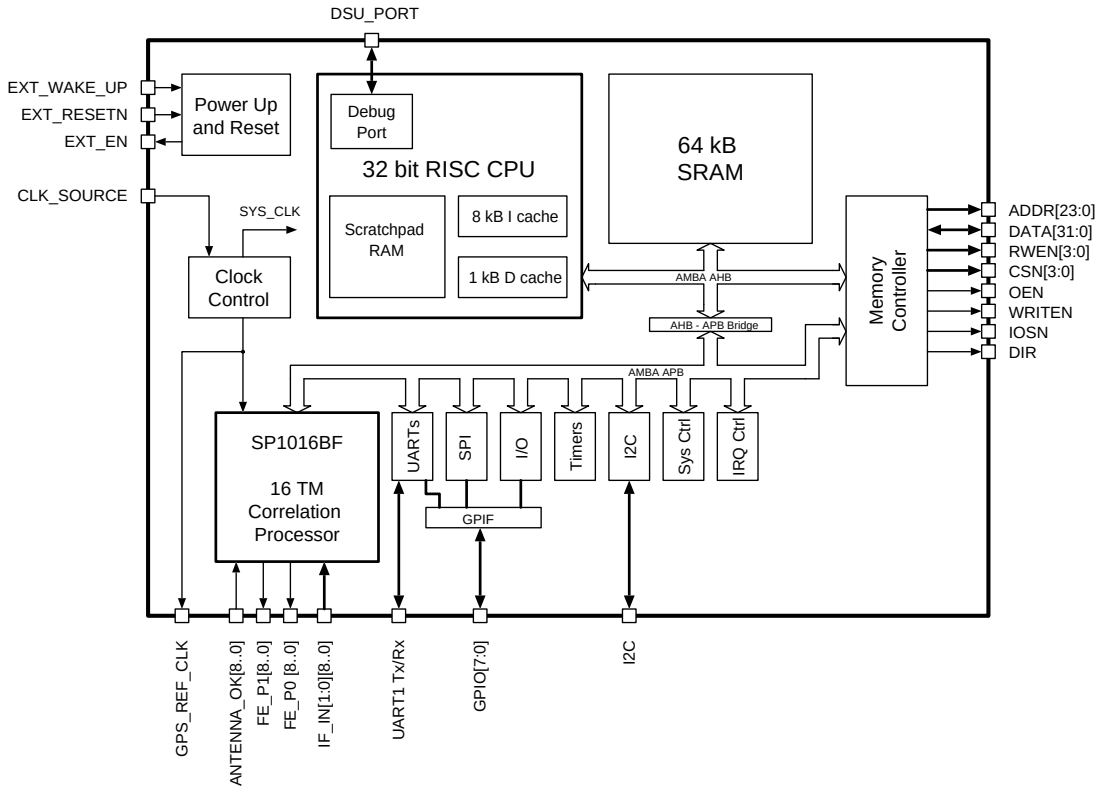

Figure 2.1: SY1031BF Block diagram

2.1 CPU

The SY1031BF CPU is a royalty free, 32bit RISC processor conforming to the IEEE_1754 (SPARC V8) architecture. It is designed for embedded applications and provides the following features:

- 5 stages pipelined architecture
- single cycle 32bit hardware multiplier
- barrel shifter
- radix 2 hardware divider
- 8 windows register file
- 8kBytes instruction cache, 1kBytes data cache
- 64kBytes scratch pad memory
- AMBA AHB and APB compatible interface
- Debug port (DSU)

More details can be found in the online Leon and SPARC V8 documentation available at http://www.gaisler.com. The Leon version implemented in the SY1031BF design is 1.0.16.

The scratch pad RAM is a block of 64kB memory dedicated to data that is directly connected to the CPU core at the same level as the D-Cache. As a consequence it has the quickest possible access time. At firmware build time, critical data structures can be assigned to the scratch pad RAM area.

2.2 On Chip SRAM

A block of 64kBytes 0-wait states SRAM is available on chip, on the fast AHB bus. This allows critical code portions as well as data structures to be stored. The on-chip SRAM content is cacheable (both instructions and data). This memory supports 8, 16 and 32 bit access mode.

2.3 External Bus Interface (EBI)

The EBI directly supports up to 4 banks of 16MBytes of asynchronous memory, with a fifth bank optionally accessible through signals of the GPIO interface. Each bank can individually be set to implement an 8, 16 or 32bit access mode with a selectable number of wait states.

When 16 or 32bit memory components are used in the system, the SY1031BF memory interface allows access to individual bytes by means of byte enable signals, typically provided by state of the art 16 or 32bit SRAMs.

2.4 Clocking

The main system clock is generated by a TCXO or, more in general, is an external digital clock source. This is the clock used for all the SY1031BF functions, excluding the GPS correlation that has a dedicated clock derived internally from the system clock (with a division factor from 1 to 8). This allows for flexible frequency plans to be implemented, with the possibility to trade off between the computational requirements of the application, the GPS frequency plan and the power consumption requirements.

2.5 GPS Correlation Unit

The GPS correlation function is carried out by the correlation unit which is a 16 tracking modules (64 correlators) implementation of the SP1016BF GPS correlator IP core. The SP1016BF is connected to the CPU as an AMBA APB peripheral. Two GPS interrupt signal (ACC_INT and MEAS_INT) are connected to the CPU interrupt controller. The correlation block is clocked by a dedicated clock (SP1016_GPS_CLK) signal derived from the main SYS_CLK, which can be deactivated when the GPS functionality is not needed by the system.

The correlation unit provides:

- 16 C/A-code acquisition and tracking modules (TMx)
- WAAS/EGNOS support
- 2bit sign and magnitude signal input
- Programmable interrupt interval and measurement rate
- Individual tracking-module activation
- Power management modes
- Direct control of the SY1006 RF front-end power management features

2.6 Other Peripherals

- **UARTs**: two serial interfaces are available. UART1 is always available on dedicated pins, while a second UART2 shares the pins of the GPIO interface. UART1 has a 16B receive and send FIFO, while UART 2 has a 4B send and receive FIFO. The UART1 lines can also be configured to act as DSU UART lines, allowing for flash re-programming reusing the buffer and connectors of UART1, without the need to access the dedicated DSU pins.
- **SPI**: both master and slave SPI interface alternatively are supported, by sharing the same pins of the GPIO interface. The SPI master supports up to 2 slaves. The slave has a send and receive buffer of 16 bytes.
- **Timers**: two 24bit timers are provided on-chip. The timers can work in periodic or one-shot mode. Both timers are clocked by a common 10bit prescaler.
- **Watchdog**: a 24bit watchdog is provided on-chip. The watchdog is clocked by the timer prescaler. When the watchdog reaches zero, an output signal (WDOG) is asserted. If enabled, this signal can be used to generate system reset.
- **Interrupt controller**: it manages a total of 15 interrupts, originating from internal and external sources. Each interrupt can be programmed with a two levels priority. Internal and external interrupt sources are used.
- **RTC**: a pseudo real time clock block with 1 second precision, 30bit wide register is implemented. It also offers a wake up functionality that can be used to recover the system from power down modes. The RTC has an on chip oscillator that uses a 32kHz quartz (On the FPGA implementation of SY1031BF the RTC timer is going to be lost if the FPGA power supply is interrupted).
- **I2C**: full featured and configurable I2C master.

2.7 GPIO Interface

An 8bit general purpose I/O interface allows for parallel I/O. This interface can be reconfigured in order to share some lines with other peripherals.

2.8 GPS IF Interface

This dedicated interface consist of 9x2bits input (sign and magnitude), 9x2 power mode control signals for the SY1006 RF front-ends, the GPS clock and an antenna ok input signals.

2.9 Power Modes

Beside fully active operation, where individual peripherals are clocked only depending on their activity, the SY1031BF supports clock-on-demand and SLEEP modes.

The SLEEP mode is entered by the CPU when a period of complete system inactivity can be expected. At this point the CPU can turn off the core power supply as well as other external components. Only a tiny portion of logic is kept powered and will reboot the system at the occurrence of a RTC wake up or an external wake up or reset.

The clock on demand option can be enabled individually for some of the clock sub-domains of the SY1031BF. When clock on demand is enabled, each block controls the gating of its own clock. One of the typical use of the clock on demand mode is for the CPU to stop it own clock, when no further processing is needed. When an interrupts from a peripheral occurs, then the CPU clock is switch on again, the interrupt is serviced and processing is resumed.

3 GPS Correlation Processor

The GPS correlation processor is an instantiation of the SP1016BF correlation processor with 16 tracking modules (TMs). It processes the digital IF signal delivered by the beamforming front-end, correlating it with replicas of the expected GPS signal and producing the measurements data that are used to compute the GPS receivers time and position. Moreover the unit generates two control signals (FE_P0_INT and FE_P1_INT) used to control the power management modes of the RF front-end. The correlation unit generates two interrupt signals (ACC_INT and MEAS_INT) that are available to the interrupt controller.

3.1 IF Interface

The signal path input is the two bit IF signal generated by the GPS RF front-end (SGN and MAG) with the coding described in the following table. If the RF front-ends are producing a one bit signal, then only the SGN bit is used, while the MAG input is tied-up.

Table 3.1: IF signal conversion

IF value	SGN	MAG
3	0	1
1	0	0
-1	1	0
-3	1	1

3.2 Clocking

The GPS correlation engine is clocked with two clocks: the SP1016_APB_CLK applied to the interface to the processor and SP1016_GPS_CLK that is a pulse deleted version of the SYS_CLK and is used for the GPS processing. The pulse deletion factor is the same as the clock division factor used to generate the external GPS reference clock for the RF front-end. In most of the portion clocked by SYS_CLK, the clock on demand option is available. If activated, this clocking option generates a clock pulse only when an access to the interface registers is executed by the CPU.

3.3 Beamformer

The SP1016BF implements a pre correlation beamforming digital front-end able to generate one composite IF stream obtained by mixing the IF stream from up to 9 RF front-ends for each of the 16 tracking channels.

The beamforming infrastructure allows control and configuration of the beamformer parameters, such as FE relative phase and data path scaling factor, independently for each tracking channel.

The main parameters for each beamformer are:

- FE On/Off: each beamformer channel (1 per tracking channel) can select which of the 9 RF front-ends to enable or disable. If a front-end input is disabled its data path is set to 0.
- FE Relative Phase: each front-end digital input is connected to a phase rotator which controls the relative phase between the different input streams of a channel beamformer
- To keep the user able to select whatever beamforming scheme, which includes a variable number of enabled digital front-end input streams and therefore a variable numerical range, a data path scaler has been added.

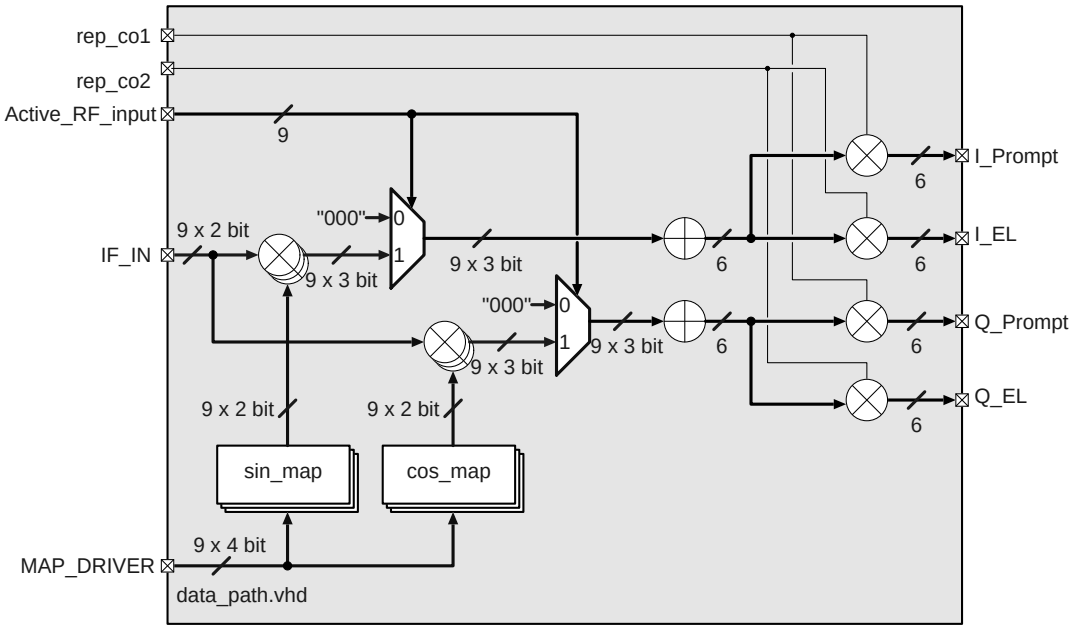

Figure 3.1: Data path block diagram

Each phase rotator consists of a multiplier and a sin/cos look-up table. The sin/cos tables have 1bit amplitude and 4bit phase quantization.

Table 3.2: Sin/cos map

input	Sin	binary	input	Cos	binary
0000	0	00	0000	1	01
0001	0	00	0001	1	01
0010	1	01	0010	1	01
0011	1	01	0011	0	00
0100	1	01	0100	0	00
0101	1	01	0101	0	00
0110	1	01	0110	-1	11
0111	0	00	0111	-1	11
1000	0	00	1000	-1	11
1001	0	00	1001	-1	11
1010	-1	11	1010	-1	11
1011	-1	11	1011	0	00
1100	-1	11	1100	0	00
1101	-1	11	1101	0	00
1110	-1	11	1110	1	01
1111	0	00	1111	1	01

The phase of each phase rotator has to be programmed into the dedicated registers in the per channel address space.

Table 3.3: Phase rotator multiplier output

IF Input	Sin /Cos	Decimal Carrier mixer output	Binary Signed Carrier mixer output
-3	0	0	000
-1	0	0	000
1	0	0	000
3	0	0	000
-3	1	-3	101
-1	1	-1	111
1	1	1	001
3	1	3	011
-3	-1	3	011
-1	-1	1	001
1	-1	-1	111
3	-1	-3	101

Since each beamforming stream can be the result of the combination of a variable number of different digital IF streams depending on the value in the ACTIVE_RF_INPUT register and considering the fixed numerical range of the whole correlation data path, a programmable scaler has been inserted between the 10bit pre accumulation and the 16bit correlation accumulator on each tracking channel.

Table 3.4: BF Scaler coding

Input	Scaling factor
“00”	1
“01”	2
“10”	4
“11”	8

The scaling factor for each channel is controlled by the SCALER register in the SP1016 channel address space.

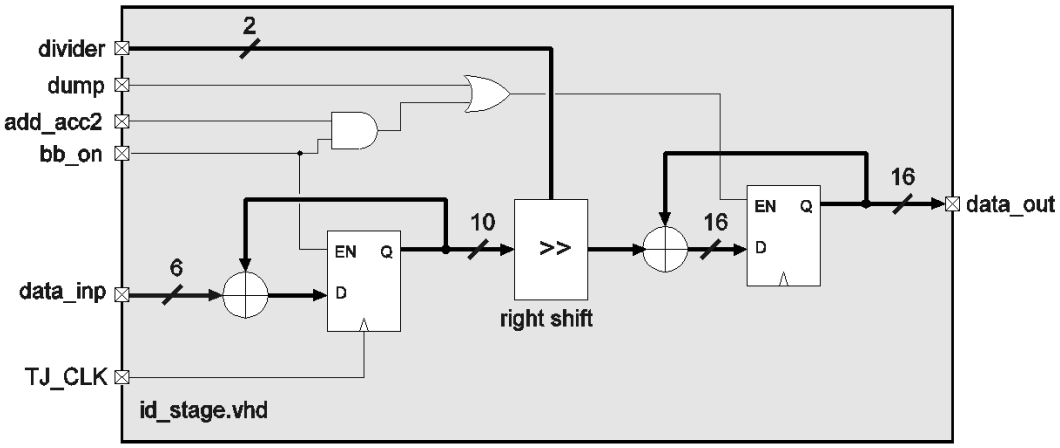

Figure 3.2: Block diagram of the id stage

3.4 Functional Behaviour

Starting from the IF signals, each tracking module can be assigned to acquire or track the signal from a selected space vehicle.

Each tracking module entails:

- A carrier NCO (numerically controlled oscillator) generating I and Q components.
- A code NCO feeding a C/A code generator that produces the C/A code corresponding to a given space vehicle and a version of the same code spaced by ½ code symbol (chip). The C/A code generator also offers the option to slew the C/A code generation by a programmable number of symbols.

The incoming IF signal is multiplied by the I and Q carrier components and by the two versions of the C/A code. The resulting 4 signal paths are continuously accumulated and the accumulated value is periodically dumped into 4 registers (INTEGR_Q_P, INTEGR_Q_EL, INTEGR_I_EL and INTEGR_I_P). These 4 values indicate the level of correlation between the locally generated signal and the one of the space vehicle that the TM has been assigned to.

Besides the correlation values, each TM generates a set of 5 measurements consisting of the code NCO phase, the carrier NCO phase, the carrier cycle count, the C/A code phase and the number of GPS epochs (1ms and 20ms epochs).

The GPS SW stack activates the necessary number of TMs, assigns them to space vehicles and does a C/A code and frequency scan in order to acquire the space vehicles signals. Once the space vehicle is acquired, the correlation values are monitored and the carrier and code NCO generators are continuously adjusted in order to track the acquired signal. By extracting GPS data from the tracked signals and computing pseudo ranges starting from the 5 measurements, the GPS SW can then compute position, velocity and time (PVT) of the receiver.

In order to operate the GPS SW has to continuously serve the ACC_INT interrupt, while it can set the MEAS_INT timing to a lower rate and poll the occurrence of this signal.

4 SW Implementation Notes

4.1 New Products Board and Platform Definitions

Starting from the NS1030 latest software release (4.0.15 production) a new set of products, board and platforms have been added:

- Platform SY1030.
- Board FPGA_SY1030.
- Product GRABEL_BEAMFORMER a standalone GPS receiver able to interface an antenna array for beamforming.

4.2 SY1031 Platform

The characteristics of the SY_1030A are:

- Hardware.
  - Scratchpad RAM 64kB.
  - AHB RAM 64kB.
  - Sin/cos map modified to 16 values map with -1, 0, 1 symbols (it was 8 values with -2, -1, 0, 1, 2 symbols).
  - A new set of registers to interface the channels.
- Software.
  - DSP code runs in the AHB RAM.
  - All the data (even in debug mode) in scratchpad RAM.

4.3 GRABEL Beamformer Product

Regarding the software, the main differences with respect to the baseline NS1030 SW 4.0.15 production are:

- Diagnostics messages X401, X402, X404 aligned to more recent versions of the post-processing tools (resp. $PSPYN1401, $PSPYN1402, $PSPYN1404,).
- SNR computation using the channel local best noise floor estimate (and not a fixed noise floor);
- It implements the beamforming algorithms. The beamforming software support can be enabled disabled simply by defining/undefining the macro __BEAMFORMING_SUPPORTED__ in the GRABEL / HOSTED MODE products configuration file “Configure.h”.

4.3.1 SY1031 Input/Output PSPYN Messages

This section briefly describes the new PSPYN Messages and lists or provides a link to the official message specification.

PSPYNNAV

This message reports the navigation solution data.

PSPYNESD

This message reports the extended satellite data, such as ECEF pos, velocity, etc.

PSPYNMCH

This message carries the information from the magnetic compass.

PSPYN901

This is a multiple format message: it is a bidirectional message used to send and get data from and to the beamformer, notify command acknowledgement or errors.

PSPYN1401 and **PSPYN1402**

PSPYN1401 is the new version of the X401 packet. Apart from the support for multiple constellations the main 1401 features are:

- Neat separation of DSP derived measurement/channel status from status reported by NAV software.
- In general the entire DSP Measurement structure is reported.
- Residuals / DSPCorrections / and Range Estimate Corrections (e.g. IONO/TROPO) all reported (no more compile time switch).
- Entire predictions structure reported.
- Reserved 32 bits words for debug purpose.

4.3.2 Message Specifications

Extended navigation data message

Frequency: 1 Hz

```
$PSPYNNAV, Time , MsgSetNum  , ConsecutiveFix , X,Y,Z, vX,vY,vZ, Lat, Lon, Alt, Heading, HSpeed, VSpeed, FixQuality, GDOP, PDOP, HDOP, VDOP, SvForFix, Bias, BiasRate
```

Time:	GPS time; to get the true GPS time just compute RecGPStime - mRecBias/LightSpeed
MsgSetNum:	incremental message numbering int
ConsecutiveFix:	number of consecutive fixes int
X,Y,Z:	receiver ECEF position m double
vX,vY,vZ:	receiver ECEF velocity m/s float

Lat: Latitude value of the user respect to the Nord. deg°float

Lon: Longitude value of the userrespect to the East. deg°float

Alt: Distance between user position and WGS 84 ellipsoid surface m float,

Heading: receiver GPS heading deg°float

HSpeed: receiver horizontal speed m/s float

VSpeed: receiver vertical speed m/s float

FixQuality: fix quality indicator hex char

gps.mGpsPos.GetOpMode()== KS_DOING_POS_FIX

```
enum EKF_STATUS {
        KS_NO_FIX_AVAILABLE                 = 0, // Operative Mode
        KS_APX_POSITION                     = 1,
        KS_DEAD_RECKONING                   = 2,
        KS_DOING_TRUE_2D_POS_FIX            = 3,
        KS_DOING_PSEUDO_2D_POS_FIX          = 4,
        KS_DOING_POS_FIX                    = 5,
        KS_DGPS_AIDING                      = BIT (3),
        KS_HIGH_COVAR                       = BIT (4),      // Fix Quality
        KS_HIGH_DOP                         = BIT (5),
        KS_INTTY_WARNING                    = BIT (6),
};
```

GDOP, PDOP, HDOP, VDOP: dilution of precision parameters float 1 dec

SvForFix: Satellites used for this fix hex 32

Bias: receiver time bias in m double

BiasRate: receiver time bias rate in m/s float

Extended satellite data message

Frequency: 1 Hz

$PSPYNESD, Time, MsgSetNum ,Num Msg, Msg Idx, PRN , CH, SNR, Az, El, BF_Az, BF_El, PseudoRange, RangeRate, RangeRessidual, RangeRate Ressidual, RangeAccy , RangeRateAccy BF_Steering , StatusBitMask, X,Y,Z, vX,vY,vZ

Time: GPS time of week (float; s)

MsgSetNum: msg set number. Incremental number increased by 1 every time a PSPYNESD set has been sent (int; 0…2^16-1)

Num Msg: number of PSPYNESD msg in the current msg set (int; 1…16)

Msg Idx: current msg index from 0 to 16 (1 per SV) (int; 0…15)

PRN: SV PRN (int; 1…32)

CH: Tracking channel on which the PRN is tracked (int; 0…15)

SNR: Signal to noise ratio in dB-Hz (int 0...99)

Az: Satellite Azimuth (float; deg)

El: Satellite Elevation (float; deg)

BF_Az: Beam Azimuth (float; deg)

BF_El: Beam Elevation (float; deg)

Pseudorange: as used by the navigation filter (Range) (double,m)

Range Rate: as used by the navigation filter (Doppler) (float, m/s)

Pseudorange Residual: intended as innovation used by the navigation filter (Propagated Range – Measured Range) (float,m)

Range Rate Residual: intended as innovation used by the navigation filter (Propagated RangeRate – Measured RangeRate) (float,m/s)

RangeAccy: estimated range accuracy (float,m)

RangeRateAccy: estimated range rate accuracy (float,m/s)

BF_Steering: On or Off (string “ON”/”OFF”)

StatusBitMask: bit field int HEX

```
Typedef struct {
        unsigned ValidRange                 :1;
        unsigned ValidDoppler               :1;
        unsigned ValidEphemeris             :1;
        unsigned BadRangeMeasurements       :1;
        unsigned BadRangeRateMeasurements   :1
}SStatusBitMask;
```

The bad flag are set using the internal integrity checks. SV which have valid Range, RangeRate and Ephemeris which have not been flagged as bad Range or RangeRate are used for fix. If ValidEphemeris is not set the SV position comes from almanac.

X,Y,Z: satellite ECEF pos at TOT (double,m)

vX,vY,vZ: satellite ECEF vel at TOT (float, m/s)

Magnetic compass heading message

Frequency: 1Hz

$PSPYNMCH, Time, SamplingPeriod, NumMeas, CompassMode, RawX0/H0 , RawY0/H1, RawX1/H2, RawY1/H3 , ,... , CalibrationStatus, GeoHeading

Time: GPS time of week at the last heading measurement (float; s)

NumMeas: Number of measurements in the H/Raw fields ([float, deg] if in “H” mode; int if in “R” mode)

SamplingPeriod: heading sampling period 1…5 Hz (int)

RawX0/H0, RawY0/H1,

RawX1/H2, RawY1/H3:

Contains raw compass data or the final computed heading from the compass; to be used when CompassMode “H” (char)

CalibrationStatus: string indicating the compass calibration status (usable when “FULL”) (string)

GeoHeading: 0 if the heading is the magnetic one (use only when “1”) (int)

PSPYN901 and PSPYN140x

For more information on those messages please consult the document SY1031 Adaptive Multi Beamformer Implementation Notes [RD15], page 26 for PSPYN901 and page 33 for PSPYN140x.

5 Reference Documents

Table 5.1: GRABEL reference documents

Ref.	Title	Doc.-ID	Version	Date
[RD1]	SY1031 Adaptive Multi-Beamformer Requirement & Specifications Document	SY1031AdaptiveMultiBeamformer Req&SpecDoc_Rev02.pdf	0.2	08.02.10
[RD2]	SY1031BF datasheet	SY1031BF-ds13.pdf	1.3	04.2005
[RD3]	SP1016 datasheet	SP1016DS-09.pdf	0.8	02.2003
[RD4]	I^2C Master Core Specification	I2C_spec.pdf	0.9	06.2003
[RD5]	SY1031 Hardware Description	SY1031_Design_HW_Rev1.0.pdf	1.0	15.02.2010
[RD6]	State of the Art and Technological Roadmaps	grabel_wp1_d1_1_r_p_v102.pdf	1.02	01.10.2009
[RD7]	Use cases and application scenarios	grabel_wp1_d1_2_r_p_v104.pdf	1.04	01.10.2009
[RD8]	Propagation environment study and implications	grabel_wp1_d1_3_r_p_v101.pdf	1.01	01.10.2009
[RD9]	Architecture and system specification	grabel_wp1_d1_4_r_p_v117.pdf	1.17	18.10.2009
[RD10]	Reconfigurable Antenna Design	grabel_wp2_d2_1_r_p_v110.pdf	1.10	31.05.2010
[RD11]	Interconnection to the Baseband Processing	grabel_wp2_d2_2_p_co_v013.pdf	1.3	02.09.2010
[RD12]	Final design and assembly of prototype	grabel_wp2_d2_3_p_co_v101.pdf	1.01	17.11.2010
[RD13]	Antenna array system based on classical GNSS antennas	grabel_wp3_d3_1_p_co_v111.pdf	1.11	10.08.2010
[RD14]	Beamforming algorithms for GNSS receivers	grabel_wp3_d3_2_p_co_v110.pdf	1.10	20.06.2010
[RD15]	SY1031 Adaptive Multi Beamformer Implementation Notes	SY1031AdaptiveMultiBeamformerImplementationNotes_Rev10.pdf	1.0	08.07.2010

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