Number	261
Publication Year	2023
Acceptance in OA@INAF	2023-02-09T16:16:28Z
Title	LRS: Acquisition system (setting and test)
Authors	COSENTINO, Rosario
Affiliation of first author	O.A. Catania
Handle	http://hdl.handle.net/20.500.12386/33360, https://doi.org/10.20371/INAF/TechRep/261

INAF Technical Report

Telescopio Nazionale Galileo

LRS: Acquisition system (setting and test)

Document version 1.1

TNG-TS-LRS-0003

Date: 27-03-2020

Author: Rosario Cosentino

Change Record

Issue/ Rev.	Date	Section/Page affected	Reason/Remarks
1.0	27/03/2020		First version
1.1	08/02/2023		General upgrade

Contents

1. Introduction

1.1.Scope

This document is intended to describe the migration between one CCD acquisition system to another. The original system, the LRS acquisition system, works from the year 2000 and is integrated in the TNG Instrument Control System (ICS) , the new one will be based on the **A**stronomical **R**esearch **C**ameras (ARC) controller and a new acquisition software system that has to be integrated in the TNG ICS [RD02].

At the beginning of this document, we will compare the different methods used by the two CCD controller to manage the scan and reading. We will describe the existing CCD waveforms, written with the waveform editor (skytech controller), the waveforms programmed with the assembler code (ARC controller) and the theoretical waveforms provided by e2v.

Following we will describe the results of the electronic tests of the clock sequences and finally we will show the results of the first tests with the CCD detector.

1.2. Additional information

No additional information, at the moment.

1.3. Contact information

Feedback on this document is encouraged. Please email to cosentino@tng.iac.es

1.4. Reference documents

[RD01]**CCD42-40 NIMO Back illuminated High Performances CCD Sensor Datasheet**

[RD02] **LRS: Implementation of ARC controller**

[RD03] **LRS – Software Requirements Specification**

2. The e2v 4240 CCD

In this paragraph are introduced some information about the e2v CCD 4240, that has been used for the programming/generation of the waveform sequences. More information and the characteristic of the e2v 4240 CCD can be found in [RD01].

DEVICE SCHEMATIC

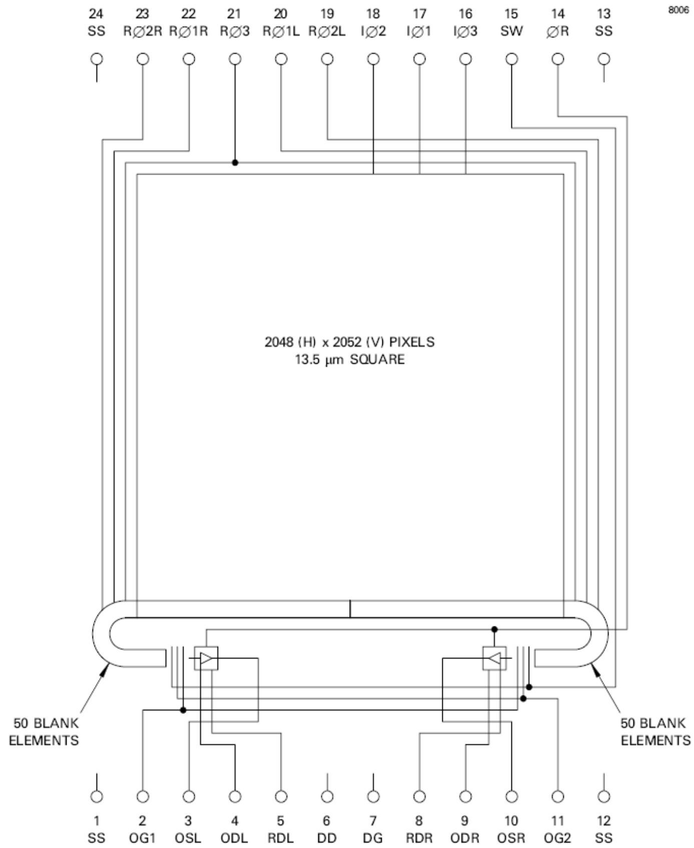

Figure 1 - Device Schematic

Table 1 - CCD Voltages

CONNECTIONS, TYPICAL VOLTAGES AND ABSOLUTE MAXIMUM RATINGS

PIN	REF	DESCRIPTION	CLOCK LOW Typical	CLOCK HIGH OR DC LEVEL (V) Min	Typical	Max	MAXIMUM RATINGS with respect to V_{SS}
1	SS	Substrate	n/a	0	9	10	-
2	OG1	Output gate 1	n/a	2	3	4	±20 V
3	OSL	Output transistor source (left)	n/a	see note 9			−0.3 to +25 V
4	ODL	Output drain (left)	n/a	27	29	31	−0.3 to +25 V
5	RDL	Reset drain (left)	n/a	15	17	19	−0.3 to +25 V
6	DD	Dump drain	n/a	22	24	26	−0.3 to +25 V
7	DG	Dump gate (see note 10)	0	-	12	15	±20 V
8	RDR	Reset drain (right)	n/a	15	17	19	−0.3 to +25 V
9	ODR	Output drain (right)	n/a	27	29	31	−0.3 to +25 V
10	OSR	Output transistor source (right)	n/a	see note 9			−0.3 to +25 V
11	OG2	Output gate 2 (see note 11)	4	16	20	24	±20 V
12	SS	Substrate	n/a	0	9	10	-
13	SS	Substrate	n/a	0	9	10	-
14	∅R	Reset gate	0	8	12	15	±20 V
15	SW	Summing well		Clock as R∅3			±20 V
16	I∅3	Image area clock, phase 3	0	8	10	15	±20 V
17	I∅1	Image area clock, phase 1	0	8	10	15	±20 V
18	I∅2	Image area clock, phase 2	0	8	10	15	±20 V
19	R∅2L	Register clock phase 2 (left)	1	8	11	15	±20 V
20	R∅1L	Register clock phase 1 (left)	1	8	11	15	±20 V
21	R∅3	Register clock phase 3	1	8	11	15	±20 V
22	R∅1R	Register clock phase 1 (right)	1	8	11	15	±20 V
23	R∅2R	Register clock phase 2 (right)	1	8	11	15	±20 V
24	SS	Substrate	n/a	0	9	10	-

If all voltages are set to the typical values, operation at or close to specification should be obtained. Some adjustment within the range specified may be required to optimize performance. Refer to the specific device test data if possible.

Maximum voltages between pairs of pins:

pin 3 (OSL) to pin 4 (ODL) . . . . +15 V

pin 9 (ODR) to pin 10 (OSR) . . . . +15 V

Maximum output transistor current. . 10 mA

NOTES

9. Not critical; OS = 3 to 5 V below OD typically. Connect to ground using a 3 to 5 mA current source or appropriate load resistor (typically 5 to 10 kO).

10. This gate is normally low. It should be pulsed high for charge dump.

11. OG2 = OG1 + 1 V for operation of the output in high responsivity, low noise mode. For operation at low responsivity, high signal, OG2 should be set high.

12. With the R1 connections shown, the device will operate through both outputs simultaneously. In order to operate from the left output only, R11(R) and R12(R) should be reversed.

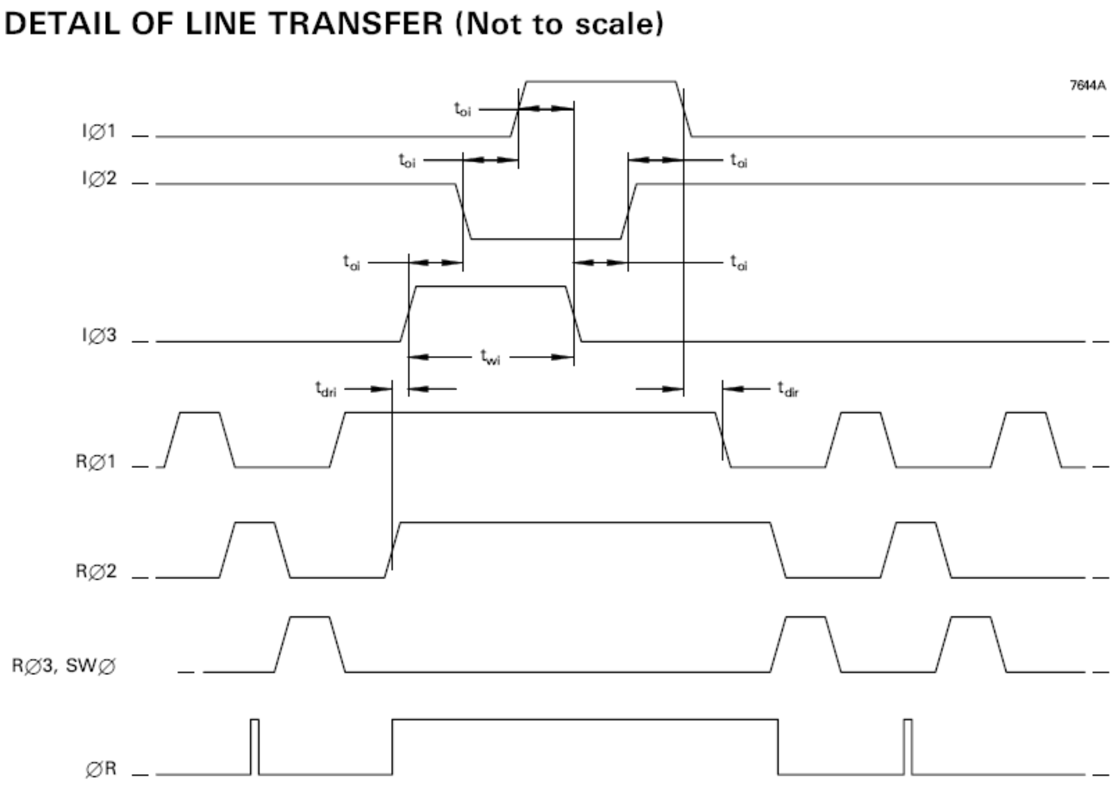

Figure 2 - Line Transfer

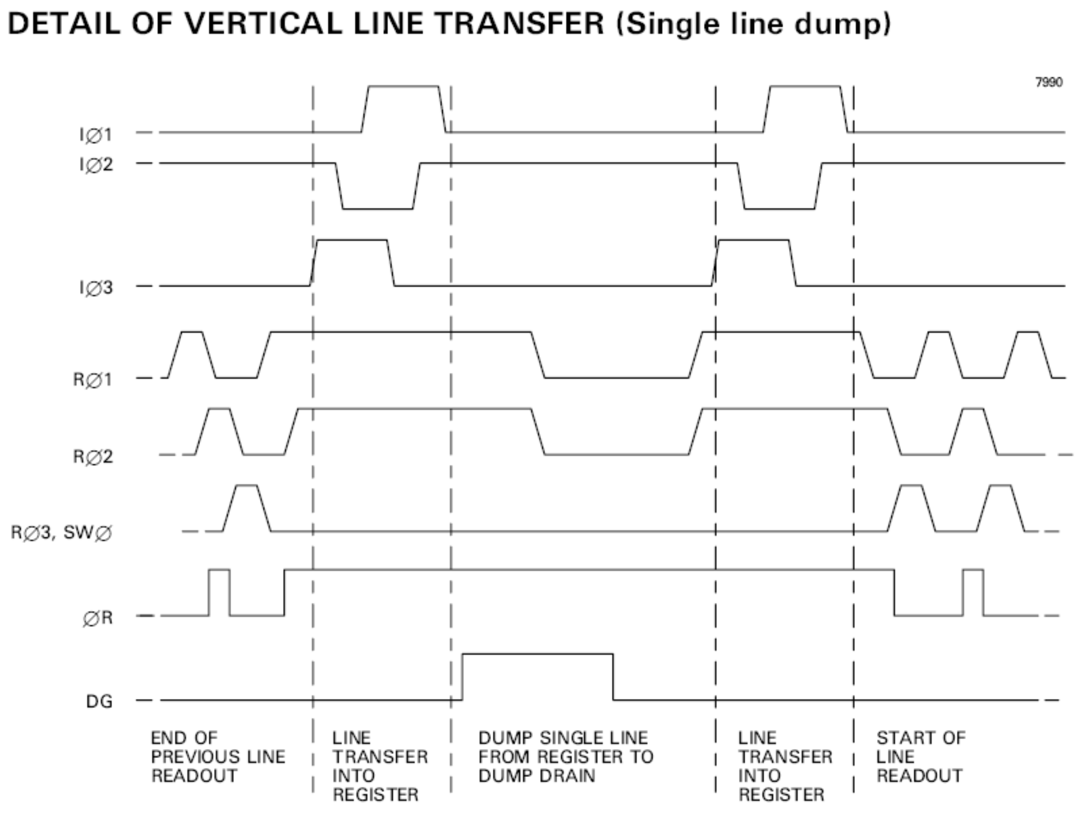

Figure 3 - Vertical Line Transfer

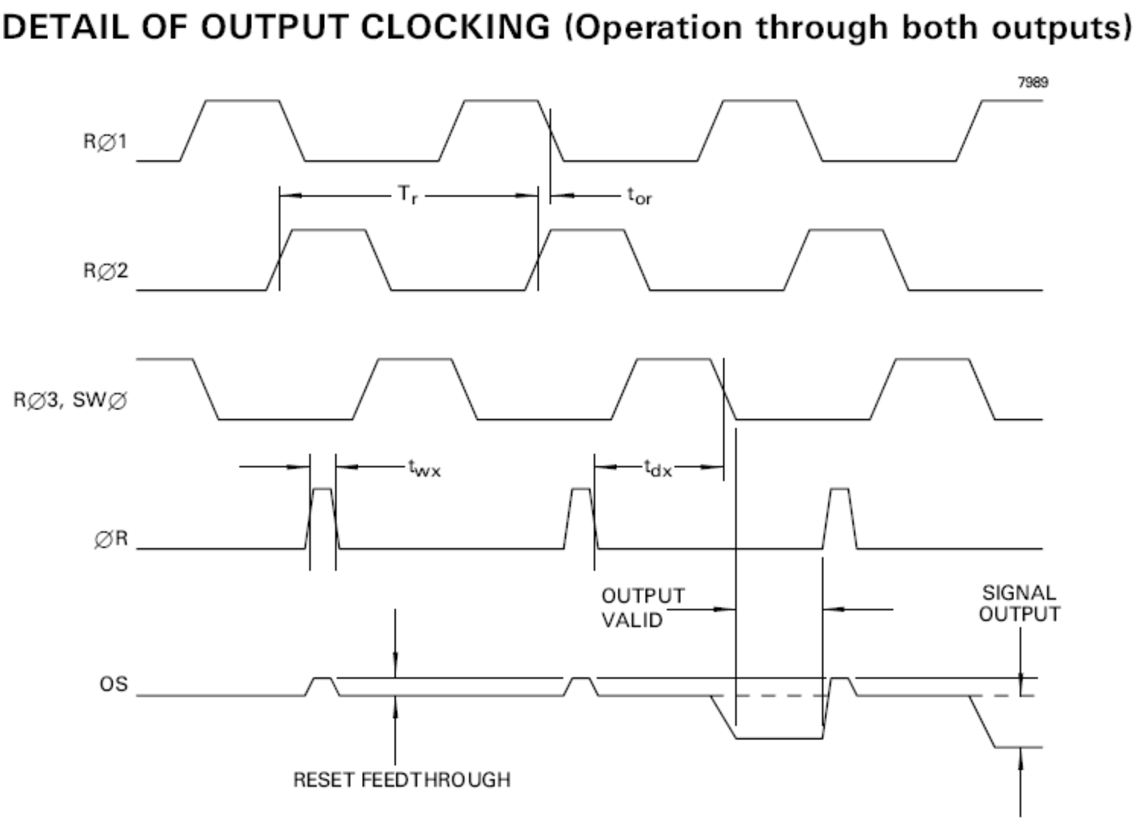

Figure 4 - Output Clocking (both output)

Table 2 - Clocking Timing

CLOCK TIMING REQUIREMENTS

Symbol	Description	Min	Typical	Max	
T_i	Image clock period	10	20	see note 13	µs
t_{wi}	Image clock pulse width	5	10	see note 13	µs
t_{ri}	Image clock pulse rise time (10 to 90%)	1	2	$0.2T_i$	µs
t_{fi}	Image clock pulse fall time (10 to 90%)	t_{ri}	t_{ri}	$0.2T_i$	µs
t_{oi}	Image clock pulse overlap	$(t_{ri}+t_{fi})/2$	2	$0.2T_i$	µs
t_{dir}	Delay time, IØ stop to RØ start	3	5	see note 13	µs
t_{dri}	Delay time, RØ stop to IØ start	1	2	see note 13	µs
T_r	Output register clock cycle period	300	see note 14	see note 13	ns
t_{rr}	Clock pulse rise time (10 to 90%)	50	$0.1T_r$	$0.3T_r$	ns
t_{fr}	Clock pulse fall time (10 to 90%)	t_{rr}	$0.1T_r$	$0.3T_r$	ns
t_{or}	Clock pulse overlap	20	$0.5t_{rr}$	$0.1T_r$	ns
t_{wx}	Reset pulse width	30	$0.1T_r$	$0.3T_r$	ns
t_{rx}, t_{fx}	Reset pulse rise and fall times	20	$0.5t_{rr}$	$0.1T_r$	ns
t_{dx}	Delay time, ØR low to RØ3 low	30	$0.5T_r$	$0.8T_r$	ns

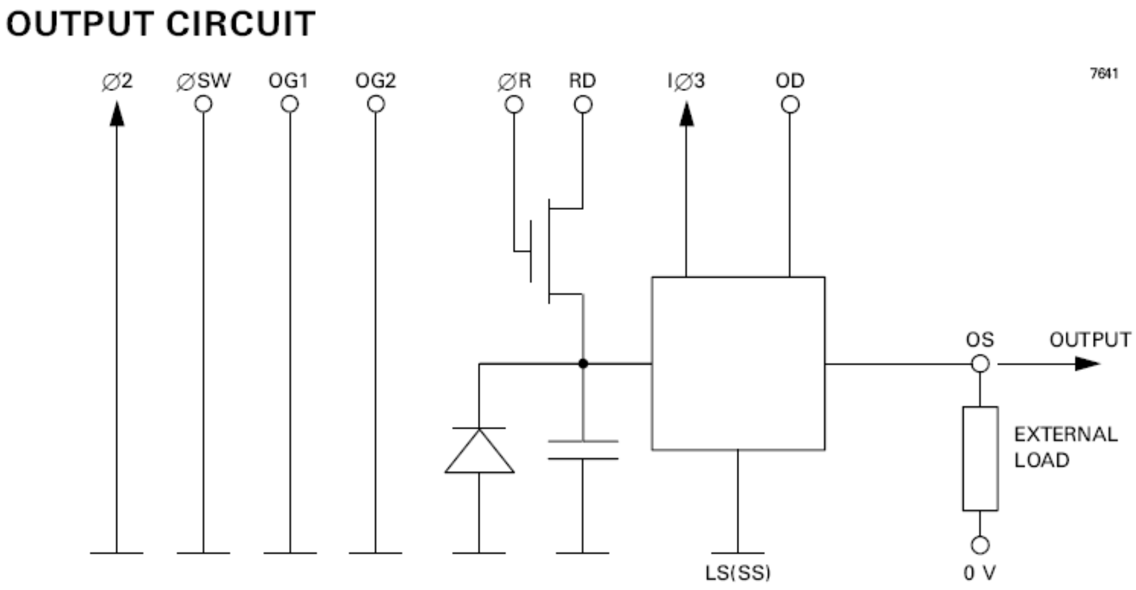

Figure 5 - Output Circuit

3. The Programmed Waveforms

The LRS CCD was used at TNG for a long time with the Skytech controller, and the waveforms was optimized to maximize the detector performances. The new ARC controller is provided with a template code, in assemble language, that has to be adapted to the CCD in use.

In this chapter are shown the different implementation of the waveform for both the acquisition systems.

3.1 The Waveform of the Skytech controller (WEditor)

The waveform shown in this paragraph was be used in the implementation of skytech CCD controller for LRS and was be programmed by using the Waveform Editor Program.

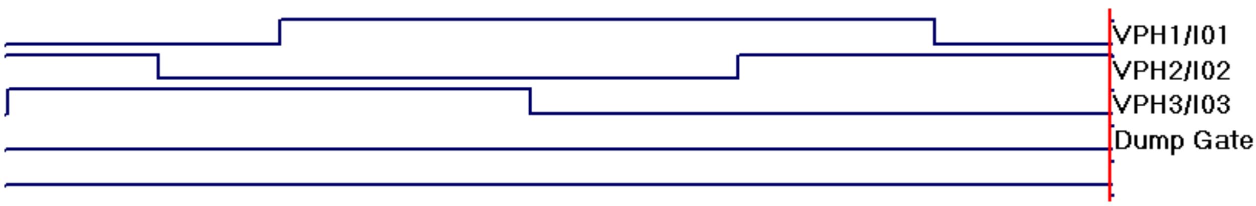

Figure 6 - Vertical phases (WE)

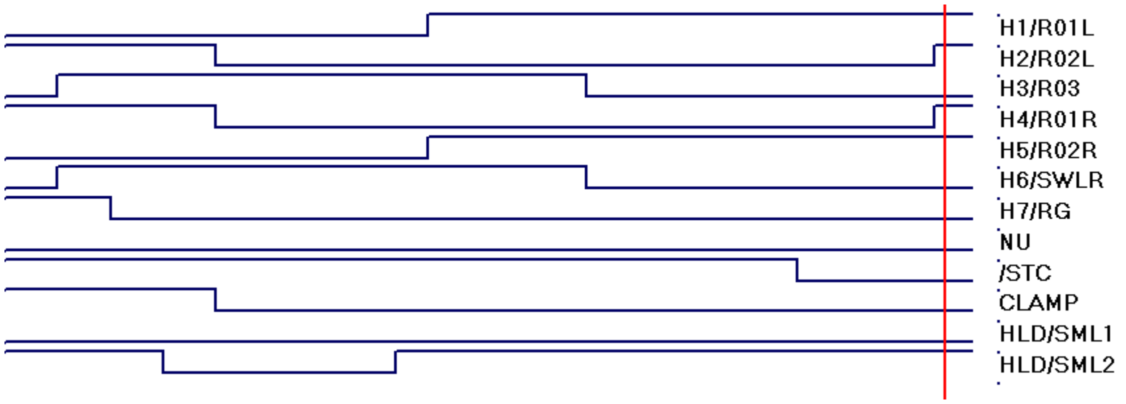

Figure 7 - Serial LR phases

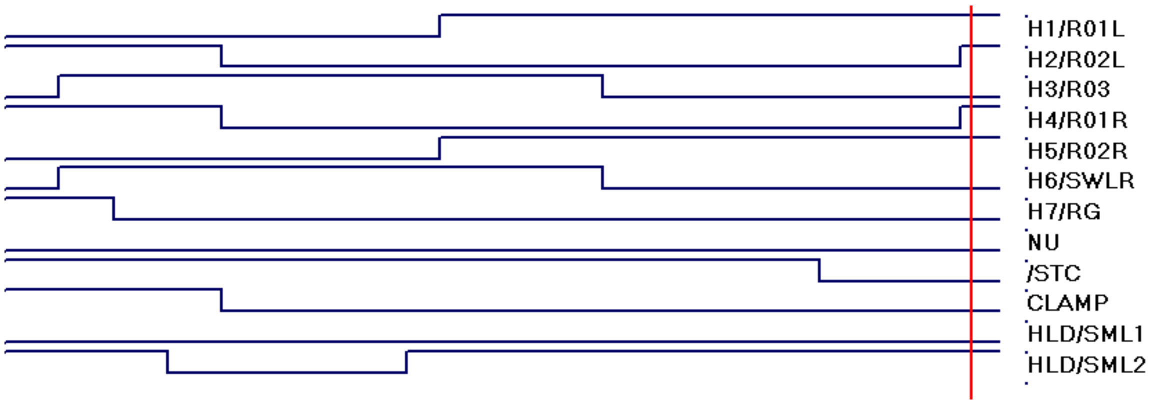

Figure 8 = Serial right phases

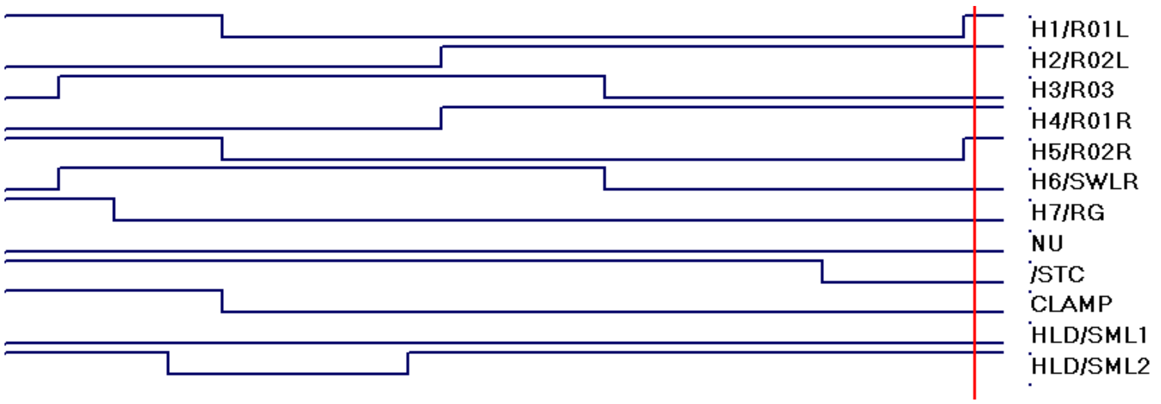

Figure 9 - Serial Right phases

3.2 The Waveform of the ARC controller (Assembler)

The waveforms for the ARC controller are generated by an assembler code and uses the Motorola 56000 DSP. An example of this code implementation of the sequences for the readout of the CCD in LR mode (readout from the two output of the CCD) is shown in the following figures.

```
; Parallel clocking UP by one line
PARALLEL_UP
    DC    END_PARALLEL_UP-PARALLEL_UP-1
    DC
    CLK2+RG+H1L+H1R+H2L+H2R+00+000+000+00
    DC    VIDEO+%0011000
    DC    CLK3+P_DELAY+I1+I2+00+00
    DC    CLK3+P_DELAY+I1+00+00+00
    DC    CLK3+P_DELAY+I1+00+I3+00
    DC    CLK3+P_DELAY+00+00+I3+00
    DC    CLK3+P_DELAY+00+I2+I3+00
    DC    CLK3+P_DELAY+00+I2+00+00
END_PARALLEL_UP
```

Figure 10 - Parallel clocking

```
SERIAL_READ_SPLIT_MED
    DC     END_SERIAL_READ_SPLIT_MED-SERIAL_READ_SPLIT_MED-1
    DC     CLK2+$030000+RG+000+H2L+000+H2R+00+CLP        ; Reset output node
    DC     CLK2+$000000+00+000+H2L+000+H2R+00+CLP
    DC     VIDEO+$010000+%1110100                        ; Reset integrator
SXMIT_SPLIT_MED
    DC     $00F000                                       ; SXMIT
    DC     VIDEO+$000000+%0010111                        ; Stop reset
    DC     VIDEO+$040000+%0000111                        ; Integrate
    DC     CLK2+$060000+00+000+H2L+000+H2R+H3+SW+CLP
    DC     CLK2+$0C0000+00+000+000+000+000+H3+SW
    DC     CLK2+$010000+00+H1L+000+H1R+000+H3+SW         ; Dump the charge
    DC     VIDEO+$000000+%0010111                        ; Stop Integrate
    DC     VIDEO+$000000+%0011011                        ; Change polarity
    DC     VIDEO+$040000+%0001011                        ; Integrate
    DC     CLK2+$060000+00+H1L+000+H1R+000+00+00
    DC     CLK2+$060000+00+H1L+000+H1R+000+00+00
    DC     CLK2+$070000+00+H1L+H2L+H1R+H2R+00+00
    DC     VIDEO+$000000+%0011011                        ; Stop Integrate
END_SERIAL_READ_SPLIT_MED
```

Figure 11 - Serial readout clocking (LR-Medium speed)

More readout more are implemented in the assembler code (Table 3) [RD03].

Table 3 - Readout modes implemented in the assembler code

Section Name	Mode	Speed	Microsec/pixel
SERIAL_READ_LEFT_SLOW	LEFT	SLOW	10
SERIAL_READ_LEFT_MED	LEFT	MED	2.5
SERIAL_READ_LEFT_FAST	LEFT	FAST	1
SERIAL_READ_RIGHT_SLOW	RIGHT	SLOW	10
SERIAL_READ_RIGHT_MED	RIGHT	MED	2.5
SERIAL_READ_RIGHT_FAST	RIGHT	FAST	1
SERIAL_READ_SPLIT_SLOW	SPLIT	SLOW	10
SERIAL_READ_SPLIT_MED	SPLIT	MED	2.5
SERIAL_READ_SPLIT_FAST	SPLIT	FAST	1

4. Test of the Waveform with the oscilloscope

To optimize the noise level of the clocks and minimize the crosstalk, the approach was the measurement of the signals in different point of the electronic chain and with different implementation (controller, clock board, cables). In the following paragraph will be described the configurations used and the results obtained.

4.1. Skytech controller with the clock board

In this test the configuration is:

- CCD controller Skytech
- Original LRS TNG clock cables
- Clock board

To simplify the analysis of the results we considered the readout mode that read the CCD from both output.

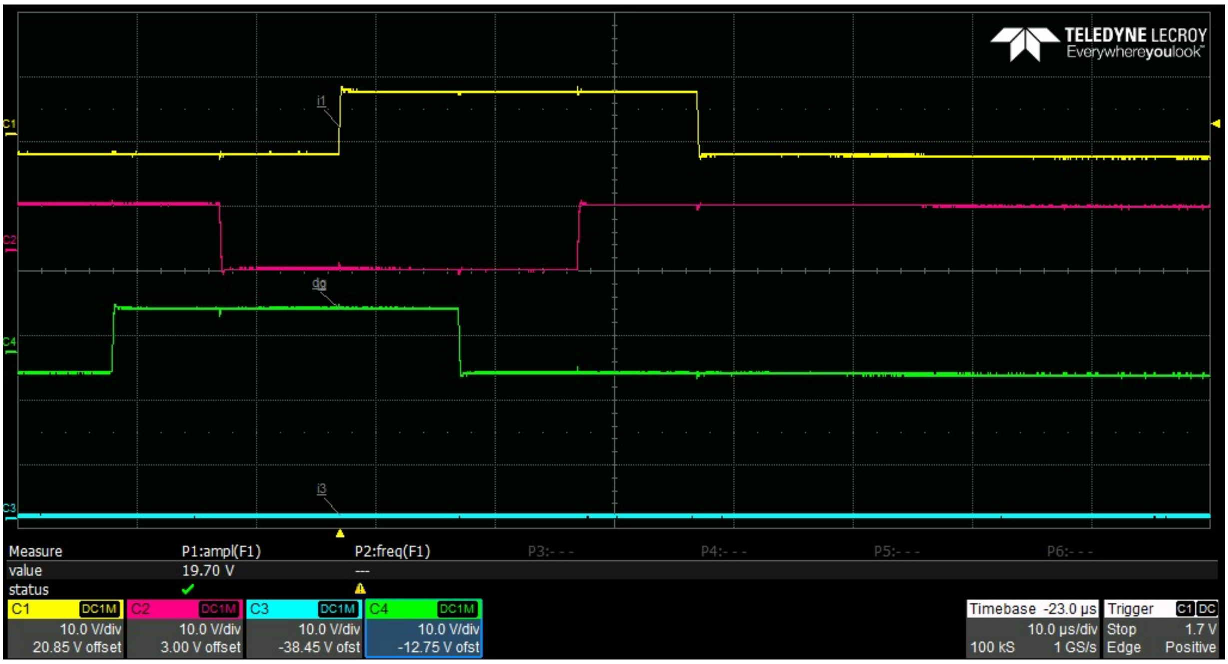

Figure 12 - Vertical waveforms

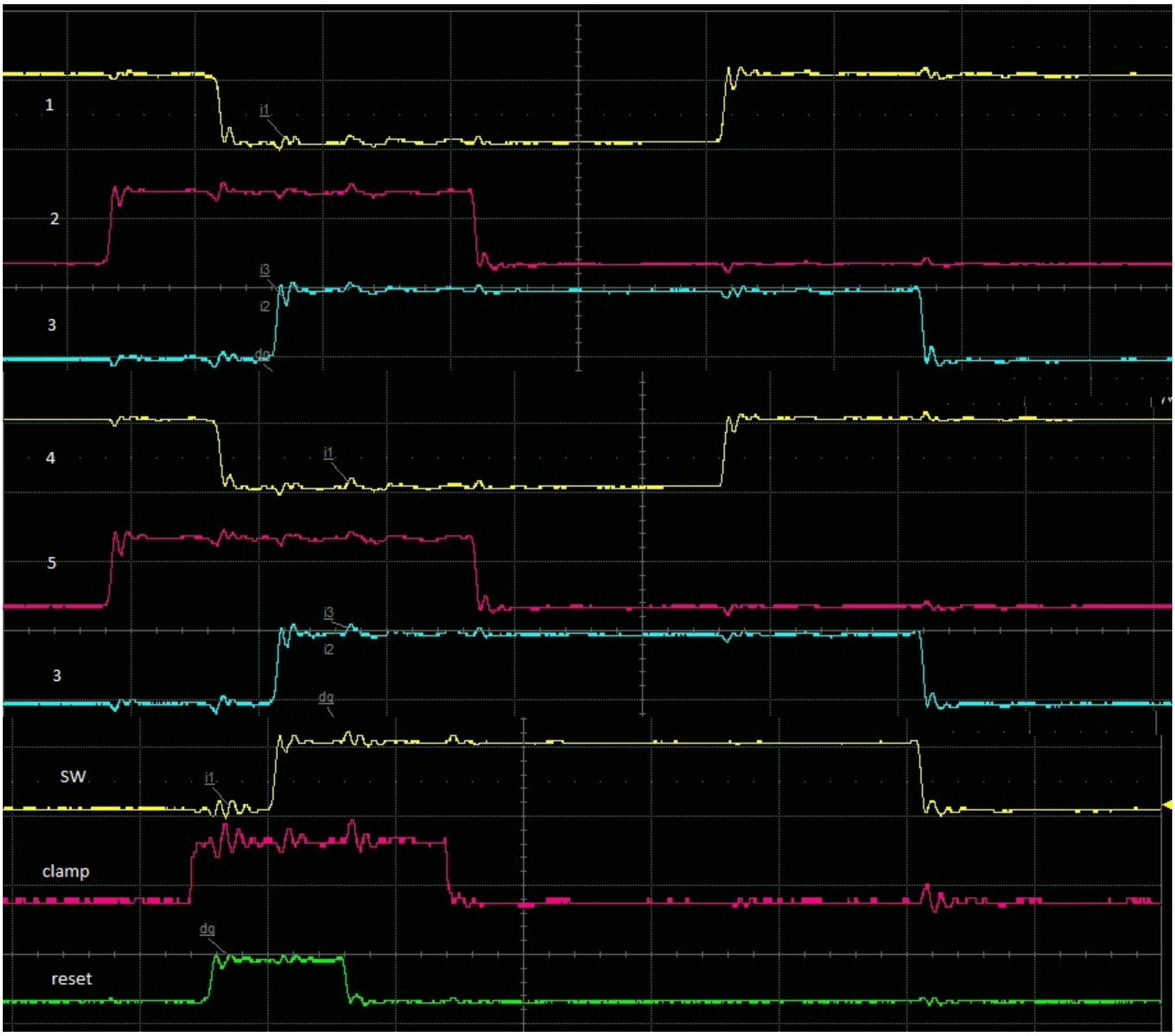

Figure 13 - Serial LR waveforms

4.2. ARC controller with the test board

In this test the configuration used is:

- CCD controller ARC
- Test board

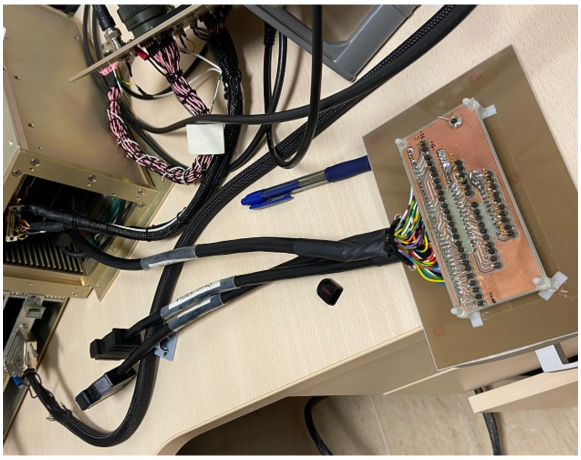

Figure 14 - ARC controller and Test Board

In this test we used the “E2VLRS.waveforms” assembler code. This version of DSP assembler code is described in [RD03].

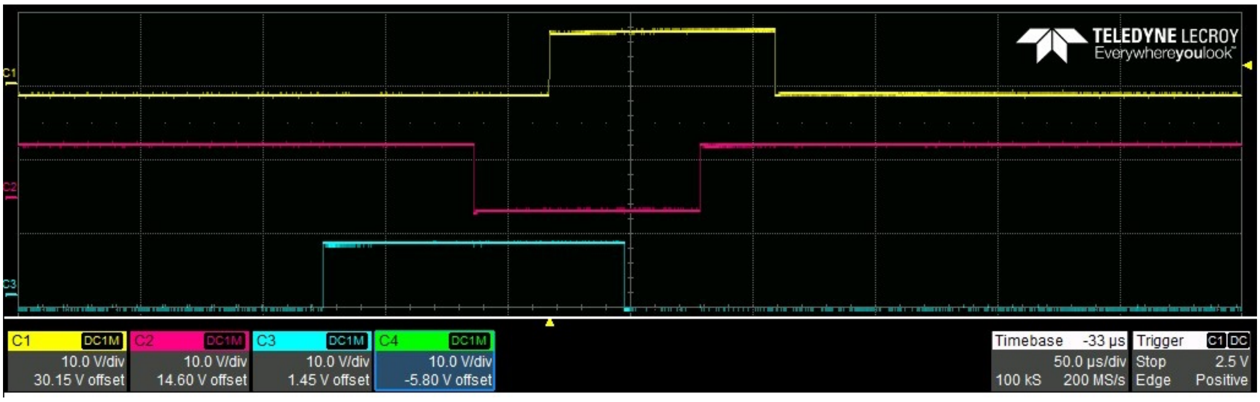

Figure 15 - Vertical waveforms

The serial RL waveforms have been analysed with different readout mode, to verify the degrading of the waveforms, depending on the readout speed. In the Fast-Mode test (Figure 16) a ‘simulated’ integration signal was added to have an idea of the processing operations.

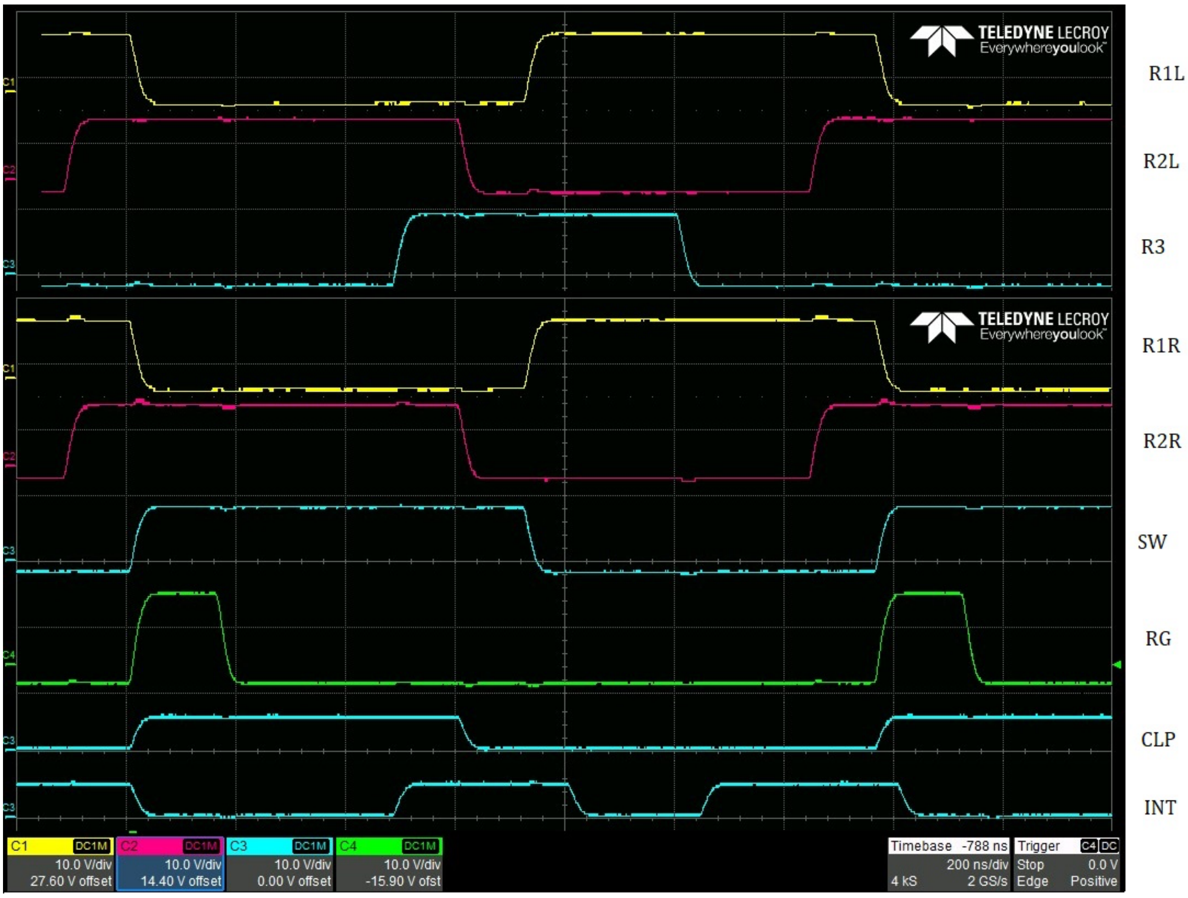

Figure 16 - Serial LR-FAST waveforms

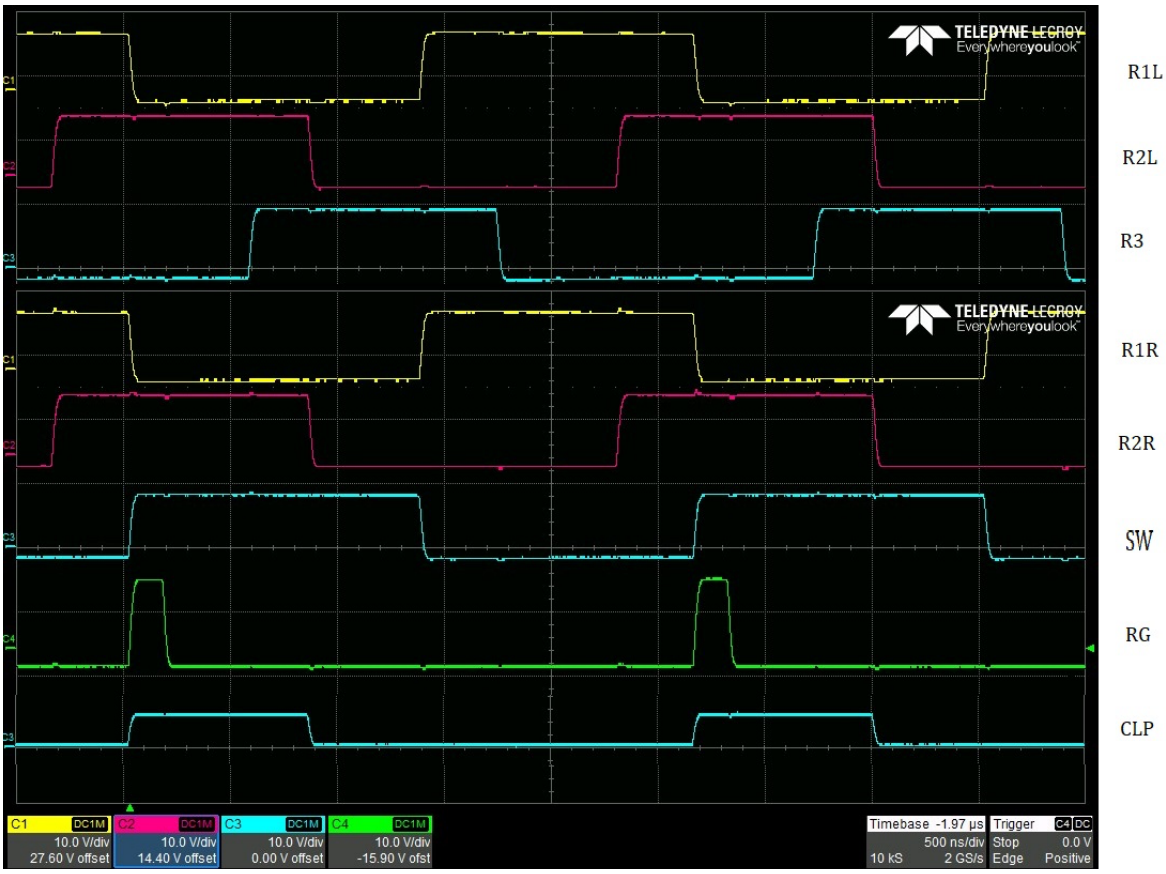

Figure 17 - Serial LR-Medium waveforms

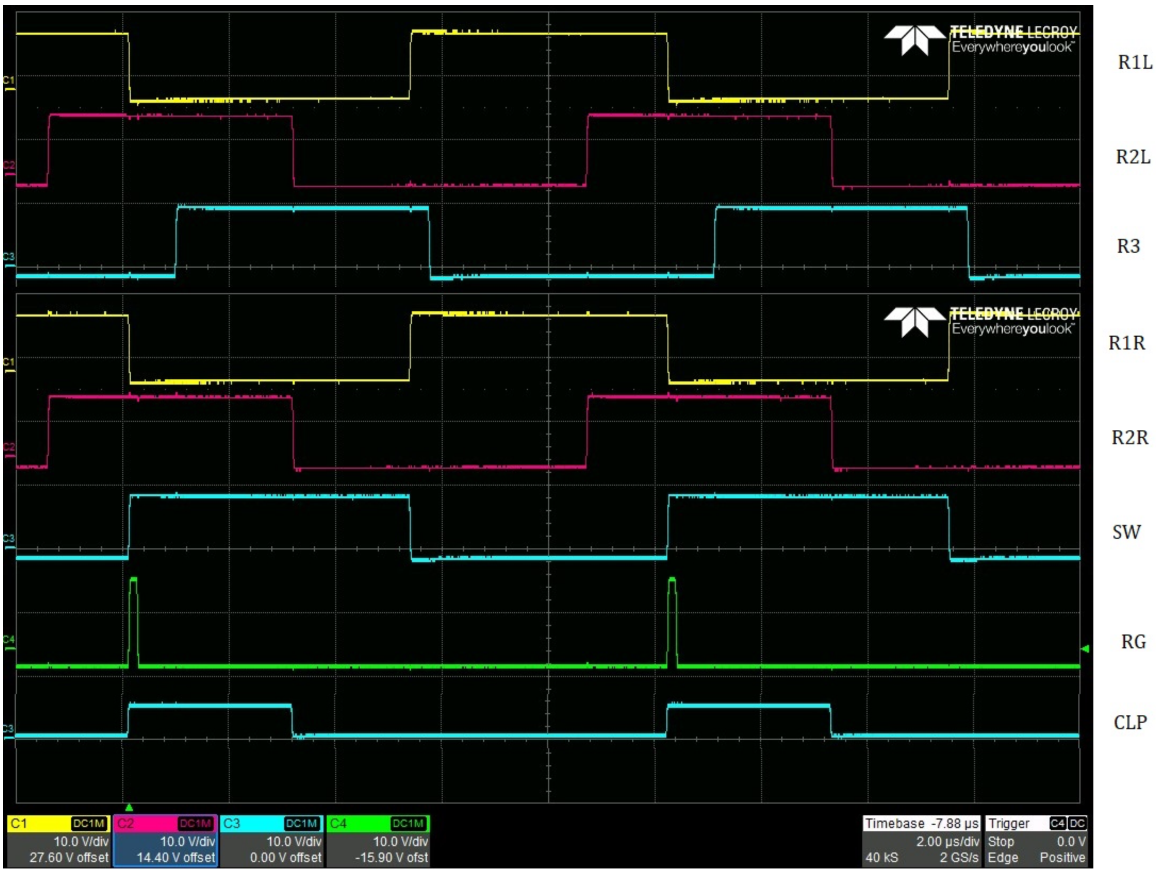

Figure 18 - Serial LR-Slow waveforms

The waveforms generated by the ARC controller are not degraded when the readout speed increases, the shapes of the clock signals don´t show significant differences at 1, 2.5 or 10 μsec/pixel readout speed.

4.3. ARC controller on the CCD board

4.3.1. Signal Measurement

These tests have been done with the real configuration for the CCD readout and taking the measure directly in the CCD socket:

- CCD controller ARC
- New custom clock cables
- New custom Video-Bias cable
- CCD Board (without CCD)

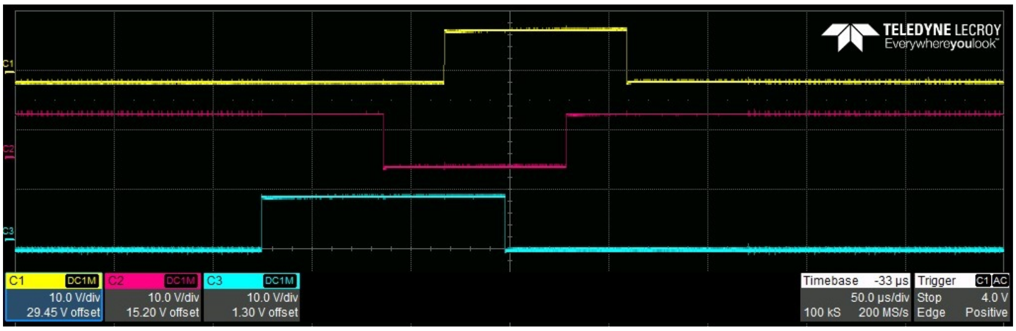

Figure 19 - Vertical Waveform

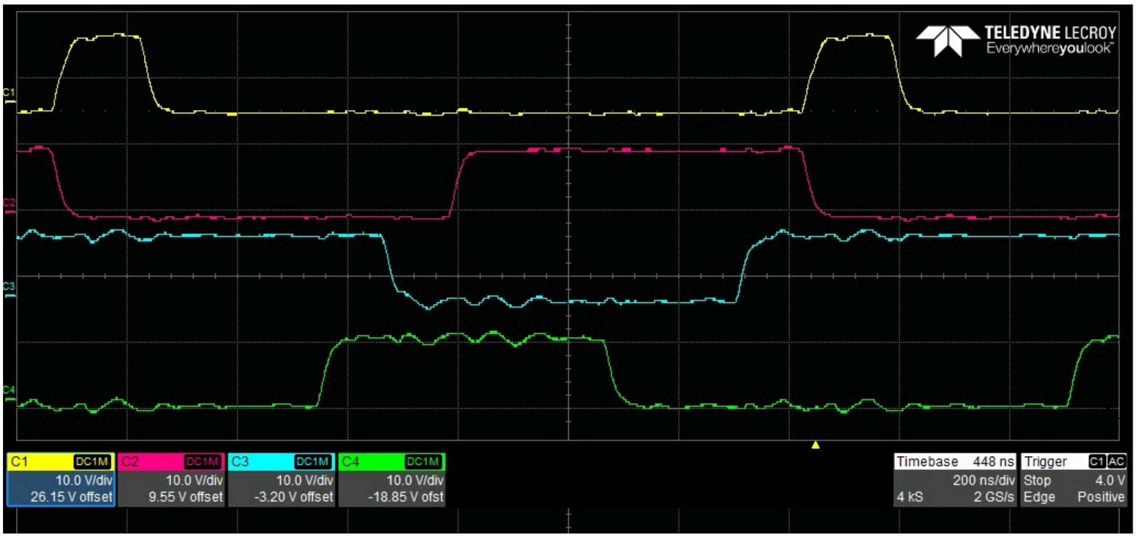

Figure 20 - Serial LR-FAST waveforms

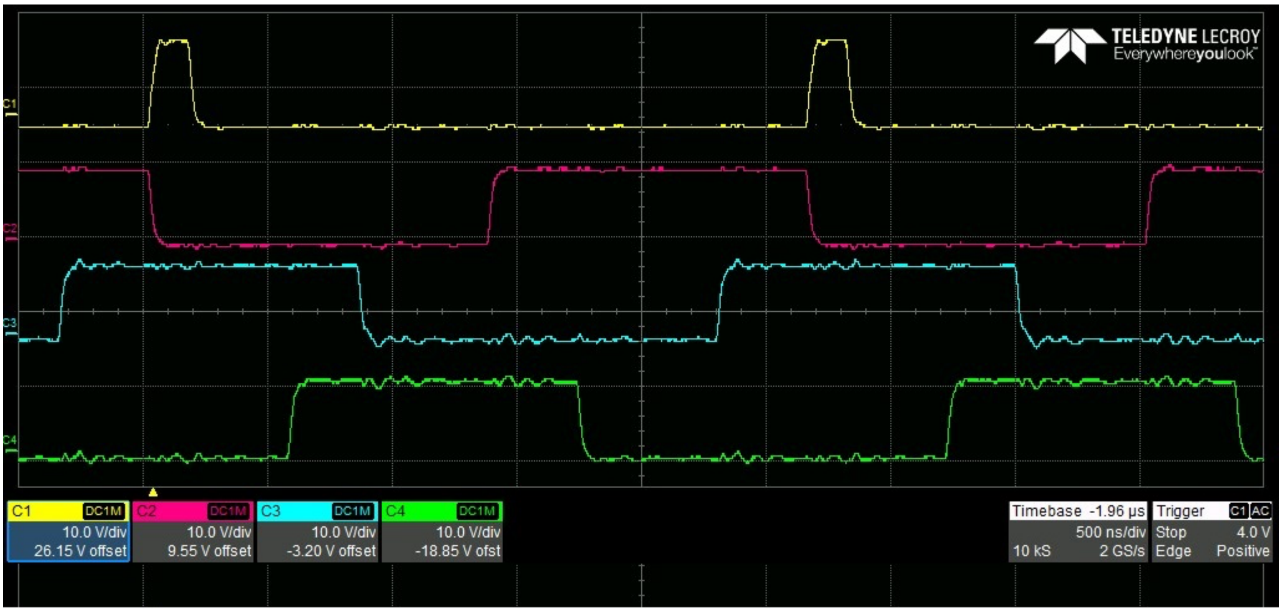

Figure 21 - Serial LR-MED waveforms

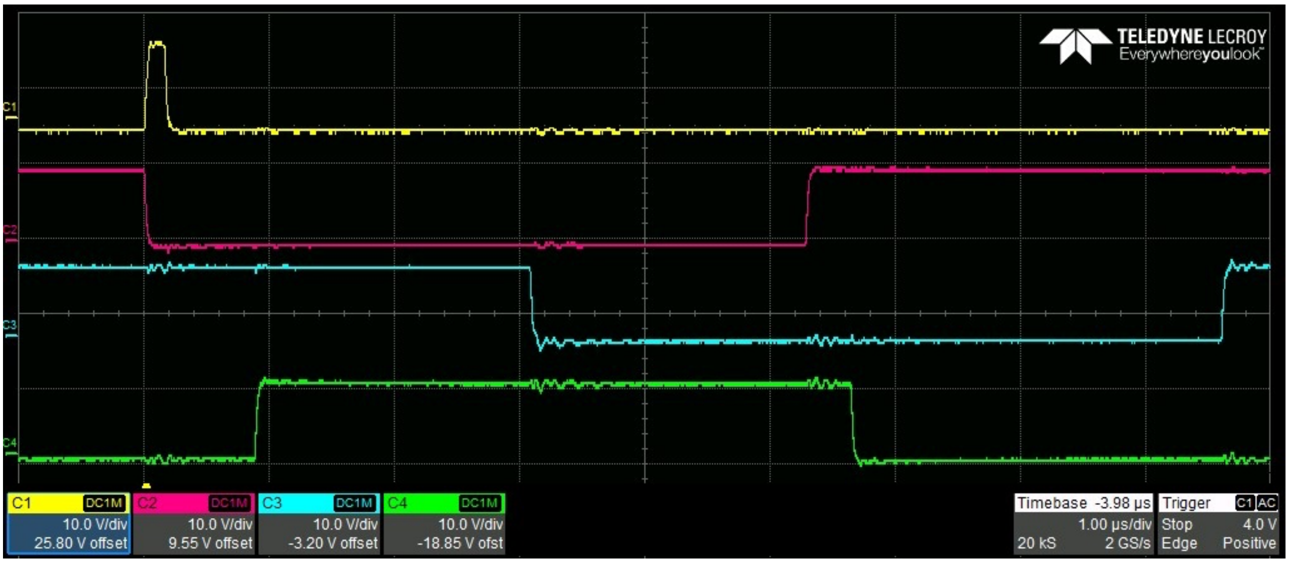

Figure 22 - Serial LR-SLOW waveforms

The clock signals generated by the ARC controller, measured in the CCD socket, are compliant with the specifications and the quality of them are compliant with the signals requested by the CCD.

4.4. CCD acquisition

After the test at CCD socket level, we are ready to test the e2v 42-40 CCD with the new acquisition system based on the ARC controller.

The following tests will be:

- The readout of the engineering CCD, mounted in a proto box
- The test of the scientific CCD at room temperature, mounted in the LRS dewar
- the test and characterization of the cooled scientific CCD, mounted in the LRS dewar

4.4.1. Engineering CCD at room temperature

These tests were done with an engineering CCD, mounted in a proto box, at room temperature. In this condition is possible verify if the acquisition system works as expected, because the CCD image has to show the overscan and the dark signal. We have adjusted the video offsets to obtain the wanted value of overscan pixels (considered as bias) and we acquired three images, one for each readout speed.

The acquired images show that the dark signal increases with a gradient trend that depends by readout time of the CCD image (with the SLOW readout mode the dark current reach the saturation of the image in the upper part of the CCD).

Configuration:

- ARC controller with video-bias and Clock cables
- Preamplifier and clocks boards
- Testing bench (proto box) with the ccd detector

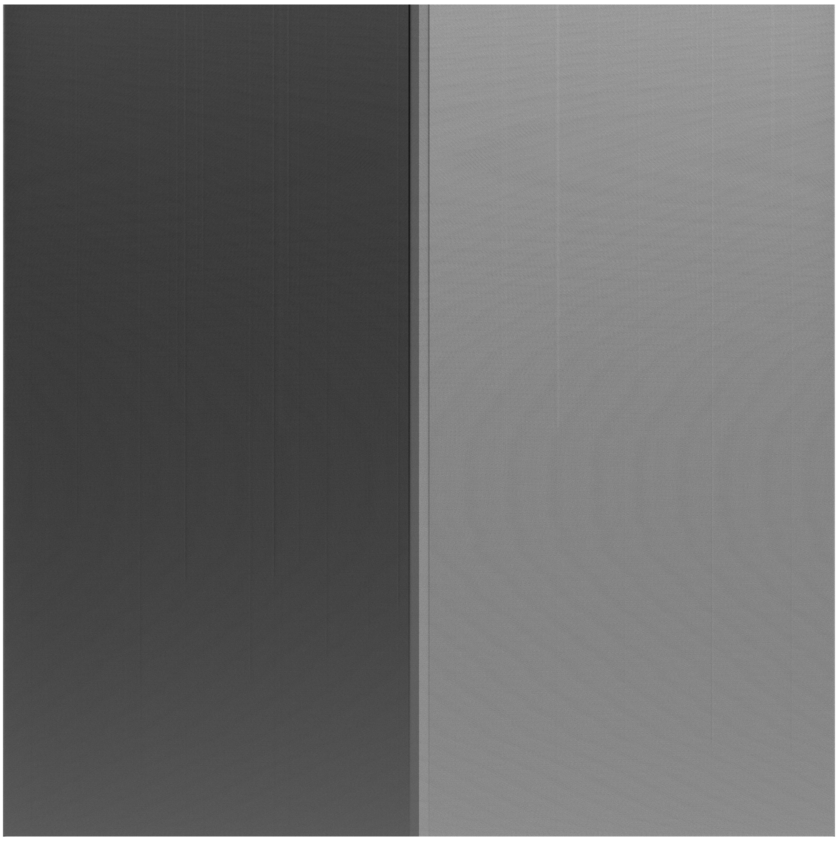

Figure 23 - CCD image at room temperature Readmode = LR-FAST

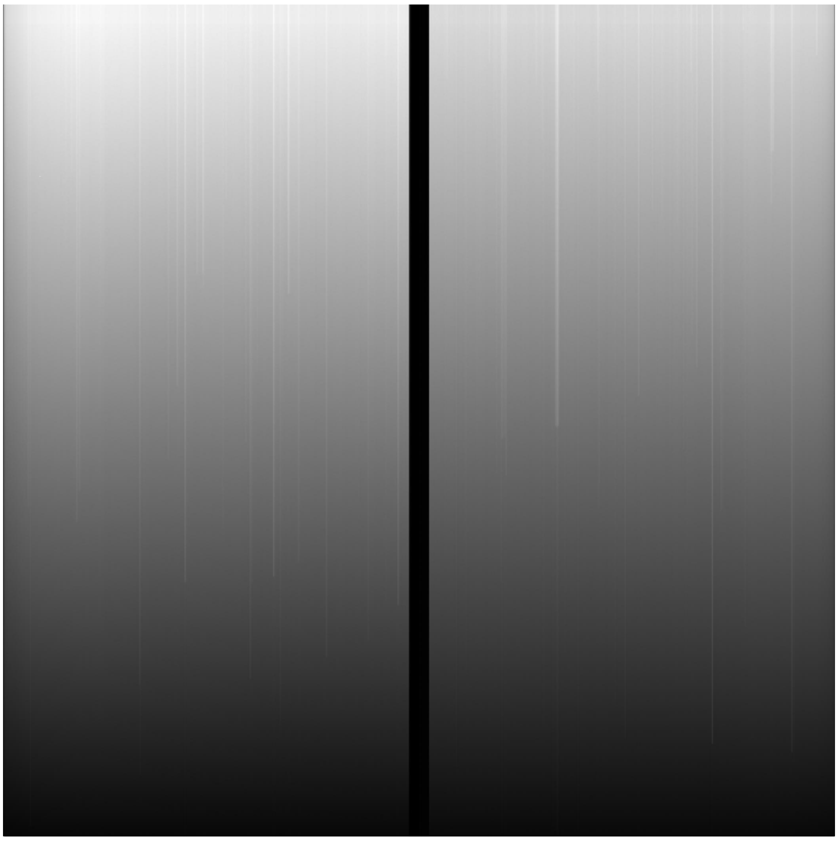

Figure 24 - CCD image at room temperature Readmode = LR-MED

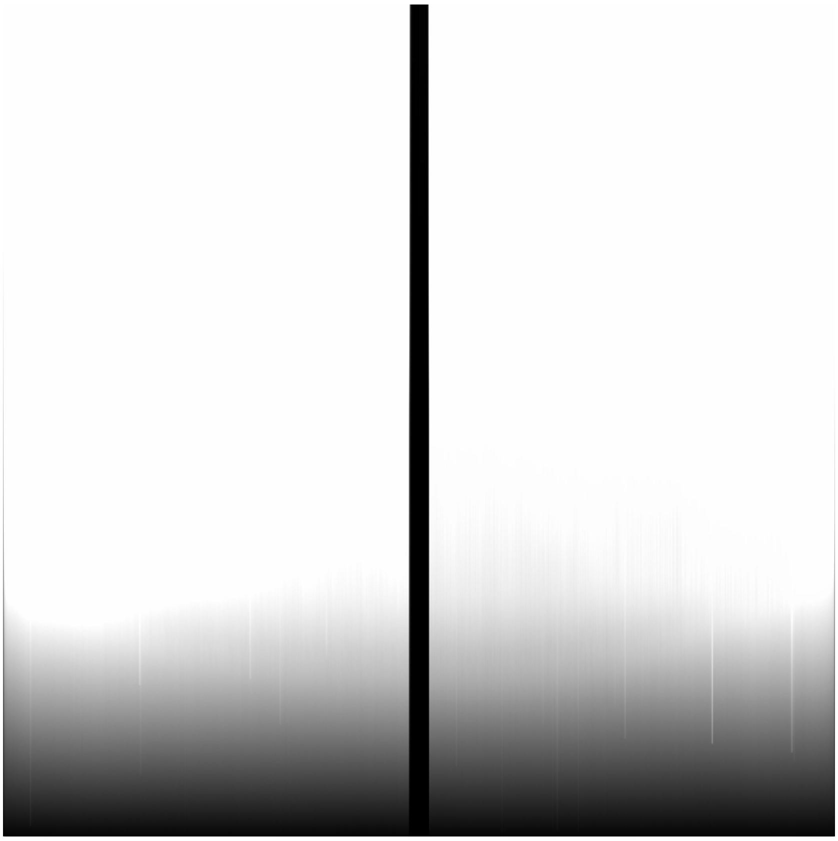

Figure 25 - CCD image at room temperature Read mode = LR-SLOW (saturated on the top of the image)

The results of the tests of the engineering CCD at room temperature shows that the acquisition system is working as expected.

The overscan of the two outputs are visible in the centre of the images, the cosmetic characteristics of the CCD is clearly visible and the gradient of the signal in the CCD area is according with the readout speed (more gradient at the increasing of the readout time).

The new acquisition system, based on the ARC controller passed the laboratory test and can be tested with the scientific CCD.

4.4.2. Scientific CCD at room temperature

The same test of the paragraph 4.4.1 was repeated with the e2v 42-40 scientific CCD, mounted in the LRS Dewar (Figure 26). The results were comparable with the test of the engineering CCD and demonstrated that the new CCD acquisition system can be used at the telescope as upgrade of the current one.

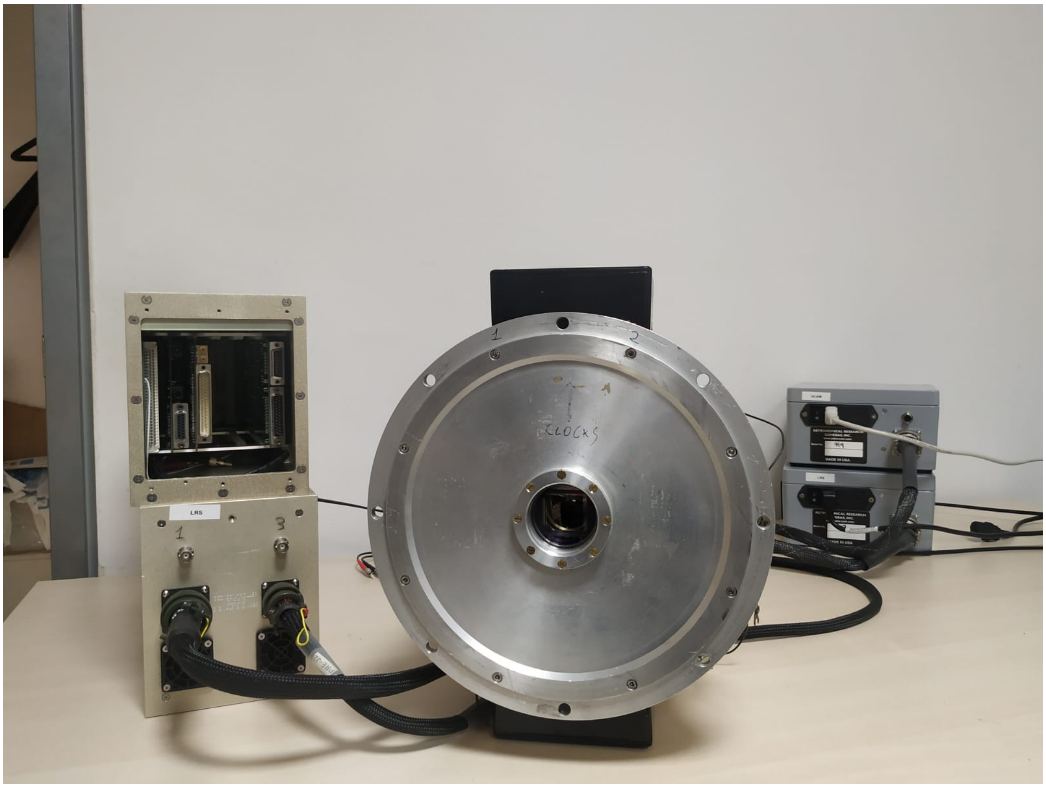

Figure 26 - LRS Dewar and ARC controller

4.4.3. Scientific CCD at cryogenic temperature

These tests are in stand-by and will be done as soon as the LRS detector will be available for the laboratory tests.

1. Appendix A – Document identification code

ORG-TYP-INS-NCOD

ORG = Originator field (i.e. TNG)

TYP = Document Type (see Table 4)

PRJ = project element (see Table 5)

NCOD= numeric code (i.e. 0001)

Example: TNG-MAN-HAN-0001

Table 4 - Document type code

AD	Assumption Document
AN	AN Analysis
COS	Cost Documents (Estimate/CaC/CtC, etc)
DD	Design Description
DP	Data Package
DRD	Document Requirements Description/Definition
DRL	Document Requirements List
DW	Drawing/Diagram
EID	Experiment Interface Document
FI	File (Software/Configuration/Network)
ICD	Interface Control Document
IRD	Interface Requirement Document
ITT	Invitation to Tender
MAN	Manual/User Guide/Handbook
MEM	Memo
MOM	Minutes of Meeting
MOU	Agreement/Memorandum of Understanding
MX	Matrix/Compliance
NCR	Non-Conformance Report
NOT	Note
OPS	Operations Document
PLN	Plan
PO	Proposal
PRE	Progress Report/Status Report
RFQ	Request for Quotation
SOW	Statement of Work
TOR	Terms of Reference
TN	Technical Note
TP	Test Procedure/Test Plan
TR	Test Report/Test Result

TS	Test Specification
VC	Verification Control Document
WBS	Work Breakdown Structure
WP	Working Paper
WPD	Work Package Description

2. Appendix C – Project Element Code

Table 5 – Project element code

BTM	Batman
CCD	CCD detector/electronic/software
HAN	HARPSN
TRK	Tracking
LRS	Low Resolution Spectrograph for TNG
SRG	SARG