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Temperature characterization of the CITIROC front-end chip of the ASTRI SST-2M Cherenkov camera.

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ABSTRACT

The Cherenkov Imaging Telescope Integrated Read Out Chip, CITIROC, is the front-end chip of the camera for the ASTRI SST-2M, one of the prototypes for the small sized telescopes of the Cherenkov Telescope Array, CTA. The telescope, operating in the energy range from a few TeV to beyond 300 TeV, is characterized by innovative technological solutions. The optical system is arranged in a dual-mirror configuration and the focal plane camera consists of a matrix of multi-pixel Silicon Photo-Multipliers. Among others, one of the most important project issue consists in the thermal characterization of the camera that, in the ASTRI SST-2M prototype, is thermo-controlled in a narrow temperature range. A set of at least nine similar telescopes will form the ASTRI mini-array proposed to be installed at the CTA southern site. In the cameras of the ASTRI mini-array telescopes the thermal control could be relaxed with a considerable gain in terms of power consumption, cost and simplicity. So, a study of the temperature dependence of the camera components is needed. The present work addresses this issue showing the results of the measurements carried out on CITIROC as a function of the temperature. We focused our investigation on the pedestal stability, linearity of the charge output signal, preamplifier gain and trigger uniformity in the temperature range 15-30°C. Our results show, for each of the above-mentioned measurable quantities, that temperature dependency is at the level of a few percent.

Keywords: Front-End; ASIC for SiPM; CITIROC; Photomultiplier : silicon ; Electronics Detector Readout; Integrated circuit; ASTRI; CTA

1. INTRODUCTION

The Cherenkov Telescope Array (CTA) is a large collaborative effort aimed at the design and operation of an Imaging Atmospheric Cherenkov Telescope (IACT) observatory dedicated to Very High-Energy (VHE) gamma-ray astrophysics in the energy range from a few tens of GeV to above 100 TeV[1, 2]. It will yield about an order of magnitude improvement in sensitivity with respect to the current major IACT observatories (H.E.S.S. [3], MAGIC [4], and VERITAS [5]). Prominent sources such as blazars, nearby well-known BL Lac objects, Galactic pulsar wind nebulae, supernova remnants, micro-quasars, and the Galactic Center will be observed with unprecedented sensitivity.

Within this framework, the Italian contribution to the CTA Project is mainly represented by the ASTRI (Astrofisica con Specchi a Tecnologia Replicante Italiana) project [6], supported by the Italian Ministry of Education, University and Research (MIUR) and led by the Italian National Institute for Astrophysics (INAF). Its primary target is to develop an end-to-end prototype of the Small-Size class of Telescopes (SST) in dual-mirror (2M) configuration devoted to the study of highest energy gamma rays range from a few TeV up to above

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100 TeV. The ASTRI prototype, named ASTRI SST-2M, is characterized by innovative technological solutions adopted for the first time in the design of Cherenkov telescopes: the optical system is arranged in a dual-mirror (2M) Schwarzschild-Couder configuration [7, 8], and the camera at the focal plane is composed by a matrix of multi-pixel Silicon Photo-Multipliers (SiPMs) [9–13].

In the ASTRI SST-2M prototype the camera is composed of a matrix of 496 Hamamatsu S11828-3344M* SiPM sensors with a total of 1984 squared pixels organized in 37 Photon Detection Modules (PDM) [14]. The very short (a few tens of ns) duration of the Cherenkov light flashes, associated with showers, requires a Front-End Electronics (FEE) able to provide auto-trigger capability and fast camera pixel read out. The FEE adopted for ASTRI SST-2M is based on the Cherenkov Imaging Telescope Integrated Read Out Chip (CITIROC) [15] (INAF intellectual property).

The evolution of ASTRI project is a collaborative effort among Italy, Brazil and South Africa to build a mini-array of al least nine ASTRI telescopes proposed to be installed at the CTA southern site as pre-production units.

While for the ASTRI SST-2M prototype old technology SiPM are used, a new model of SiPM is foreseen for the ASTRI mini-array. The new detectors exhibit low level optical cross talk, small gain variation with temperature, higher PDE (Photon Detection efficiency) and higher gain. Because of the improved performance of the new SiPM the thermal control of the ASTRI mini-array cameras could be relaxed.

This work presents the results carried out to characterize the CITIROC ASIC as a function of the temperature and its compliance with the new sensors. In particular, we investigated the pedestal stability, the linearity of the charge output signal, the preamplifier gain and the trigger uniformity as function of the temperature. We tested the whole electronics chain CITIROC + SiPM using a new version of the sensor, manufactured by Hamamatsu, opportunely designed to obtain a level of cross-talk $< 15\%$ and a dark rate < 1MHz. This device is not commercially available now, but some samples, named LCT (Low Cross Talk), have been sent to our laboratories for testing and characterization [16, 17].

2. THE CITIROC CHIP

CITIROC, designed by WEEROC†, is based on the extended analogue Silicon photo-multiplier integrated read out chip (EASIROC) [18–22] architecture, with the addition of the custom functions required by the ASTRI team.

It is a 32 channel fully analog front-end ASIC designed to read out SiPMs with sensitivity at level of single photon electron. Its analog core and characteristics are listed in [14]. The processing of the analog signal takes place in the front-end channels of the device, while the read out is handled at the internal back-end of the ASIC. A schematic view of CITIROC design is shown in Figure 1. Two separate electronics chains allow for High- and Low-gain (HG and LG) simultaneous processing of the analog signal. Each of the two chains is composed of an adjustable preamplifier followed by a tunable shaper (SSH: Slow Shaper), and a selectable track-and-hold circuit (SCA: Switched Capacitor Array) and an active Peak Detector (PD) employed to capture and hold the maximum value of analog signal. Fine-tuning of each pixel gain is obtained adjusting the voltage applied to the SiPM through an 8-bit Digital-to-Analog Converter (DAC) ranging from 0 to 4.5 V.

A third chain implements the trigger channel generation using a fast shaper (FSB: Fast Shaper Bipolar) with fixed shaping time of 15 ns, followed by two discriminators.

*http://www.hamamatsu.com/sp/hpe/HamamatsuNew s/HEN111.pdf

†http://www.weeroc.com

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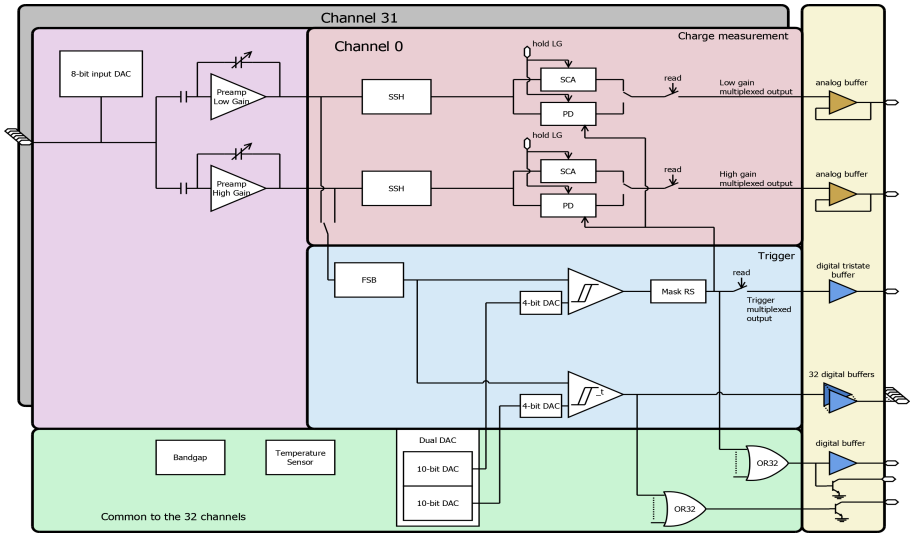

Figure 1. Architecture of the front-end CITIROC (courtesy of WEEROC).

3. EXPERIMENTAL SET-UP

We carried out two different sets of measurements aiming to characterize some specific CITIROC performance (pedestal and linearity) as function of temperature and to check that in the complete chain (CITIROC + LCT5 SiPM) the ASIC does not affect the correction of the gain variation with temperature. The HG preamplifier chain and the LG preamplifier gain are set to obtain a monotonic response from 1 to 100 pe and from 100 to 1000 pe respectively. The shaping time constant, for both HG and LG, is fixed at 37.5 ns, producing an actual peaking time of $\sim$40 ns.

For the CITIROC characterization we used an arbitrary pulse-function generator to create a precise and repeatable pulse signal (input charge). The input signal was injected in one channel of the front-end evaluation board located inside a controlled in temperature small metal box, as shown in Figure 2. The shape of the signal has been tailored to the actual shape of the LCT5 SiPM output pulse. It is characterized by a very fast rise time (a few hundreds of ps) followed by an exponential decay of about 250 ns. The amplitude of this signal has been fixed at a value of 315$\pm$4 μV, giving an input charge of 0.43 pC, equivalent to 1 pe for a SiPM operating at a gain of 2.72×10^6.

In the second set of measurements (CITIROC + LCT5 SiPM), performed with the same set-up, the SiPM pixels were illuminated by a Blue Light Diode (B-LED) driven by a pulse generator at a constant rate of 10 kHz. All measurements presented in this paper were performed in the temperature range 15-30°C and involve only one of the 32 channels available in the CITIROC, unless explicitly stated.

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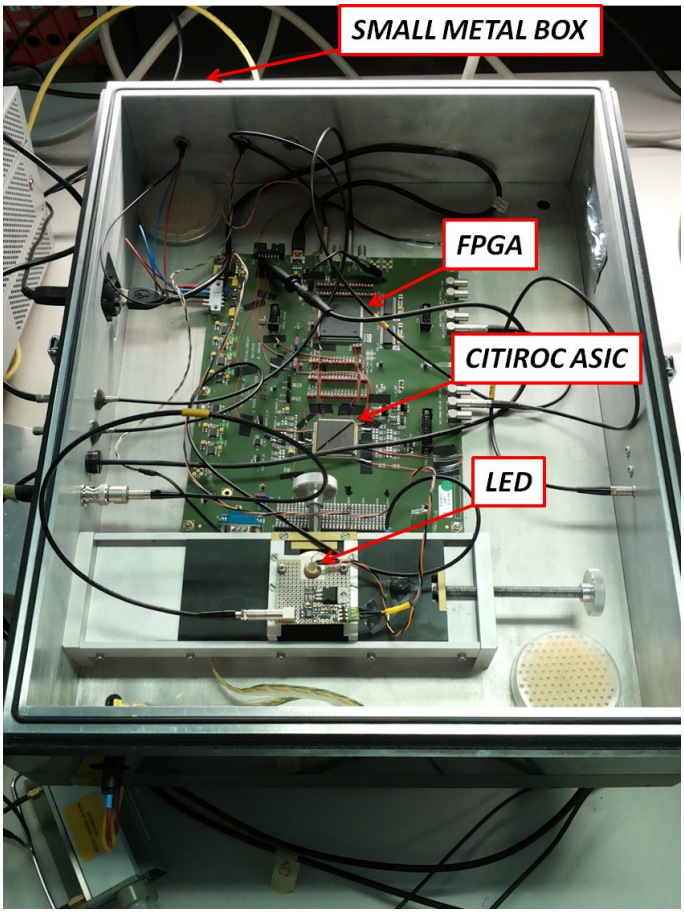

Figure 2. Experimental set-up used for the SiPM+CITIROC characterization.

4. CITIROC CHARACTERIZATION

In this set of measurements, we evaluated the pedestals, the output response linearity, the linearity, the efficiency and the cross talk of the trigger as function of the temperature. Measurements were performed injecting signals directly to the FEE from the pulse generator.

4.1 Output signal pedestal

To study the CITIROC pedestal no signal is injected and measurements are performed for all 32 channels. The values and the corresponding errors have been obtained by sampling, at fixed temperatures, the output signal of each HG and LG front-end channel in PD mode. In particular, the analog-to-digital converter (ADC) value of the pedestal and its error are computed as the average and the standard deviation of the distribution obtained with 5000 runs. Results are shown in Figure 3 for all the investigated temperatures (15, 20, 25, 30°C).

The maximum variation of the pedestals, that is relative to a change of the temperature from 15°C to 30°C, averaged over all channels is 1.3 ADC (with a RMS of 0.3 ADC). This value is of the same order of magnitude of the statistical error of each channel for both HG and LG chain.

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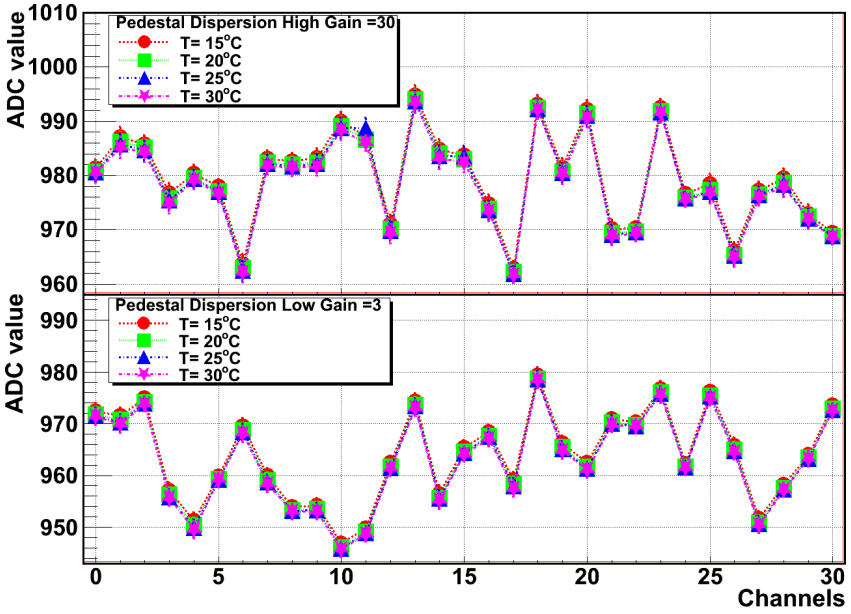

Figure 3. Pedestal ADC values of each channel as function of temperature for the HG and LG chains.

4.2 Output signal linearity

Linearity response measurements in the HG and LG chains as a function of temperature are performed injecting pulse signals into an FEE channel. The input charge ranges from 0.43 to 54.4 pC (1-125pe) for the HG and from 21.76 to 652.8 pC (50-1500pe) for the LG. For each point, the distribution of digitalized signals sampled over 5000 runs is collected. ADC values and errors are computed again as the average and the standard deviation of the distributions.

Results are shown in Figures 4 and 5. Linear fit of the curves in the range 0-43.52 pC (0-100 pe) for the HG chain and in the range 21.76-435.2pC (50-1000pe) for the LG chain shows good linearity response. The values of the slopes at the sampled temperatures are shown in Figure 6 and 7, respectively. A significant trend with temperature is observed in the slopes of the HG electronics chain. Fitting data with a constant gives a unacceptable value of χ^2 (7.5 for 3 dof). The slope variation with temperature obtained from the fit with a line is $\sim$0.006 ΔADC/pe/°C. The LG chain (see Figure 7) does not show any significant variation of the slopes with temperature; the fit with a constant gives a χ^2= 0.9 for 3 dof.

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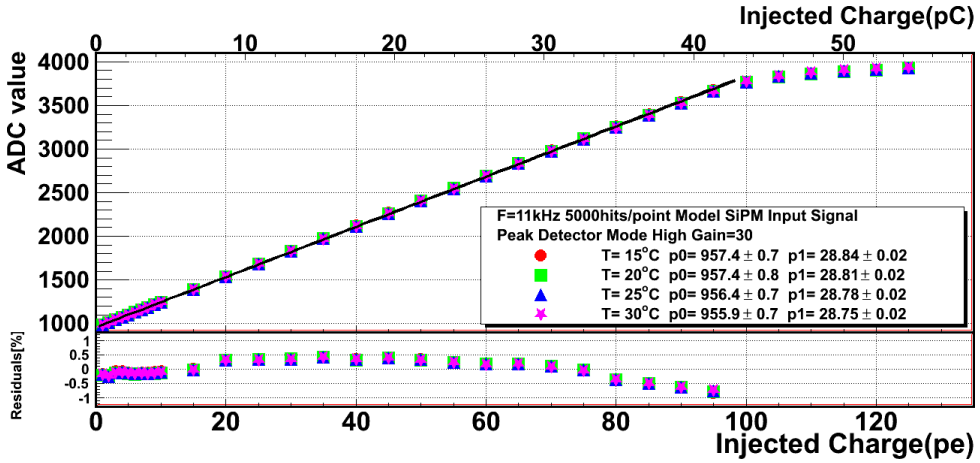

Figure 4. ADC values versus injected charges as function of the temperature for the HG chain. The black lines are the linear fits up to 100 pe where the ADC value saturates. The p0 and p1 are the intercepts and the slopes of the lines of the best fit. The bottom panel shows the residuals respect to the fitted lines and actual ADC values.

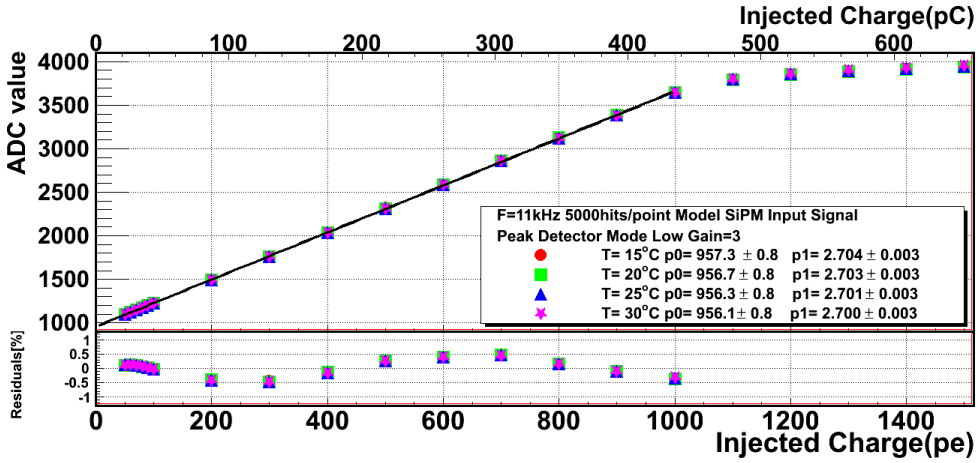

Figure 5. ADC values versus injected charges as function of the temperature for the LG chain. The black lines are the linear fits in the range 50-1000pe. The p0 and p1 are the intercepts and the slopes of the lines of the best fit. The bottom panel shows the residuals respect to the fitted lines and actual ADC values.

To complete our characterization, we investigated the presence and any possible changes with temperature of the electric cross talk. Injecting input charge in one channel we measured the output signal in the nearest ones. No significant electric cross talk is observed for any of investigated temperature.

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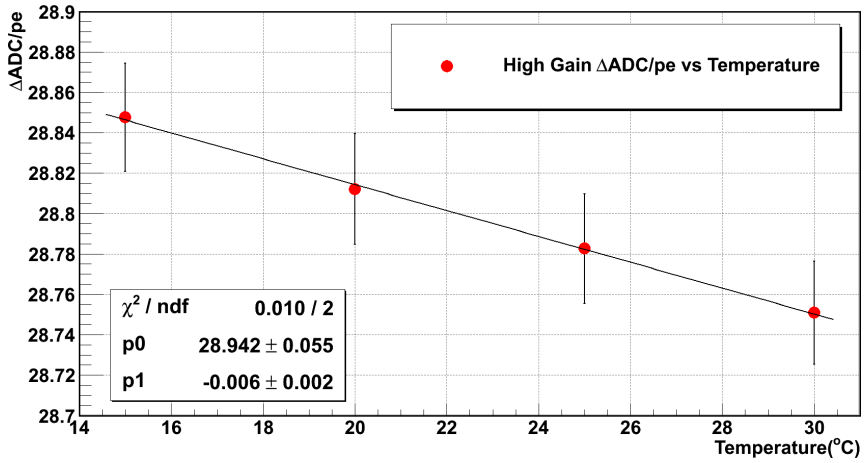

Figure 6. ΔADC/pe values versus temperature for the HG chain. The p0 and p1 are the intercept and the slope of the line of the best fit.

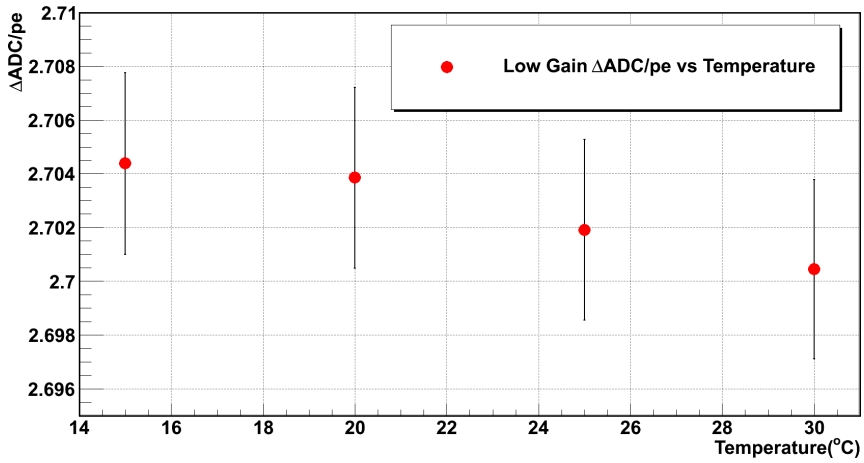

Figure 7. ΔADC/pe values versus temperature for the LG chain.

4.3 Trigger linearity and efficiency

To check the linearity of the ASIC discriminator, we studied the curves of the trigger efficiency as a function of the threshold. They are obtained by varying the input charge and the threshold level, keeping constant the other parameters, such as the preamplifier gain and shaping time. Figure 8 shows the evolution of the DAC relative to 50% trigger efficiency as a function of the injected charge in the range 0.43-17.40pC (1-40pe). To evaluate the variation with temperature, we use the change of the slope in the range where the DAC exhibits linearity.

Fitting with a linear regression each curves up to 4.78 pC (11 pe), slopes variation of the slopes gives ∼0.04 ΔDAC/pe/°C (see Figure 9).

As for the output signal, we investigated the electric cross talk of the trigger between neighbouring channels and found that it is always lower than 0.5%.

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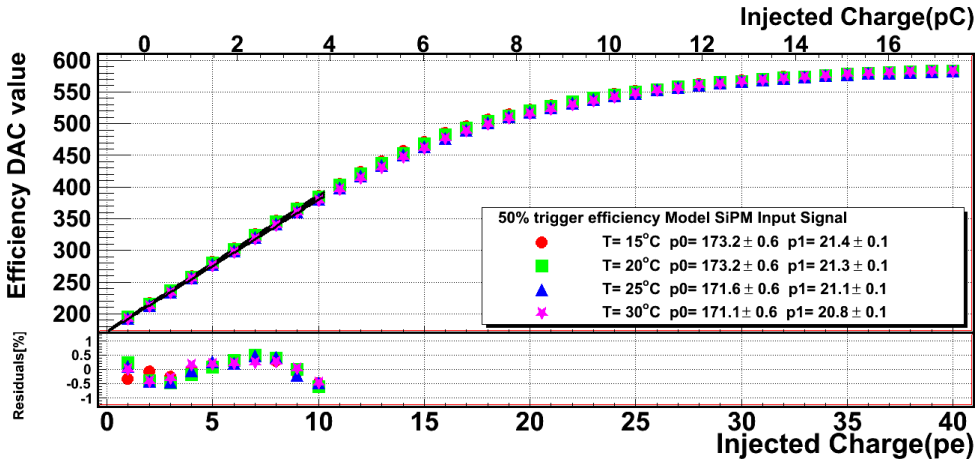

Figure 8. 50% trigger efficiency threshold versus injected charge from 0.43 to 17.40 pC (1-40pe) as function of the temperature. The p0 and p1 are the intercepts and the slopes of the lines of the best fit. The bottom panel shows the residuals with respect to the lines.

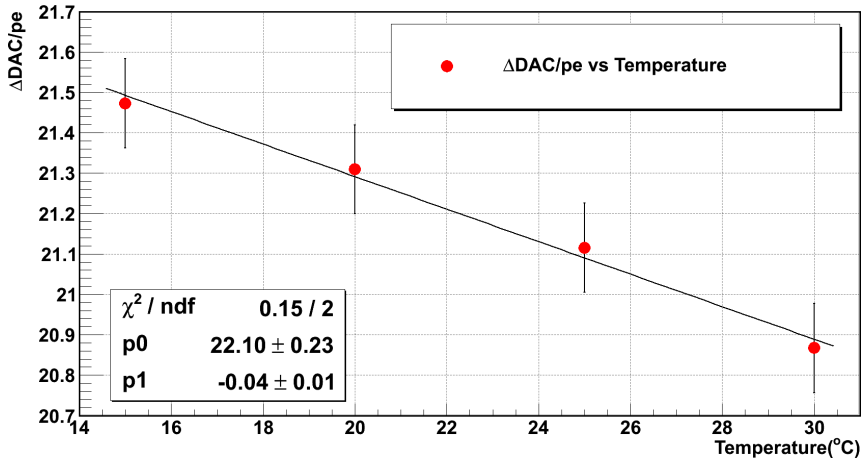

Figure 9. The variation of 50% trigger efficiency threshold versus temperature. The p0 and p1 are the intercept and the slope of the line of the best fit.

5. CHARACTERIZATION OF THE CITIROC + LCT5 CHAIN

The second set of measurements is performed on the complete chain (CITIROC + LCT5) with the B-LED. For consistency, we adopted the same gain applied in the first set of measurements. To verify this, we overlapped the Pulse Height Distribution (PHD) obtained for the SiPM with that from the pulse generator (see Figure 10): the two distributions have statistically compatible gain.

All results presented in this section are relative to the HG chain. The gain G in each histogram is determined from the average of the ADC distances between subsequent local maxima applying the following equation:

$$G = \frac{1}{N-2} \cdot \sum_{i=2}^{N} (ADC_{i+1} - ADC_i) \qquad [ADC] \tag{1}$$

where G is given in ADC units, ADC_i is the ADC value of the maximum of the i-th peak on the histogram while

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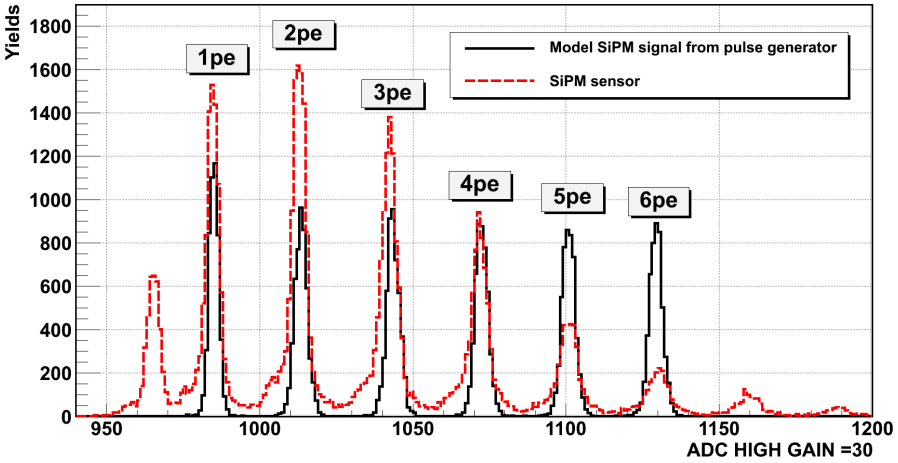

Figure 10. Overlap of the distributions obtained with the SiPM and with the pulse generator in the HG chain.

N is the number of peaks. The error on G is given by the standard deviation of the measured values with respect to the mean. In the gain evaluation, we excluded the pedestal (i=1) that contains events due to electronic and SiPM noise.

Figure 11 shows an example of the integrated charge spectra at the investigated temperatures. The operating voltage was adjusted to correct the temperature variation of the SiPM (0.52 ADC/°C).

We obtained that the ADC distances between the individual peaks of each pulse height distribution present differences of the order ∼0.3%.

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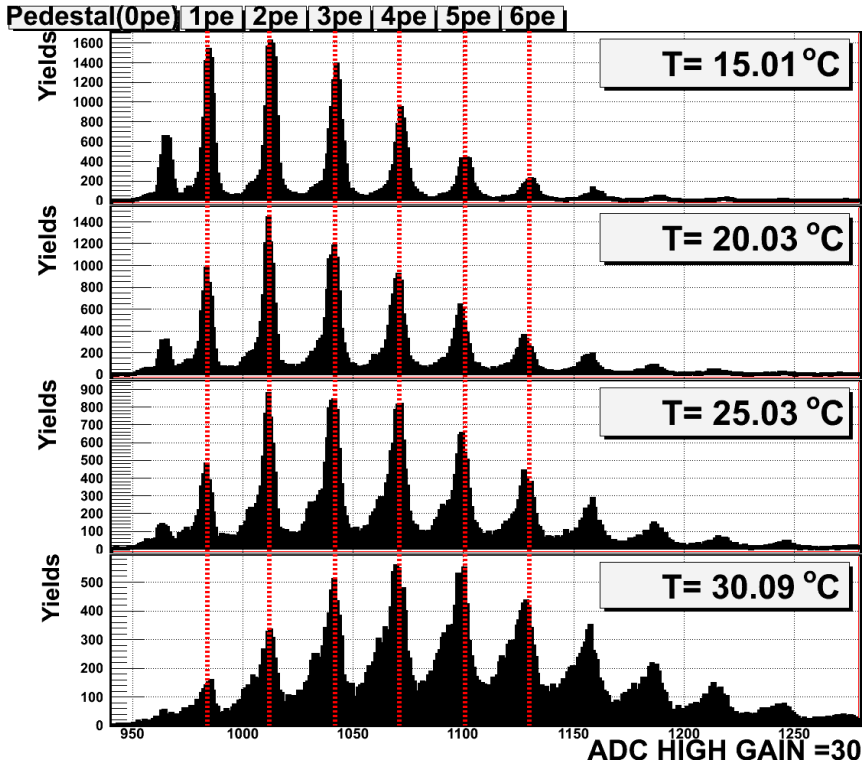

Figure 11. An example of pulse height distributions for several temperatures at a fixed gain of 2.72×10^6.

6. SUMMARY AND CONCLUSION

Characterization of the performances of the ASIC CITIROC as function of the temperature in the range 15-30°C has been performed in two steps using a laboratory set-up. Firstly, ASIC has been characterized using only a pulse generator. In this case evaluation of temperature dependence for pedestals, charge linearity and trigger linearity shows variations smaller than 1%. Moreover, no electric cross talk in the neighbouring channels was observed both in the signal and in the trigger.

In the second set of measurements, we found that CITIROC does not affect the correction of the SiPM gain variation with temperature. Increasing the temperature from 15°C to 30°C a residual gain discrepancy of the order $\sim$0.3% is observed.

We conclude that CITIROC is suitable for the ASTRI mini-array cameras in the whole working temperature range.

7. ACKNOWLEDGEMENTS

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