

The XGIS instrument on-board THESEUS: the detection plane and on-board electronics

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ABSTRACT

The X and Gamma Imaging Spectrometer instrument on-board the THESEUS mission (selected by ESA in the framework of the Cosmic Vision M5 launch opportunity, currently in phase A) is based on a detection plane composed of several thousands of single active elements. Each element comprises a $4.5 \times 4.5 \times 30$ mm³ CsI(Tl) scintillator bar, optically coupled at both ends to Silicon Drift Detectors (SDDs). The SDDs acts both as photodetectors for the scintillation light and as direct X-ray sensors. In this paper the design of the XGIS detection plane is reviewed, outlining the strategic choices in terms of modularity and redundancy of the system. Results on detector-electronics prototypes are also described. Moreover, the design and development of the low-noise front-end electronics is presented, emphasizing the innovative architectural design based on custom-designed Application-Specific Integrated Circuits (ASICs).

Keywords: THESEUS mission, Chipset, ORION, ASIC, Silicon Drift Detector, Scintillator crystals

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1. INTRODUCTION

The *Transient High-Energy Sky and Early Universe Surveyor* (THESEUS^{1,2}) is a space mission concept aiming at fully exploiting Gamma-Ray Bursts (GRBs) for investigating the early Universe and at providing a substantial advancement of multi-messenger and time-domain astrophysics. THESEUS is currently in Phase A study by the European Space Agency (ESA), as a candidate mission for the M5 slot for a possible launch in 2032. The Phase A study will be completed in Spring 2021 with the final downselection to one candidate in Summer 2021. The THESEUS mission is planned to be launched in a low Earth orbit (LEO) with low inclination ($<6^\circ$). Its planned nominal lifetime is 4 years, which ensures a sufficient number of high-redshift GRBs (according to the yearly rate of those type of events, which are among the main target of the mission) to be observed and studied.

The THESEUS payload combines two high energy instruments with large a Field of View (FoV) working in synergy for transient events detection. The *X-Gamma Imaging Spectrometer*³ (XGIS) is a wide field deep sky monitor covering the 2 keV–10 MeV energy pass-band. The XGIS consists of two units, with imaging capability in the 2–150 keV band through the employ of a coded aperture mask. In this energy range the FoV is $77^\circ \times 117^\circ$ while above ~ 150 keV the instrument acts as a full sky spectrometer. The two XGIS units are pointed at $\pm 20^\circ$ offset with respect to the payload axis in a way that their FoV partially overlap. Extensive study of the expected sources of background on the XGIS has been done and in particular of its effects on the instrument sensitivity⁴. The THESEUS *Soft X-ray Imager*^{5,6} (SXI) comprises 2 detector units (DU). Its 0.3–5 keV energy pass band partially overlaps the XGIS energy range. Each DU is a wide field Lobster Eye telescope using the optical principle first described by Angel (1979)⁷. The optics aperture is formed by an array of 8×8 square pore Micro Channel Plates (MCPs). The MCPs are 40×40 mm² and are mounted on a spherical frame with radius of curvature 600 mm (2 times the focal length of 300 mm). The use of the Lobster Eye concept allows an unprecedented combination of large FoV (0.5 sr), source location accuracy (< 1 –2 arcmin). The SXI and XGIS triggers on transient events are exploited by the third instrument of THESEUS, the near *Infra-Red Telescope*^{8,9} (IRT) which is composed by a primary mirror of 0.7 m of diameter and a secondary mirror of 0.23 m in a Cassegrain configuration. In imaging mode the IRT has a FoV of $15' \times 15'$. Transient events that triggers in the FoV of the SXI and/or XGIS will be observed by IRT that will provide immediate identification systematically within a few minutes with sub-arcsecond position accuracy and spectroscopic redshift determination. An overview of the THESEUS mission with its payload is given in Figure 1. The three instruments are coaxial and in particular, the SXI FoV is fully included in that of the XGIS.

In the following Sections a detailed description of the XGIS will be given, focusing on the design of the detection plane and on the related readout electronics. For each XGIS camera, a customized architecture for the electronics is required, given the complexity and peculiarity of the detection plane, made with 12800 silicon-based detectors coupled in pairs to 6400 scintillator bars. The design of an Application Specific Integrated Circuit (ASIC) chipset for the XGIS instrument, named ORION, is presented. Both ORION front-end (ORION-FE) and ORION back-end (ORION-BE) structures with their interaction are described. Simulation results of a single-channel prototype, which is currently being experimentally characterized, are discussed.

2. XGIS: GENERAL OVERVIEW

The XGIS¹⁰ instrument is composed by two cameras which are tilted of $\pm 20^\circ$ in the two opposite directions with respect to the satellite axis¹¹. To enable imaging capability for each XGIS Camera in the 2–150 keV energy range, a coded aperture system placed 63 cm above the detection plane will be used. In order to provide effective coding of the sky in the full energy range, the coded mask opaque elements are 1 mm thick. In its imaging energy range, the XGIS FoV fully overlaps that of the SXI. A collimator made of Al enclosing a W foil 0.25 mm thick limits the FoV of each XGIS Camera to $77^\circ \times 77^\circ$. Under these assumptions the overall FoV of the XGIS will be $117^\circ \times 77^\circ$. Each Camera is composed by a matrix of 5×2 *Super-Modules*, while each Super-Module is in turn composed of 10 *Modules*. Finally, each Module consists of a matrix of 8×8 pixels which are Thallium activated Cesium Iodide (CsI(Tl)) scintillator bars coupled to two Silicon Drift Detectors (SDD) cells, at top and at bottom side of each CsI(Tl) bar. The SDDs work both as direct detectors for low energy photons and as a readout system for the scintillation photons. Indeed, low energy X-rays (< 30 keV) interact directly in the SDD, while for energies above 30 keV the indirect photon detection occurs with the photon interaction in the CsI(Tl) crystals. The resulting scintillation light, which is in the optical energy range, is collected by SDDs

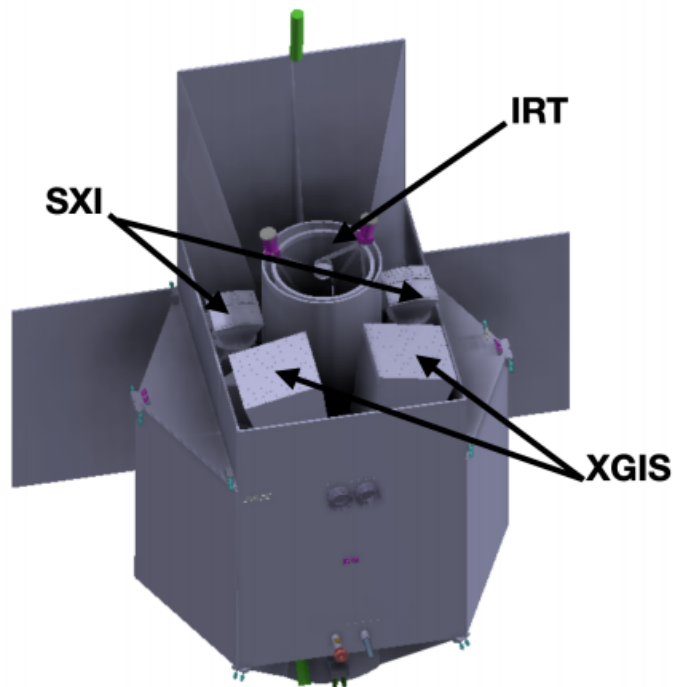


Figure 1. An engineering drawings view of the THESEUS mission with the three on-board instruments.

on both side of the crystal. Such configuration, allowing for a compact and efficient broadband single device detection unit, has been also called *siswich* (from Silicon-sandwich)¹²⁻¹⁴ in analogy with the phoswich detection system successfully used in several experiments (e.g. PDS/BeppoSAX¹⁵, HEXTE/RXTE¹⁶, HE/HXMT¹⁷). The SDD size determines the spatial resolution of the detector. Furthermore, if the interaction occurs in the scintillator bar, by weighting the signals from the SDD at both ends (whose intensity is inversely proportional to the distance between the interaction point and the SDD), the coordinate of the scintillation point along the bar can be estimated. Figure 2 illustrates the working principle of the *siswich* detection system, together with the achievable detection efficiency.

In the XGIS configuration, each CsI(Tl) bar has dimensions $5 \times 5 \times 30 \text{ mm}^3$, the longer dimension along the XGIS Camera axis. A custom electronic read-out will distinguish the two kind of signals, depending on the interaction that can occur directly on the topmost SDD (the one facing the sky) or on both SDDs, meaning that the radiation interacted in the CsI(Tl) bar. In particular, electron-hole pair creation from X-ray interaction in Silicon generates a fast signal (about 100 ns rise time). On the other hand, due to the fluorescent light component and crystal characteristics, the scintillation light collection is emitted and collected in a much longer timescale (typically 1–2 μs).

The segmented structure leading progressively from a single SDD+CsI(Tl)+SDD pixel to a camera (Figure 2) and to the XGIS full system is also explained with the diagram shown in Figure 3 in which are also reported the sub-systems correlated to each structure of increasing complexity. In particular, the highlighted blocks are those directly connected both to the modularity of the instrument and to its associated electronics. These two topics are the subjects of this paper. In the following Sections we will describe the Module ORION ASIC, the Super-Module back-end electronics (BEE) and the Camera BEE, respectively. Finally, a general description of the XGIS system will be reported with particular highlight to the the power distribution, to the Data Handling Unit (DHU) and to the total power consumption of each XGIS camera.

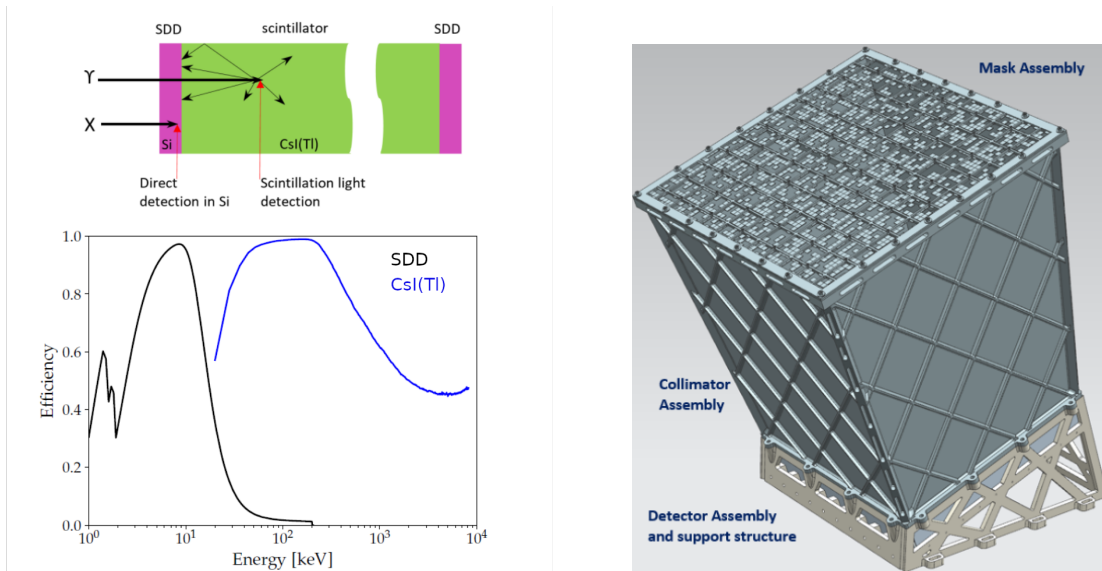


Figure 2. *Top left:* the working principle of a *siswich* detection system. Two SDD are placed at both ends of a CsI(Tl). The low energy radiation (below ~ 30 keV) interacts in the SDD. Photons with energy above a certain threshold cross the SDD and interact in the scintillator bar. The light output is collected at both SDD coupled with the CsI(Tl) bar. *Bottom left:* efficiency vs. photon energy for the direct detection in the SDD (black curve) and through light conversion in the CsI(Tl) (blue curve). *Right:* design of one XGIS camera on board THESEUS.

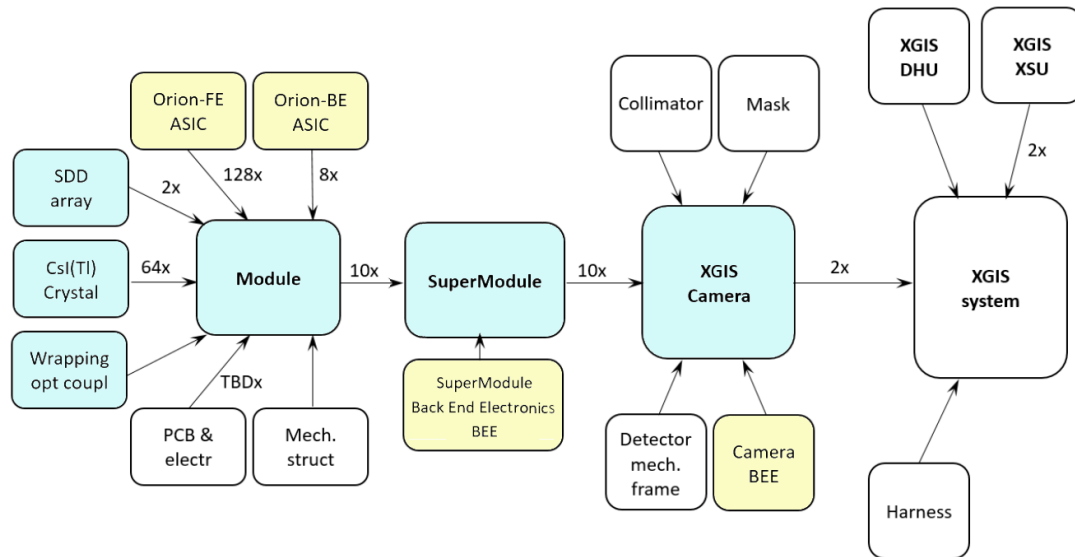


Figure 3. Block diagram showing the XGIS systems and subsystems. In the present paper we focus on the modularity of the XGIS (cyan blocks) with increasing complexity from left to right and on the electronics (yellow blocks).

3. XGIS MODULE SILICON SENSORS: SDD

Due to the peculiarity of the detector architecture of the combined detection of X and Gamma radiation in the THESEUS XGIS instrument, a fully custom SDD matrix design is needed. The SDD development activity is a natural progress of the developments carried out within the ReDSOX research program* financed by INFN and co-financed jointly by FBK for the part related to the SDD technology.

In particular, the XGIS application provides the optical coupling of two SDD sensors to the opposite faces of

*<http://redsox.iasfbo.inaf.it>

a scintillator bar to detect the light generated by the interaction of gamma radiation within the crystal. In this configuration, the SDD sensor is also capable of detecting the X radiation impinging on the face not coupled to the crystal, facing the sky. This solution is also suitable to the realization of a detector with imaging capability by packing together a certain number of scintillator bars read out by monolithic SDD sensor matrices. In the ReDSOX context, some SDD sensor prototypes dedicated to this application have been designed, implemented and characterized. Already in the early stages of prototype development, the size of the scintillator bar section was originally chosen as $5\text{ mm} \times 5\text{ mm}$. Consequently, SDDs have been designed with elements with this active area and the design parameters have been determined so as to optimize the performance for this specific dimension. The simulation and design of the devices is carried out by the INFN section of Trieste and by the University of Udine, while the realization takes place in the Micro Nano Facility of FBK. A first technological validation test of the sensors is performed in FBK at wafer level, while a more accurate characterization is carried out after the cut by TIFPA-TN in collaboration with INFN-TS.

In a XGIS module are employed 2 SDD-arrays, each one made by 8×8 individual SDD elements as shown in Figure 4, whose parameters are summarized in Table 1. The detectors are made using a full double-side process: the p-side is the side in which the optical entrance window is made exploiting a shallow implant, while the n-side is the side in which the collecting anode electrode is made by an ohmic bulk contact, surrounded by the drift rings. The basic geometrical parameters are: the pitch between elements, that has been fixed to 5 mm, and the peripheral guard-rings structure ($\sim 1.2\text{ mm}$ wide), whose represents an insensitive area to the incoming radiation, reducing the overall fill factor of the final assembly.

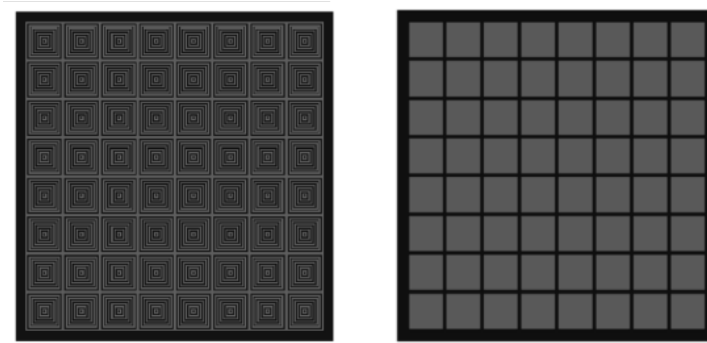


Figure 4. XGIS SDD array with 8×8 individual SDDs. *Left:* the *n*-side, with collecting anodes. *Right:* the *p*-side that will be optically coupled to scintillators

The *n*-side of the detector will be directly exposed to radiation. The sensitive area for X-rays detection, which in principle is the geometrical area $5 \times 5\text{ mm}^2$ of each array element, is instead reduced due to a partial obstruction made by the assembly PCB. At the end, the final sensitive area will be defined by the definitive version of the assembly PCB. The *p*-side of the detector will be optically coupled to the scintillators. To guarantee an adequate optical separation between adjacent elements, a 0.5 mm wide Al track is deposited between the SDD elements, thus reducing the sensitive area for the scintillation light to $4.5 \times 4.5\text{ mm}^2$.

The depletion voltage of each SDD (VDEPL), is strongly linked to the doping concentration of the substrates and then for a large area detector the doping uniformity at wafer level is crucial. For devices manufactured in the same production run with the same substrate batch VDEPL uniformity level well fit the requirements for the production of the XGIS sensor for THESEUS. However for XGIS-Camera we foresee to select SDD with uniform VDEPL for the same Super-Module (assembly with 10 Modules mechanically and logically connected), regulating the VDEPL at Super-Module level via TLC. A first production of such devices, to both check the process flow and the device layout, has been carried out in FBK during the first part of 2019 and concluded in June 2020. Such batch results in a multi-project wafer assembly. Preliminary measurements were performed in FBK to acquire the IV-total curve, with the aim to estimate the leakage current density for each SDD array, as a kind of production quality check. From such measurements, SDD arrays results in very low-level leakage current density, estimated to be $< 200\text{ pA/cm}^2$ measured at $+24^\circ\text{C}$, then considered very promising for further

Table 1. Main parameters of the SDD array

Array size	$42.4 \times 42.4 \text{ mm}^2$
Si thickness	$450 \mu\text{m}$
# of SDD	64
Single SDD active area (n side)	$5 \times 5 \text{ mm}^2$
Single SDD active area for scintillator (p side)	$4.5 \times 4.5 \text{ mm}^2$
Metal grid between single SDD (p side)	0.5 mm wide
Typical polarization voltage (1 connection for the whole array)	$-100 \div -150 \text{ V}$
Typical return voltage (1 connection for each SDD)	$-12 \div -20 \text{ V}$
Single SDD capacitance	50 fF (typical)
Dark current (typical at $T = 20^\circ$)	50 pA (typical)
Optical spectral response	350 – 1000 nm (typical)
QE	$> 80\%$

investigations and characterization of the single SDD cells.

4. XGIS MODULE READOUT ASIC: ORION

The electrical signals from the SDD anodes are collected and processed by the ORION chipset, a constellation of ASICs composed by the ORION-FEs, for the charge readout and the initial signal shaping placed in close proximity of the SDDs, and the ORION-BEs for the complete signal processing and digitization. The simplified schematic of the ASIC readout architecture is shown in Figure 5. A similar structure is adopted in the HERMES (*High Energy Rapid Modular Ensemble of Satellites*) nano-satellites mission^{18,19} in which the ASICs of the LYRA family (LYRA-FE and LYRA-BE) are employed.

The ORION chipset is responsible for both the analog readout of the SDD charge and for the digitization and data communication of the event information to the module electronics. For each detected event, the ORION ASIC is able to provide the energy of the event, the type of the event (i.e. X or γ) the position of the event (i.e. pixel coordinates) and the timing of the event with respect to an external clock. The ORION chipset is composed by a total of 12800 analog ORION-FE that send a pre-shaped signal to 800 mixed-signal back-end multi-channel chips (8-channels ORION-BE) for dedicated signal processing and digitization.

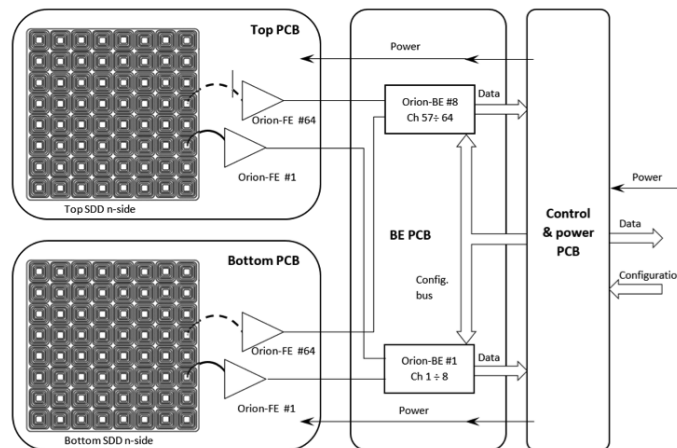


Figure 5. Structure of the electronics for collecting and processing the SDD signals based on the ORION-FE and ORION-BE ASICs.

Due to the peculiar architecture of the ASIC, each single channel ORION-FE is physically placed close to the SDD anode, in order to keep the stray capacitance at the preamplifier input as low as possible. The

ORION-FE single channel collects the SDD generated charge and performs pre-amplification. The ORION-BE, that is physically placed a few cm away on the bottom of the module, receives the signals from 8×2 ORION-FEs, processes them, handles the time marking of each single event and interfaces with the module electronics (Figure 6).

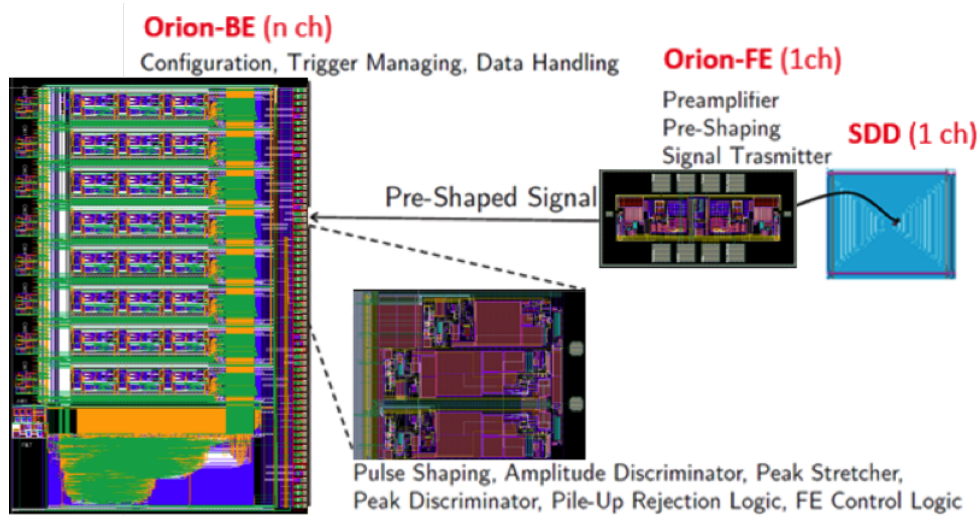


Figure 6. Structure of the electronics for collecting and processing the SDD signals based on the ORION-FE and ORION-BE ASICs.

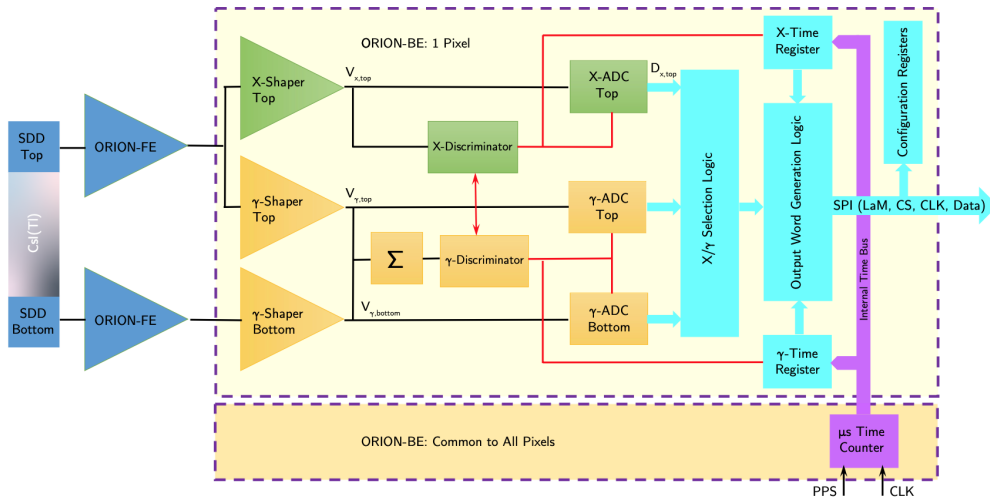


Figure 7. The ASIC architecture related to a pixel.

Figure 7 shows the general ASIC architecture for a single pixel, which, as discussed previously, is composed by two SDD optically coupled with a CsI(Tl) bar at both ends. The rationale for this architecture is the following:

- If an X-ray (2–30 keV) is detected only in the top SDD (hereafter called *X-mode event*):
 1. The preamplifier output signal is fast (hundreds of ns).
 2. As the X-ray detection is (almost) point-like in the SDD, the arriving time of the signal at the SDD anodes is delayed up to $1 \mu\text{s}$ with respect to the event occurrence, due to the drift time of the electron cloud within the SDD. The time marking of the event is then affected by the uncertainty due both to the jitter of the trigger and to the unknown position of the interaction in the SDD (Figure 8).

3. The best signal/noise ratio is achieved with a short shaping time ($1 \mu\text{s}$ typical).
 4. The discrimination between X-ray and γ -ray is done only using the top SDD signal (see below).
- If a γ -ray ($>20 \text{ keV}$) is detected simultaneously in top and bottom SDDs (hereafter called γ or *S-mode event*):
 1. The preamplifier output signals is slow (of the order of few μs), in agreement with the typical scintillation decay time.
 2. The scintillation light is spread across the whole SDD, therefore both scintillation time and maximum drift time of the charge should be taken into account to avoid ballistic deficit.
 3. The best signal/noise ratio is achieved with shaping time of the order of $3 \mu\text{s}$ (typical).
 4. The amplitude discrimination is achieved operating on the sum of top and bottom SDD signals.
 - Mixed X-ray/ γ -ray events in time coincidence can occur with quite low probability (few % even at the highest photon energies).



Figure 8. The time marking of the X and γ -events. *Left*: an X event is detected only in the top SDD but the time tag is affected by both the trigger jitter combined with the uncertainty due to the charge drift time due to the unknown interaction position within the SDD cell. *Right*: the time tag of a γ -event depends on the trigger jitter combined with a longer signal collection due to the fluorescence light component.

4.1 ORION-FE

The ORION-FE is a fully-analog ASIC conceived to provide the first amplification of the charge signal coming from the SDD, keeping a low area occupation ($\sim 0.3 \text{ mm}^2$) in order to allow a close connection to each anode, without compromising the detection area. The ORION-FE is mainly divided in three stages: a Charge Sensitive Amplifier (CSA) with a dynamic range of 32 fC, followed by a pole-zero compensation stage and a current conveyor, which additionally introduces a first CR shaping with $1 \mu\text{s}$ time constant. To avoid spurious injection the CSA is operated in continuous reset mode, and the output of the ORION-FE is delivered as a current signal generated by the current conveyor itself. Each ORION-FE has a power consumption of $290 \mu\text{W}$ at $T = -20 \text{ }^\circ\text{C}$, which also includes the contribution from the internal biasing module and of the Electrostatic Discharge (ESD) protection module.

4.2 ORION-BE AND LOGIC

The signals generated by the top and bottom ORION-FE of each pixel are transmitted as current signals on $\sim 4\text{--}5 \text{ cm}$ long lines and readout by the ORION-BE using two low-input impedance current receivers. A signal coming from the bottom SDD is uniquely identifying a γ -ray event, while the signal coming from the top SDD cannot be a priori identified as an X or γ -ray event, and the output of the top current receiver is sent to both X-/ γ processing channels, which operate with peaking times of $1 \mu\text{s}$ and $3 \mu\text{s}$, respectively. The stretched output voltage is then digitized by a second-order 12 bit ENOB incremental A/D converter. After the conversion, the pixel logic is able to discriminate the type of detected event, with the respective timestamp, and eventually forward the information to the on-board module electronics. Each read-out BE channel is thus made up by three parallel paths, each one including also an independent ADC. Even if the BE discriminators deliver X and

γ related triggers on a given event, due to the nature of the instrument, this information is fundamental but not sufficient to determine the type of event. For this reason the ADC outputs as well as the triggers from the BE are processed by a dedicated logic which has the double aim of extracting the type of event, assigning the timestamp and creating the digital output frame. This frame will include information on the event time, the type of event, its address, the discriminators triggered during the event and, in probe mode, further information useful for detailed characterization of the ASIC, such as, for instance, the signals on the internal ADC buses. In probe mode through a multiplexer and a buffer also all the analog outputs of the BE channels and their triggers are available for external measurement. Finally, in the multi-channel ASIC several channels may trigger together for a common event. For this reason, the embedded logic waits a programmable time, named RTP (Rise-Time Protection), before sampling all the BE signals (analog and triggers), starting the data conversion and finally building the output frame. When the frame is ready, a Look at Me (LaM) signal is given. The ORION ASIC embeds 1-kbit memory bank for SDD read-out analog channel configuration, for internal logic settings and for temporary output frame storage. The configuration and the output frames can be loaded/read-out either through a shift register or an SPI interface, based on a 4-wire bus plus reset. The ORION-BE has a power consumption of 980 μW per pixel (including both X/ γ channels) at $T = -20^\circ\text{C}$.

4.3 ORION RESULTS

The ORION chipset has been simulated to have an Equivalent Noise Charge (ENC) (with a detector capacitance of 50 fF and a leakage current of 0.7 pA) of about 12.5 e^- r.m.s. at 1 μs of peaking time on the X channel and 32.9 e^- r.m.s. at 3 μs on the γ channel. Despite a very wide input dynamic range on the γ channel (from 400 e^- to 180 000 e^-) the expected linearity error is below $\pm 1.2\%$, and below $\pm 0.1\%$ on the X channel. Due to the expected degradation of the SDD leakage current during the whole mission lifetime, the ORION chipset must be capable of handling high levels of input currents, up to 700 pA, which represents the worst case scenario for the detector leakage current in the End-Of-Life (EOL) condition, as shown in Figure 9. The ORION chipset, whose architecture is shown in Figure 6, is currently under production in its 4-channel version, and the experimental characterization on one front-to-back channel is expected by the end of 2020. In fact, a single channel version of the ORION ASIC, the layout of which is shown in Figure 10, is under experimental characterization, while a stand-alone analog-to-digital (A/D) converter module has been already produced and characterized. Figure 11 shows the measured accuracy in terms of Effective Number of Bits (ENOB) of the elementary A/D converter developed *ad hoc* for the ORION ASIC, featuring 11.9 bits including both noise and distortion effects.

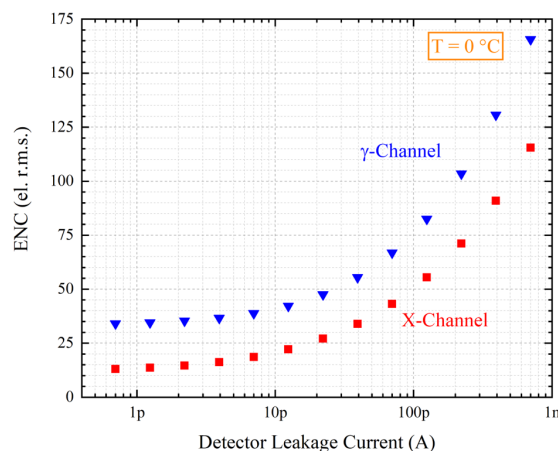


Figure 9. Simulated noise for different input leakage currents, corresponding to the expected Beginning-Of-Life (0.7 pA) and End-Of-Life (700 pA) performance of the detector.

5. SUPER-MODULE AND CAMERA BACKEND ELECTRONICS

A XGIS Super-Module is a logical and hardware subset of the detector assembly and consists of 10 Modules joined with a Super-Module Back End Electronics board (SM-BEE). The segmentation of the XGIS camera in

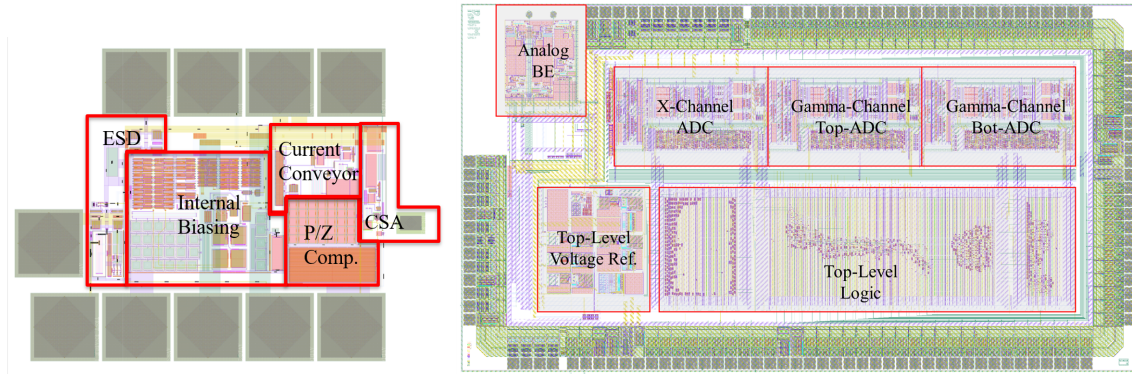


Figure 10. A detailed layout view of the ORION-FE (left) to be placed in close proximity of the SDDs and of the single channel prototype of the ORION-BE (right). In the top-left corner of the ORION-BE, the analog BE module, with the two small-pad inputs, is visible. The analog-BE as well as the ADCs are realized on a modular layout structure, for ease of implementation in multi-channel architectures.

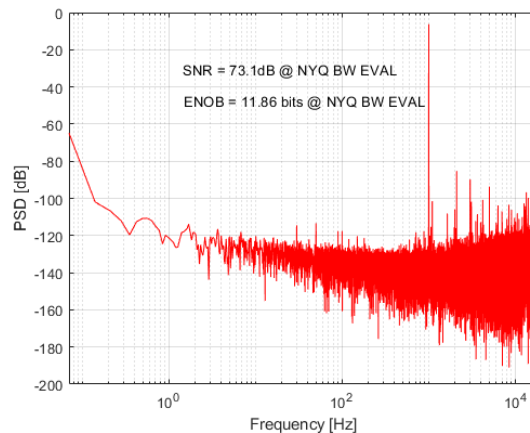


Figure 11. ORION ADC elementary module output spectrum applying a 1 kHz sinusoidal signal at full scale

Super-Modules allows to mitigate the effects of a potential system failure that, in case of occurrence at Super-Module level, would consist in a reduction of only 10% of the sensitive area. The modularity at the ASIC level ensures that in case of failure of an ASIC only 8 pixels are unusable. By exploiting the same concept, for each detected event, only 8 pixels get “frozen” leading to a dead time interval (since the corresponding ASIC is busy). On the contrary, it allows to perform parallel acquisition of contemporary events falling in non-adjacent pixels. The segmentation in Super-Modules also ensure a remarkable reduction of the connections between ORION-BE ASIC and FPGA (5 lines), of the total FPGAs used in a XGIS Camera (10 FPGAs) and of components (ADCs+Logic embedded into the ASICs). For each XGIS-Camera is also planned to install selected SDD with uniform depletion voltage (VDEPL) in the same Super-Module, with the possibility of regulating the VDEPL at Super-Module level via telecommands. The possibility, for large area detectors, of a fine tuning of VDEPL is crucial. In Figure 12 are shown a general view as well as an exploded view of a single Module together with the full detection plane in which is highlighted its partition in 10 Super-Modules.

The SM-BEE provides the power supply to 10 Modules, commands the Modules, collects the data (events/HKs) from the Modules and interfaces all the functions (commands, HKs, Alarms, Data) with the XGIS Camera Back End Electronics (C-BEE). The architecture of the SM-BEE will be built around one FPGA that will control 80 Orion-BE ASICs with a logic as depicted in Figure 13 whose main characteristics are:

- for the I/F with each single ORION-BE ASIC there are only 5 logic lines between the FPGA (where 3 of them are in common);

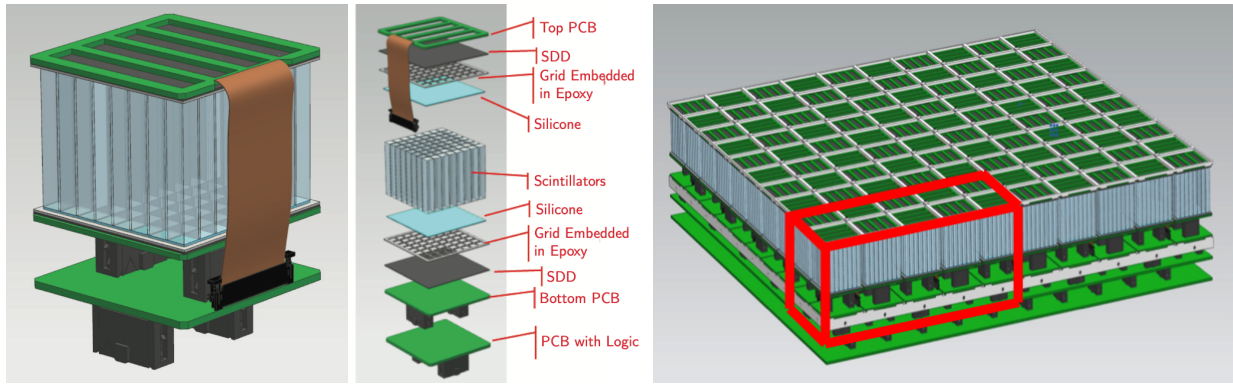


Figure 12. *Left:* A Module of the XGIS in which are visible the different parts that compose the detector pixels and the PCBs. *Right:* an XGIS Super-Module (highlighted in red) which is made with 10 Modules. One entire XGIS camera, which is also visible in figure, is made with 10 Super-Modules.

- the FPGA of the SM-BEE manages $160+3 = 163$ logic lines in total (I/O pins);
- the I/F with the C-BEE will be buffered with a memory of proper size;

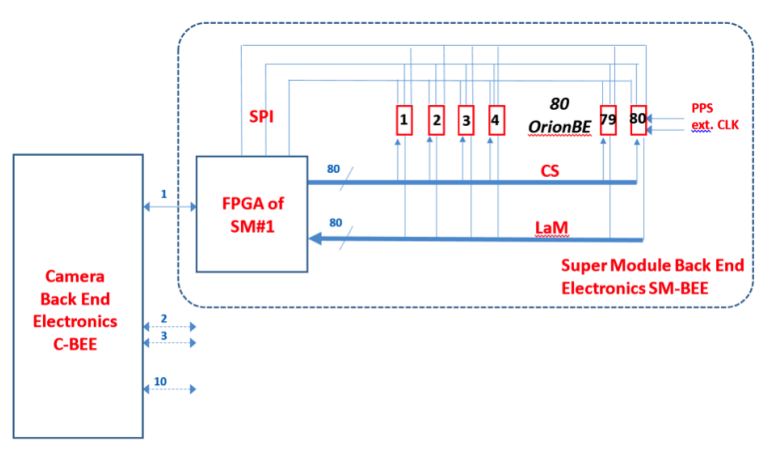


Figure 13. Logic concept of the Super-Module Electronics. One FPGA manages 80 ORION-BE and 10 SM-BEE are connected to the Backend Electronics of the Camera (C-BEE).

The XGIS Camera is managed through a Camera Back End Electronics board (C-BEE) which is organised in two logical sections, in cold redundancy, each connected to the DHU main and redundant section respectively, and simultaneously connected with the 10 SuperModules. The main functions of the C-BEE are of providing power supply distribution and management of all Super-Modules and of power supply interface with the XSU. Other functions of the C-BEE are: Data I/F with all Super-Modules, Data buffering and I/F with XGIS-DHU, telecommands I/F with XGIS-DHU, telecommands implementation and verification, HK management and transmission to XGIS-DHU and Alert management. The logical connection between SuperModules and XGIS-DHU through C-BEE is shown in Figure 14.

6. XGIS ELECTRICAL ARCHITECTURE

Beside the 2 XGIS-Cameras, two 2 XGIS Supply Units (XSUs) and a DHU compose the XGIS instrument. The XSUs will be contained in two boxes each one supplying one XGIS-Camera. The electrical architecture of the

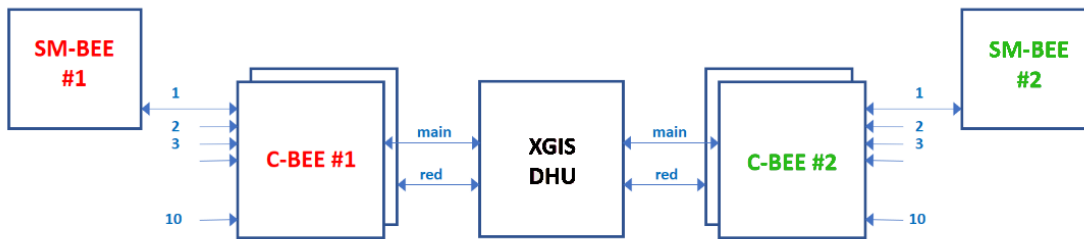


Figure 14. Logical connection between Super-Modules and XGIS-DHU through C-BEEs

XGIS is shown schematically in Figure 15 in which functional blocks of XGIS instrument and their interfaces with the THESEUS spacecraft platform are shown. Central element in the XGIS operation and data acquisition chain is the DHU that serves as telecommand/telemetry and power interface between the Spacecraft Service Module (SVM) and the XGIS-Cameras. The on-board burst trigger capability is implemented as a part of the DHU, which is directly interfaced with the on-board data handling (OBDH) system. The electrical interface is assumed to be SpaceWire. Each C-BEE is connected to the DHU for control, data, and health monitoring. The bus power is routed through the XSU power distribution unit providing ON/OFF switching and protection capability, with an overall power consumption of about 210 W (included margins) for each camera.

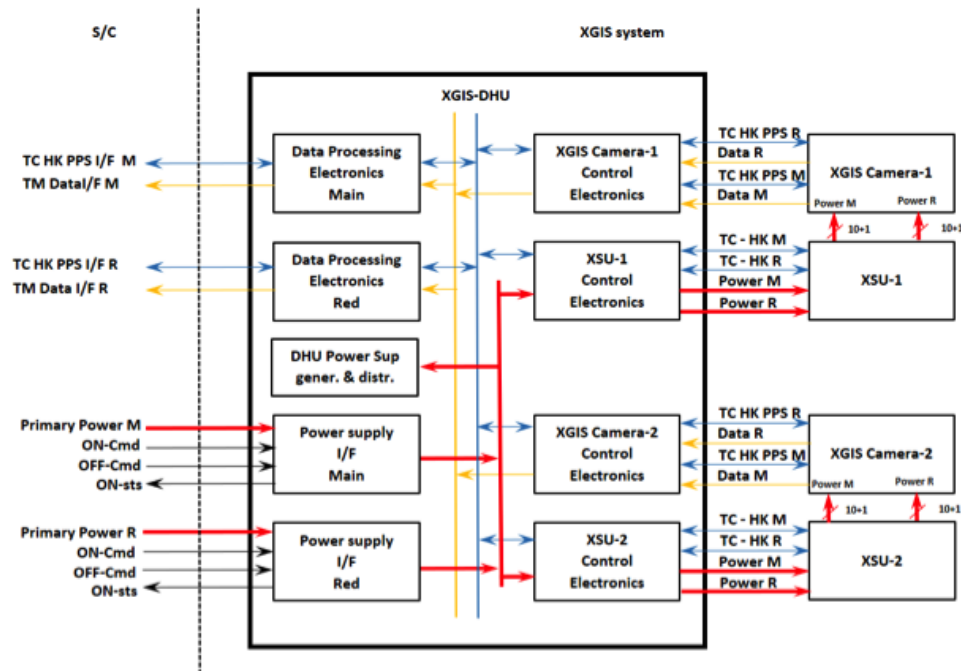


Figure 15. Functional block diagram of the XGIS system, consisting of 2 identical cameras. Each camera is made of 100 Modules organized in 10 Super-Modules), 2 power distribution boxes (XSU) and a Data Handling Unit (DHU) (in cold redundancy).

7. SUMMARY AND PROSPECTS

In this paper we have shown the main features of the XGIS on board THESEUS. In particular we have described the ASIC ORION-FE and ORION-BE which has been developed specifically for the THESEUS mission concept.

The concept of having the electronic chain split in two ASICs as in the LYRA FE and BE case has been tested with success in the context of the HERMES nano-satellite mission. First prototypes of the ORION-FE and ORION-BE ASICs have been assembled and are currently in testing and characterization.

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