IXPE ITALIAN CONTRIBUTION

Instrument User Manual

[OP-003]

Written by	***Responsibility***
Alessio Trois	Instrument GSE/AIV-T Manager
Antonino Tobia	Electrical Calibration Set-Up
Guido Parissenti	Senior System AIV/AIT
Verified by	
Daniele Brienza	Instrument PA Manager
Francesco Santoli	Italian PM
Approved by	
Ettore Del Monte	Instrument PO Manager
Paolo Soffitta	Italian PI
Luca Baldini	Italian Co-PI
Francesco Santoli	Italian PM
Pasqualino Loffredo	Italian Documentation Manager

CHANGE RECORDS

ISSUE	DATE	§ CHANGE RECORDS	AUTHOR
i01p00	18 Apr 2018	First issue for I-CDR	Antonino Tobia/ Alessio Trois
i02p00	15 Jun 2018	Par. 4.2.5 Updated (RID: 040-AA-003)	Antonino Tobia/ Alessio Trois
		Par. 4.4 Table 4.3 Updated with the TM description (RID: 036-AA-001)	
		added Par. 4.5 and Table 4.4 with telemetry report Vs Functional Mode	
		Par. 4.6 Table 4.5 Updated with the TC description (RID: 037-AA-001)	
		added Par. 4.7 and Table 4.6 with Telecommand Vs Functional Mode	
		added Par. 5.5.4 with the memories map (RID: 040-AA-004)	
		added Par. 5.5.5 with the patch/dump/checksum procedures (RID: 040-AA-006)	
i03p00	23 Mar 2020	The document has totally changed as result of phase C/D	Antonino Tobia/ Alessio Trois / Guido Parissenti
i04p00	14 May 2020	Added Reference documents RD11, RD12 and RD13 Added par 3.2 Instrument Flight Configuration Updated section 3.3.6 (FCW) Updated section 5.9.7 (FCW) Updated section 5.9.3 (DU Pixel Mask)	Alessio Trois
i05p00	11 Sep 2020	Updated section 3.3.6 (FCW) inverting clockwise/counter clockwise and FORWARD/BACKWARD FCW anomaly: Added reference to the document FCW FM1 ANOMALY REPORT (RD 14). Updated paragraph 5.3 and added par. 7.6.3 Update section 5.2.1 (boot mode, safe patch and	Alessio Trois / A. Tobia

		dump) Update section 7.2 (internal error conditions, software errors) Added par. 5.9.2.1 (DU BEE Setup Preset Retrieving) Added par. 5.9.3.1 (DU pixel Mask Preset Retrieving) Added par. 5.9.4.1 (DU BEE Alarm Preset Retrieving) Updated Table 1-1 and table 5-3 par 5.9.6(Default Voltage Operative Ranges and Nominal Vgem) after Instrument Bench Acceptance Test (August 2020) Updated MRAM configuration (ANNEX B.3): DU1_VGEM_E_MIN {DDD0018X} = -480V DU2_VGEM_E_MIN {DDD0018X} = -466V DU3_VGEM_E_MIN {DDD0018X} = -465V Update par. 3.3.6: Added Table 1-1b: Motor Steps from the fixed source position to align sources and GPD center	
i06p00	3 Mar 2021	Paragraph 5.3, removed: “Due to an anomaly to the FCW mounted on the DU FM3 (FCW serial number 1, RD [14]), the procedure described in par. 7.6.3 has to be executed immediately after a successful boot of the DSU both main or redundant section.” Removed par. 7.6.3 Par 5.4 : added the maximum length of a load TC. Added reference to the annex C.2	Alessio Trois

		Annex C.2: added the general ASW patch procedure	
i06p01	25 Mar 2021	Updated Table 1-3 page 67 (Vgem values) Updated Annex B.2 pages 106-107 (DU# Ki/Kp TEC/HOP values)	Alessio Trois
i07p00	6 Sept 2021	New issue in which we report some updates in the instrument configuration after the observatory TVAC test. • Updated section 3.3.6 table 3-1b • Updated section 5.9.6 with the latest HV nominal values and Vgem minimum operational value • Updated Annex B.3 with the latest Vgem minimum operational value • Updated Annex B.7 with the latest Pixel Masks configuration • Updated Annex B.8 with the latest FDIR configuration	Alessio Trois

TABLE OF CONTENTS

TABLE OF ANNEX

1. INTRODUCTION

1.1 Scope

IXPE (Imaging X-Ray Polarimetry Explorer) is an X-ray observatory chosen by NASA as next Astrophysics Explorers Program (SMEX 14). IXPE will measure the linear polarization of astronomical objects as a function of energy, time and, where relevant, position to improve the understanding of how X-ray emission is produced in objects such as magnetars, isolated pulsars, pulsar wind nebulae and supernova remnants, microquasars, active galaxies and supermassive black holes.
The mission, led by NASA's Marshall Space Flight Center (MSFC) in Huntsville (Alabama), is a joint collaboration with Italian Space Agency (ASI). IXPE will feature x-ray optics fabricated at NASA/MSFC and the strategical technology named Gas Pixel Detectors (GPD), provided in the framework of the IXPE Italian Collaboration (ASI, INAF and INFN).
The purpose of this document is to outline the user manual for the IXPE Instrument.

1.2 Applicability

This document is valid for IXPE Instrument EIDP.

1.3 Document Roadmap

Table 1-1: Roadmap for the IXPE Instrument User Manual

Chapter	Content
1	Introduction and scope
2	List of the documentation linked
3	Instrument Architecture
4	Instrument Handling and Transportation
5	Instrument Start-up and Configuration
6	Instrument Nominal Operation
7	Instrument On-board Monitoring and Contingencies
8	Annex A - Telemetries and Telecommands

9	Annex B - MRAM Default Configuration
10	Annex C - FDIR parameters
11	List of Acronyms

2. LINKED DOCUMENTS

2.1 Applicable Documents

[AD 1] 2509663 IXPE CONOPS

[AD 2] [DR 04] I2C-IAPS-IFF-ICD-001; DSU – DU Interface Document (Input to ICD-Instrument to Spacecraft document) (Issue 1)

[AD 3] I2C-OHBI-IOP-TEC-004; PFM DSU User Manual (Issue 2)

[AD 4] I2C-INFN-AIT-PRC-722; DU ISC Installation and Handling Procedure (Issue 1p02)

[AD 5] I2C-INFN-AIT-PRC-724; DU OSC Installation and Handling Procedure (Issue 1p01)

[AD 6] I2C-INFN-ISE-ICD-002; DU Electrical Interface Control Document EICD (Issue 6)

2.2 Reference Documents

[RD 1] [DR 01] I2C-IAPS-ISE-TEC-001; IXPE Instrument Design Description (Issue 2)
[RD 2] I2C-IAPS-ISE-TEC-004; Instrument Timing Management (Issue 1)
[RD 3] 2506879; IXPE Instrument to Spacecraft Interface Control Document Rev3
[RD 4] I2C-OHBI-ISW-ICD-002: IXPE Software Telemetry/Telecommand Definitions (issue 4)
[RD 5] I2C-OHBI-ISW-TEC-004: IXPE Instrument Flight Software Database (issue 5)
[RD 6] I2C-OHBI-IOP-TEC-003; IXPE Software User Manual (Issue 4)
[RD 7] I2C-INFN-ISE-TEC-004; DU User manual (Issue 3)
[RD 8] ECSS-E-70-41A
[RD 9] I2C-OHBI-ISE-ANR-002; IXPE Failure Detection, Isolation & Recovery (FDIR) (Issue 3)
[RD 10] I2C-IAPS-AIT-REP-010; Instrument E2E Test Report (Issue 2)
[RD 11] I2C-OHBI-IOP-TEC-001; DU FCW User Manual (issue 3)
[RD 12] 1560SE-005-1; IXPE MICD INSTRUMENT TO SPACECRAFT_PPR
[RD 13] I2C-OHBI-ISE-TEC-006; IXPE INSTRUMENT HARNESS DOCUMENT (issue 2)
[RD 14] I2C-OHBI-ISE-TEC-011; FCW FM1 ANOMALY REPORT (issue 1)

2.3 Standards/Handbooks

NA

3. INSTRUMENT ARCHITECTURE

3.1 Hardware

The IXPE Instrument comprises of three (3) identical Detector Units (DUs) and a (1) Detectors Service Unit (DSU). For the IXPE instrument development, testing and calibration we also define:

- Ground Support Equipment (GSE) for testing, mounting and logistics;
- Instrument Calibration Equipment (ICE) for End-to-End Instrument testing and calibration.

The IXPE Instrument product tree is reported in Figure 3-1, where the responsibility for the development and procurement of each item is identified.

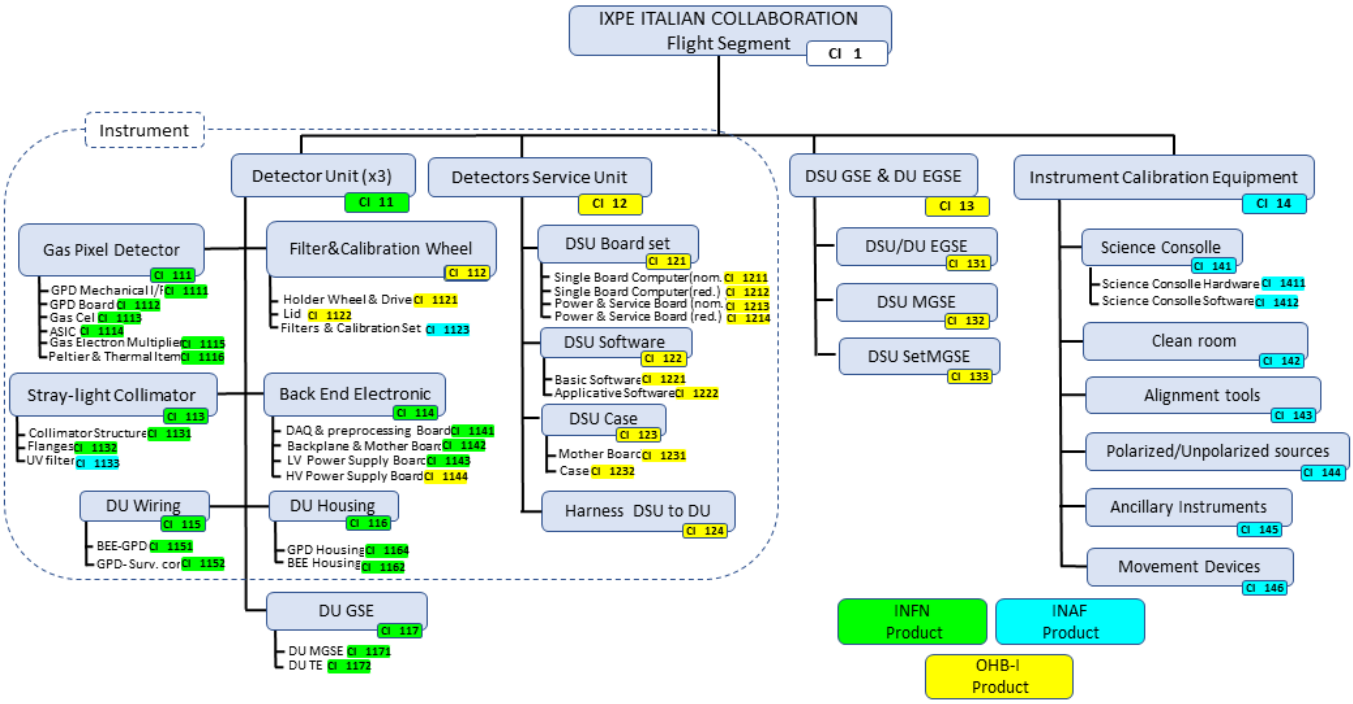


Figure 3-1: IXPE Instrument product tree.

The DU is the unit hosting the detector sensitive to polarization and the related electronic to power and interface the detector. Each DU comprises of the following sub-Units:

- a **Gas Pixel Detector** (GPD), which is an X-ray detector with gas as absorption medium and a custom ASIC as readout electrode, specifically developed by INFN-Pisa in collaboration with INAF-IAPS for X-ray polarimetry. The thermal environment is controlled by means of a Peltier.

- a **Filter & Calibration Wheel** (FCW), which host calibration sources and filters for specific observations, which can be placed in front of the GPD when needed.
- a **Back-End Electronics** (BEE), which comprises of electronics boards to manage the GPD ASIC and provides it with the required HV lines.
- a **Stray-light Collimator** (STC), which is used to avoid, together with X-ray shields mounted around mirrors, that X-ray photons coming from outside the mirror field of view can reach the sensitive volume in the GPD.
- a **DU Housing** (DUH), which provides the mechanical and thermal interface of the DU to the S/C.
- a **DU wiring** (DUW), which provides the electrical interfaces (internal to the DU) between the BEE and the GPD.

The DSU is the unit which provides the DU with the needed secondary power lines, controls and powers the FCW, formats and forwards the scientific data of the three DUs to the spacecraft. The DSU comprises of the following sub-Units:

- a **DSU Board Set** (DBS), which is the set of electronic boards (both nominal and redundant) which performs the DSU tasks.
- the **DSU Software**, which comprises the software which will run in the DSU.
- a **DSU Case** (DSC), which provides the electrical interface among the DSU boards and the mechanical and thermal interface of the unit.
- the **Harness DSU to DU**, which comprises the cables necessary to electrically interface the three DUs to the DSU.

3.2 Instrument Flight Configuration

Table 3-1 describes the Instrument flight configuration on board the IXPE mission.

Table 3-1 Instrument Flight configuration

Instrument Flight Configuration				
DSU-PFM physical set of connectors [RD 13]	**DU Flight Model**	**DU-FM top deck position [RD 12]**	**DU-FM physical Set of Connectors [RD 13]**	**Harness and connectors [RD 13]**
J07	DU FM2	DU# 1	J16	P16/DATA01/P7
J08			J17	P17/PWR01/P08
J09			J18	P18/FCW01/P09
J10	DU FM3	DU# 2	J16	P16/DATA02/P10
J11			J17	P17/PWR02/P11
J12			J18	P18/FCW02/P12
J13	DU FM4	DU# 3	J16	P16/DATA03/P13
J14			J17	P17/PWR03/P14
J15			J18	P18/FCW03/P15

3.3 Detector Unit

The DU (see Figure 3-2) is based on a Gas Pixel Detector (GPD) designed to detect the incident X-rays and measure energy, impact position and arrival time of each photon, as well as ejection direction of the photoelectron to be able to measure, on a statistical basis, polarization degree and angle of astrophysical sources. A block diagram of the DU is in Figure 3-3.
It is designed to be a compact unit to fit in the available space on the top deck of the satellite. It contains in a single unit both the detector and its readout and conditioning electronics (low and high voltages distribution), as well as FCW for on orbit calibration monitoring. It is organized in two boxes, the top one contains the detector, its thermal control, and the FCW: the top cover holds the wheel on the bottom side (with sources at the right distance from the detector) and the motor and control electronics on the external side (with dedicated connector directly to the DSU). A collimator, to reduce background photons

on the detector, is also attached to the top cover, as well as a UV filter. The second box is placed just below the GPD one and contains all the BEE boards. This configuration minimizes the distance (therefore the cable length) between the detector and its readout electronics and allows all the cables to be inside the box. The advantages are easy handling and no risk (high voltage or radiation) for the operators.

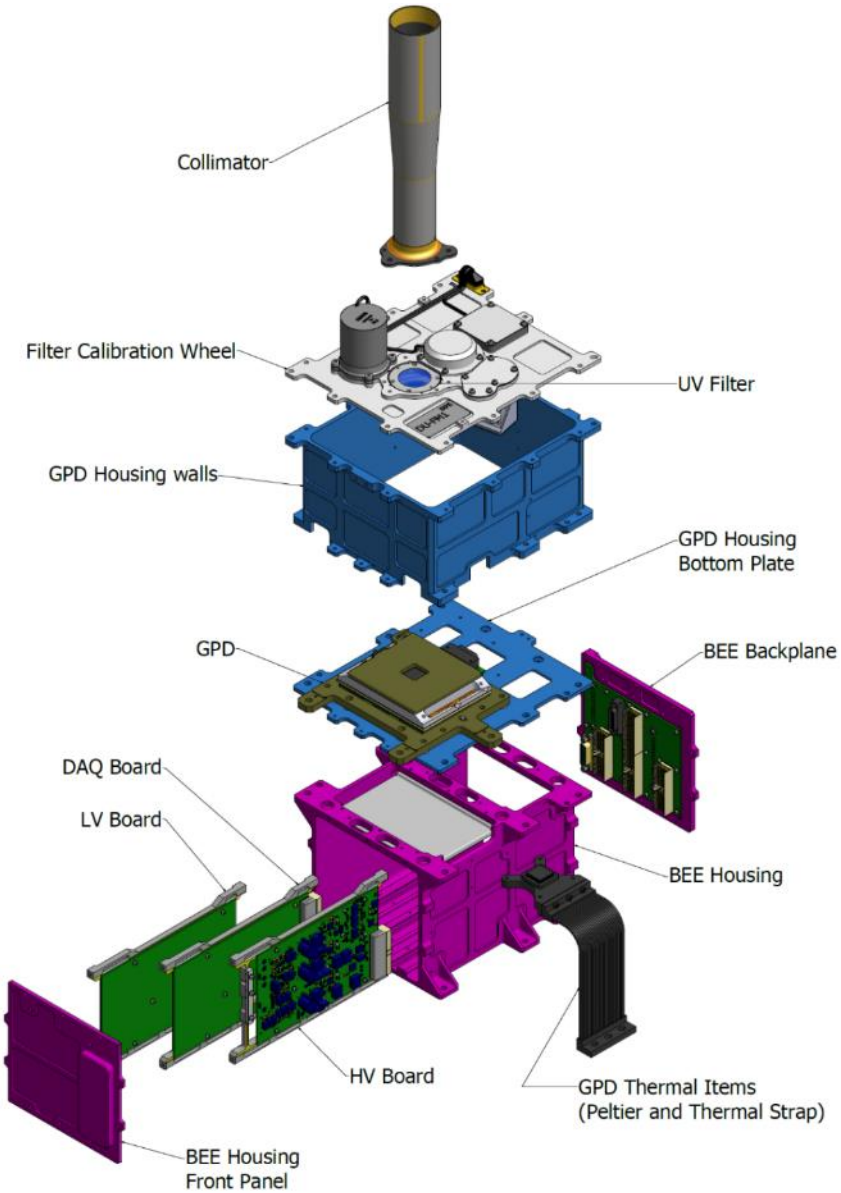


Figure 3-2: Exploded view of the IXPE DU.

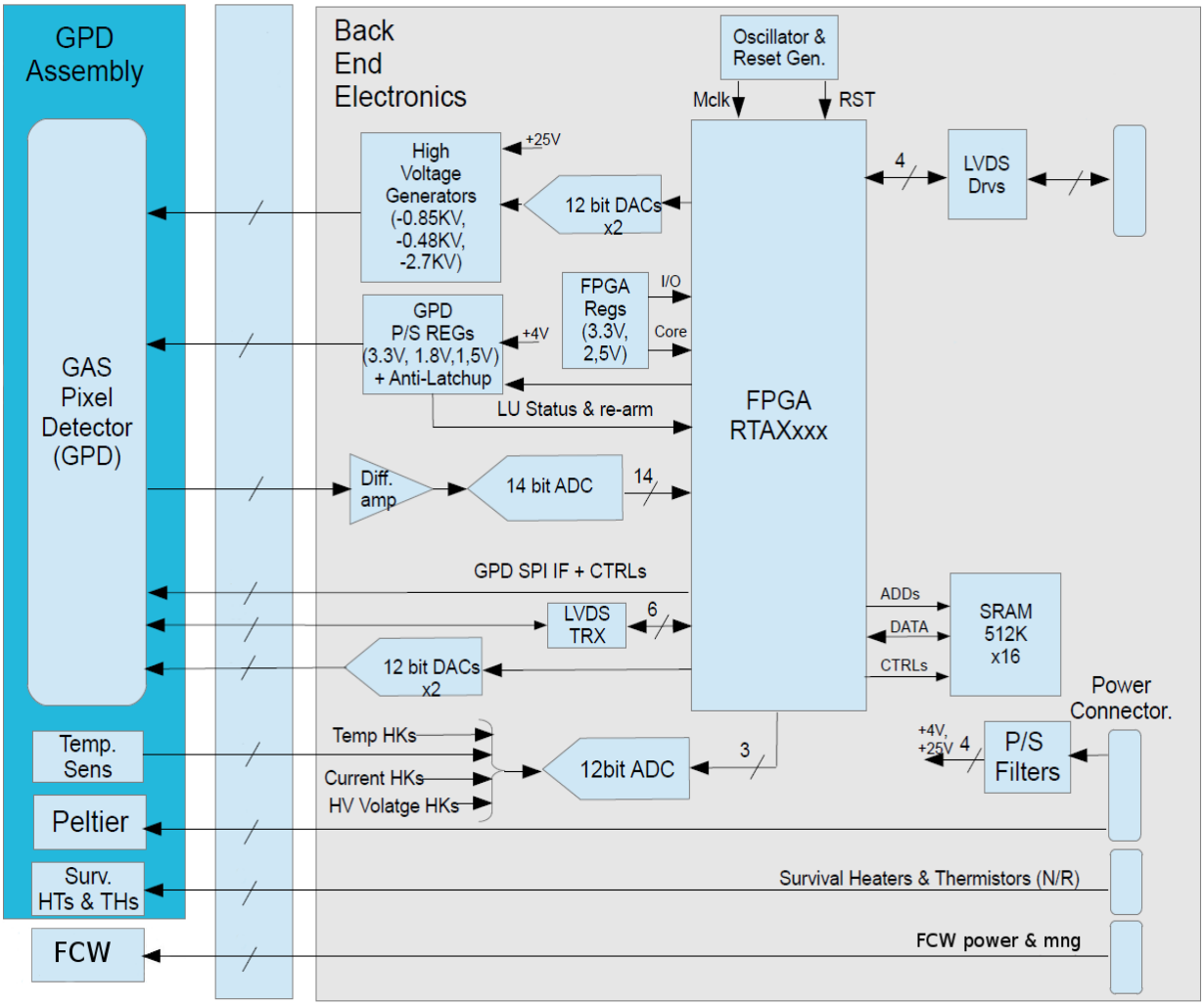


Figure 3-3: DU block diagram.

3.3.1 The Gas Pixel Detector

The Gas Pixel Detector (GPD) is a micro-pattern gas detector, where the gas amplification is provided by a Gas Electron Multiplier (GEM), a thin dielectric foil metalized on both sides and etched with a regular pattern of holes, and the signal is readout from a matrix of 105k pixels (300x352 pixels arranged in a 50 µm pitch triangular pattern) of a dedicated, custom CMOS ASIC.

The GPD assembly concept is built around the ASIC. This is mounted on a Printed Circuit Board inside a commercial ceramic package that acts as the bottom parts of the sealed gas cell. The PCB in glued on top of a mechanical interface that contains also the alignment reference and works also as thermal interface. A first ceramic spacer (see Figure 3-4) defines a lower gas gap for the drift of the electrons amplified by

the GEM glued on top of it. A second ceramic spacer defines the X-ray absorption gas gap, under a top titanium frame with a beryllium window. The basic building blocks of the GPD assembly and their functions are schematically illustrated in Figure 3-4 and are:

- a mechanical interface (*GPD Mech. I/F*), which supports the GPD unit, connects it to the focal plane and provides references for alignment with the MMA.
- a printed circuit board (*GPD Board*), integrating the readout ASIC which connects the GPD to the readout electronics.
- a ceramic spacer (*GEM Support Frame*), supporting and insulating the GEM from the GPD Board.
- the GEM foil (*GEM*), including four soldering pads for the high voltage connections.
- a ceramic support (*Drift Spacer*), which defines the X-rays absorption gas cell above the GEM and isolate the GEM from the top electrode.
- a titanium frame (*Ti frame and Be window*) which closes the gas cell and allows X-rays into the GPD through the integrated thin, optical-grade beryllium window, it also work as drift electrode.
- a filling tube of OFHC copper and its fixture to the titanium frame (*tube and fixture*).

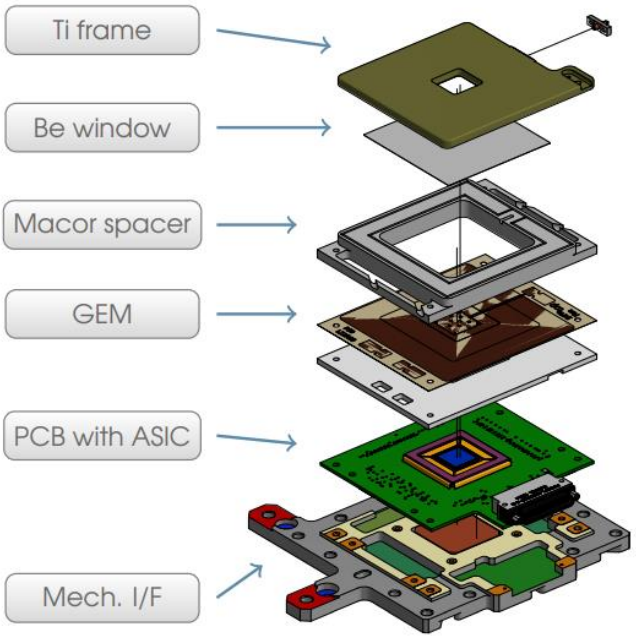


Figure 3-4: Schematic representation of GPD assembly.

Three high voltages are required by the GPD: on the top electrode (for the electric field in the detection/drift region, V_{drift}), on the bottom and top of the GEM (V_{bottom} and V_{top}, to set the multiplication gain, and the field in the transfer gap between GEM and ASIC).
The small pitch of the ASIC and the GEM are key for a good image of the photoelectron track (see Figure

3-5). To minimize track blurring a gas mixture based on DME has been selected and pressure is optimized in the energy range of interest. The projection of the track is analyzed to reconstruct the point of impact and the original direction of the photoelectron.

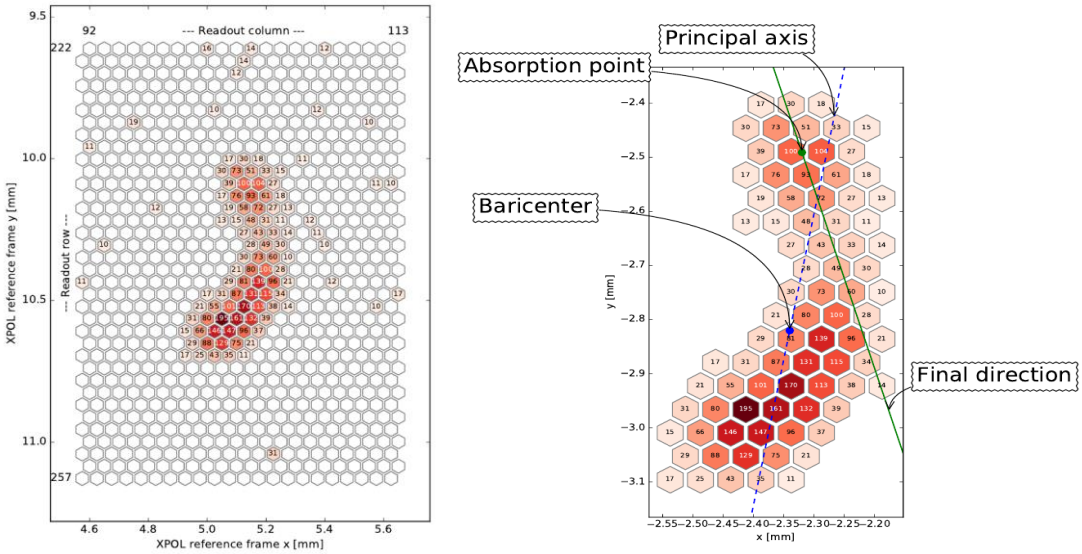


Figure 3-5: Real photoelectron track at 5.9 keV. Raw image (left) is first cleaned of noisy and isolated pixels and then analyzed to reconstruct photon absorption point and photoelectron direction of emission.

The linear polarization is determined from the angular distribution of the photoelectron tracks, named modulation curve. If the radiation is polarized, the modulation curve shows a cosine square modulation, whose amplitude is proportional to the degree of polarization and whose phase coincides with the angle of polarization.

3.3.2 Back-End Electronics

The Back-End Electronics (BEE) is the set of electronic boards that provide power (low and high voltage) to the GPD, control the ASIC functionalities, digitize the analog signal from the ASIC, manage the housekeeping, counters and timing signals for science analysis. The BEE is controlled by the DSU that provides 2 power voltages (5V and 25V), 2 communication channels (one for commands and housekeeping, the second for scientific data), timing signal (1-pps and 1MHz clock) and auxiliary signals. The DSU controls directly thermal hardware of the GPD, but the hardware lines go through the BEE power cable to minimize the number of connectors to the DU.
The BEE is composed of 4 electronic boards:

- a Data Acquisition board (DAQ board), for data acquisition and ASIC commands.

- a Low Voltage Power Supply board (LVPS board), to generate all the required voltages for GPD and BEE.
- a High Voltage Power Supply board (HVPS), for the generation of the GPD high voltages.
- a backplane (BP board), to distribute all signals among the board, with the GPD and with the external control equipment.

3.3.3 DAQ board

The DAQ board is based on a FPGA (RTAX2000) that takes care of all the digital function of the board, in particular:

- ASIC configuration management and readout.
- signal digitization management, via a dedicated space-qualified ADC.
- event formatting and on board zero suppression.
- rate and counters management, for lifetime measurement and diagnostic counters.
- communication with DSU via 2 digital interfaces:
  - Command Control Interface (CCI) for commands and housekeeping based on SPI protocol.
  - Science Data Interface (SDI) for event packets to the DSU.
- housekeeping management, for voltages, current and temperature readout.

A schematic representation of the functional blocks of the DAQ board is in Figure 3-6.

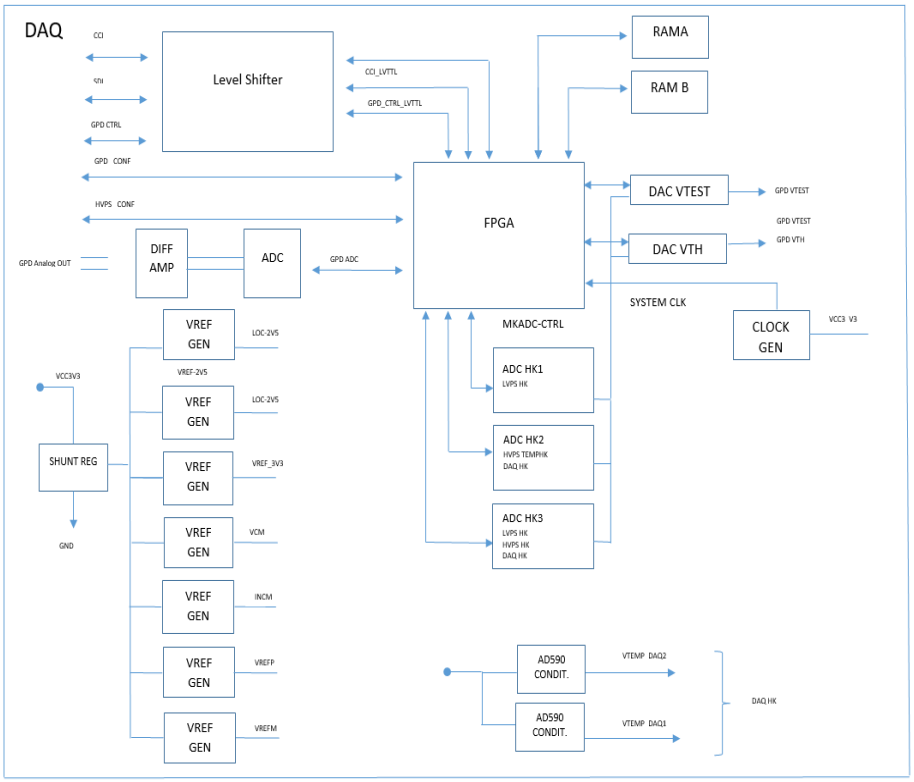


Figure 3-6: Functional blocks of the DAQ board.

Time tagging is done by the FPGA exploiting two signals from the DSU, a 1-pps signal (from the GPS or synthetized by the DSU itself) and the 1 MHz signal for microsecond. The FPGA implements 2 x 32-bit counters, for seconds and microseconds. The "seconds" counter is incremented at the rising edge a 1-pps signal received from the DSU. The "microseconds" increments at the rising edge of an external 1 MHz Ultra Stable clock signal and reset at the rising edge of the external 1-pps. See Section 7 for more details. As already mentioned, the DAQ Board is controlled by the DSU, that can read/write its registers and send commands via the CCI. This interface is based on SPI protocol with 8-bit data as basic unit and 1 parity bit. CCI is used by the DSU to access DU register bank, which is 16 bits wide and up to 128 registers deep. High Voltage control is done by the DSU via the FPGA in the DAQ board, which, in turn, writes the DAC on the High Voltage board.

3.3.4 High Voltage Power Supply Board (HVPS)

The GPD needs three negative high voltages to operate. Two of them are applied to the bottom and top electrodes of the GEM, and they are named V_{bottom} (or V_b) and V_{top} (or V_t), respectively; these are required to generate the electric field in the GEM holes and multiplicate the primary charges produce by the photoelectron. The third high voltage, applied to the GPD window, is necessary to generate the drift field in the gas cell. Two additional high voltage lines (rings) are generated on the HVB starting from the GEM

voltages (V_t and V_b) by using high voltage resistors.

The three HV values control different parameters of the GPD. In particular:

- The difference between V_{top} and V_{bottom} sets the GEM gain. An excessive difference between the HV values of the GEM bottom and top may cause disruptive discharges. A typical value is $|V_{top}-V_{bottom}|$= |(-870 V) - (400 V)| = 470 V. The maximum voltage difference before disruptive discharges is $|V_{top}-V_{bottom}|$=510 V.
- The value of V_{bottom} sets the drift field in the region between the GEM and the ASIC (which is at 0 V). In this case, we want a high drift field to increase the fraction of the charge that after multiplication is eventually collected by the ASIC. A typical value is -450 V.
- The difference between the V_{drift} and V_{top} sets the drift field in the GPD sensitive volume. A typical value is $|V_{drift}-V_{top}|$= |(-2670 V) - (-870 V)| = 1800 V.

3.3.5 Low Voltage Power Supply Board (LVPS)

This board takes as input the 5V from the DSU and generated all the 4 required voltages for the DU:

- 1.5 V for FPGA core.
- 1.8 V for ASIC analog circuitry.
- 3.3 V for all digital circuitry.
- 5 V as main voltage.

Each line includes a DC/DC converter and a current sensor for power consumption monitoring (no DC/DC for 5 V output obviously). Temperature sensors (AD590) are placed close to critical components and read with the dedicated ADC on the DAQ board.
There is no power-up command: once the DSU turns up the 5 V, all the voltages are on together and the BEE is powered up. Note: the 25V aren't connected to the BEE but directly to the HVB, and that's the reason why power-up and power-down sequences are fixed.

3.3.6 Filter and Calibration Wheel (FCW)

The FCW [RD 11] hosts filters and calibration sources which will be placed in front of the GPD to calibrate the detector or to perform peculiar observations. The position of the FCW will be commanded before each observation. The FCW will have 7 positions, corresponding to open position, close position, gray filter, calibration source A, B, C and D. FCW 3D CAD views are shown in Figure 3-.

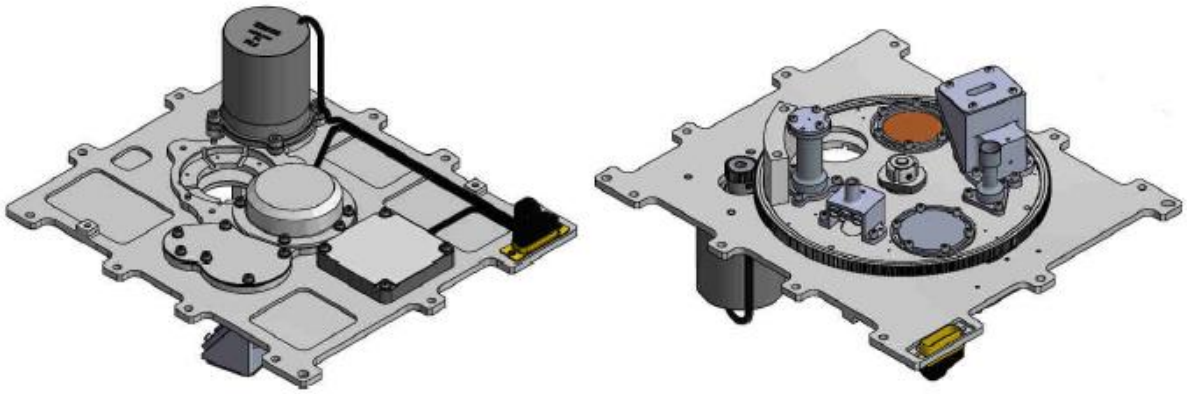


Figure 3-7: FCW CAD model (top view on the left, bottom view on the right)

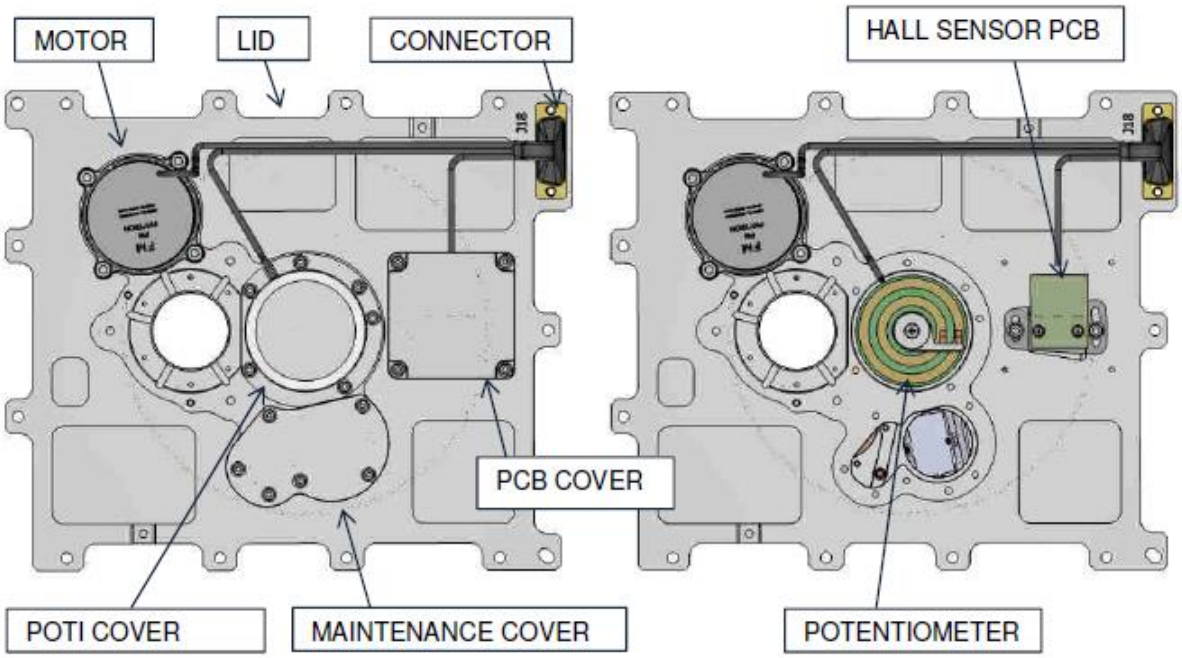


Figure 3-8a: Top View ((covers not shown on the right).

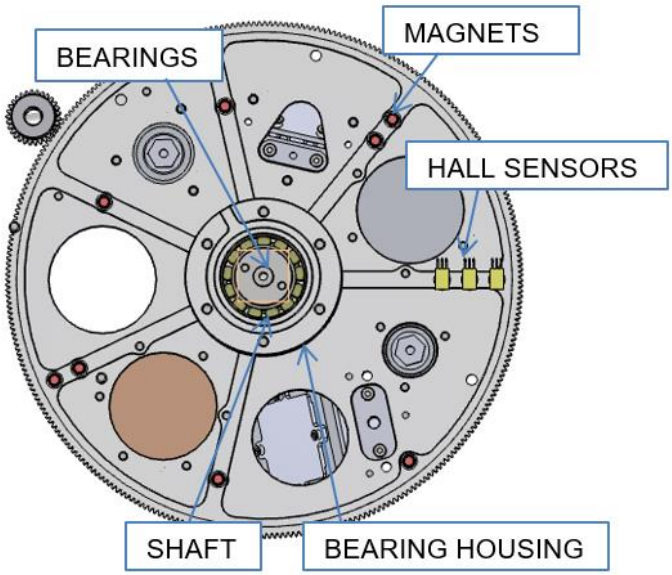


Figure 3-8b: Top view (lid, potentiometer and PCB not shown).

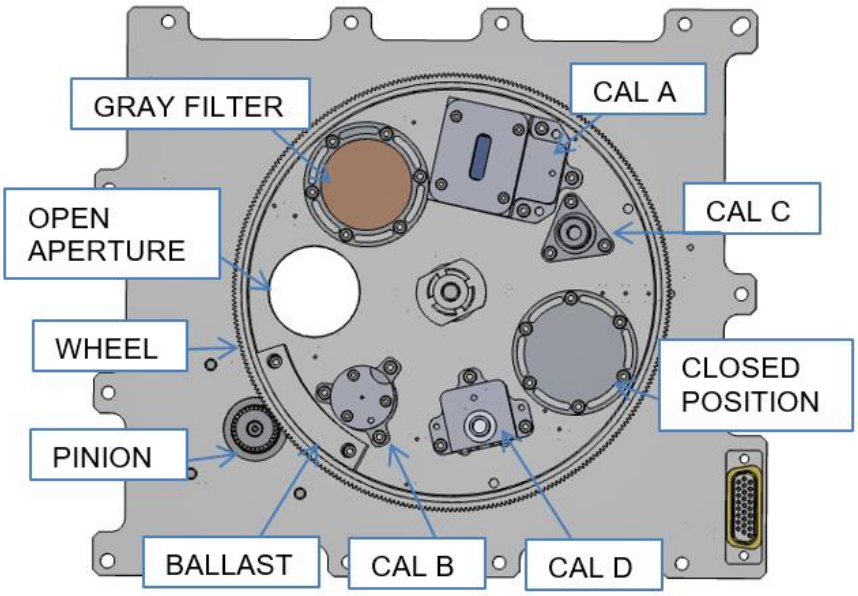


Figure 3-8c: Bottom View

Figures 3-8a, 3-8b and 3-8c show details of the FCW from bottom and top view.
Hall Effect Sensors are used as non-contact switches to stop the Wheel rotation to the requested position commanded by the DSU.

Three sensors are needed to identify seven Wheel positions. These sensors are accommodated on a spacer that is screwed to a customized PCB. The sensors are accommodated inside recessed pockets that defines the relative position.

The Baseline Operation is to alternate rotation direction in order to balance the wear on the FCW mechanisms and to reduce the total number motor steps, thereby maximizing the life of the FCW motor. From the fixed position, it is possible to move the FCW step by step to positioning the sources exactly on top of the centre of the GPD (see table 3-1b).

If it is assumed to consider the open position as the reference position, the operations should move BACKWARD (clockwise from the top view) to reach the Gray Filter, CAL A and CAL C positions and then to move FORWARD to go back to the Open position.
With the same approach, the FCW should be moved FORWARD to reach CAL B, CAL D, and Closed positions and BACKWARD to return back to Open.

Table 3-1a: Direction of the baseline operation

START	**END**						
	OPEN	**GRAY**	**CAL_A**	**CAL_C**	**CLOSED**	**CAL_D**	**CAL_B**
OPEN	-	BACKWARD	BACKWARD	BACKWARD	FORWARD	FORWARD	FORWARD
GRAY	FORWARD	-	BACKWARD	BACKWARD	BACKWARD	FORWARD	FORWARD
CAL_A	FORWARD	FORWARD	-	BACKWARD	BACKWARD	BACKWARD	BACKWARD
CAL_C	FORWARD	FORWARD	FORWARD	-	BACKWARD	BACKWARD	BACKWARD
CLOSED	BACKWARD	FORWARD	FORWARD	FORWARD	-	BACKWARD	BACKWARD
CAL_D	BACKWARD	BACKWARD	FORWARD	FORWARD	FORWARD	-	BACKWARD
CAL_B	BACKWARD	BACKWARD	BACKWARD	FORWARD	FORWARD	FORWARD	-

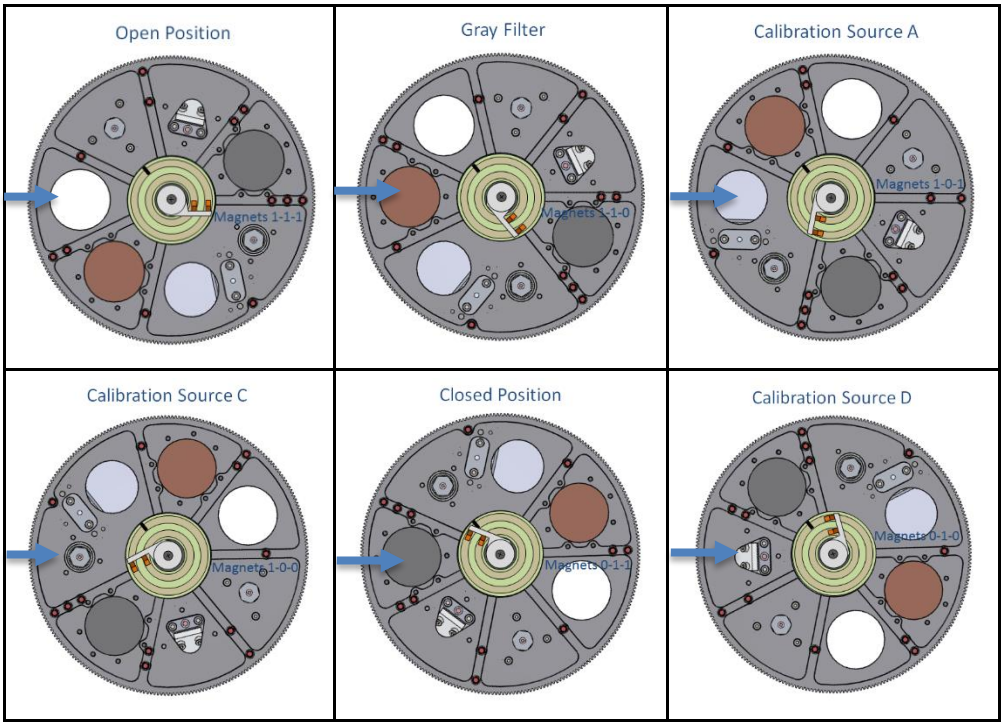
Table 3-1b: Motor Steps from the fixed source position to align sources and GPD center

DU#	**Item**	**Source Cal A**	**Source Cal B**	**Source Cal C**	**Source Cal D**
1	DU1 (DU-FM2)	4 forward	5 forward	0	0
2	DU2 (DU-FM3)	1 backward	2 backward	0	0
3	DU3 (DU-FM4)	0	2 forward	0	0

Using as reference the Open position the potentiometer nominal resistance is given in Table 3-2.

Table 3-2: Wheel position parameters

Pos.	Item	Potentiometer Values			Magnets			Angle (deg)		Motor steps	
		DU1 (DU FM2)	DU2 (DU FM3)	DU4 (DU FM4)	A	B	C	Abs	Rel	Abs	Rel
1	Open	1.66 V	1.70 V	1.68 V	1	1	1	0 (360)	51.5	0 (2000)	286
2	Gray Filter (Be-Filter)	2.39 V	2.42 V	2.40 V	1	1	0	51.4	51.4	286	286
3	Calibration Source A	3.11 V	3.14 V	3.13 V	1	0	1	102.8	51.4	571	285
4	Calibration Source C	3.83 V	3.86 V	3.85 V	1	0	0	154.2	51.4	857	286
5	Closed (W-shield)	4.56 V	4.59 V	4.58 V	0	1	1	205.6	51.4	1142	285
6	Calibration Source D	0.20 V	0.25 V	0.23 V	0	1	0	257	51.4	1428	286
7	Calibration Source B	0.93 V	0.98 V	0.95 V	0	0	1	308.5	51.5	1714	286



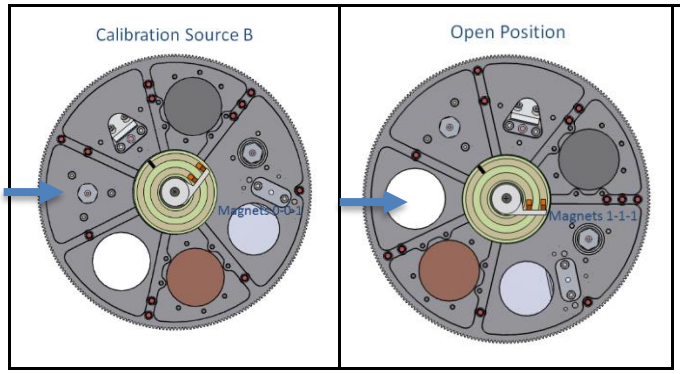


Figure 3-9: Wheel Positions (top view) rotating backward direction.

3.3.6.1 Filters and Calibration Set

The Filters and Calibration Set (FCS) comprises the items which can be alternatively put in front of the GPD by rotating the FCW. There are:

1. **Open position**. In this position no filter is put in front of the detector. The open position will be the standard one used for science observations. Only in case the source to observe is expected to be exceptionally bright (flux higher of about 4 10^{-8} erg/cm^2/s, or 2 Crab), the use of the gray filter described below will be recommended to reduce and better control the measurement dead time.
2. **Close position**. In this position a black filter, that is, a filter which is opaque to the radiation of interest, is placed in front of the detector. Mechanically, the filter will be a disk of aluminum 3 mm thick, which provides a transmission lower than 10^{-5} at 12 keV.
3. **Gray filter**. In this position a filter partially opaque to the radiation to be observed is used. As a baseline, the filter will be made of Beryllium and 0.25 mm thick; in this case, the counting rate in the energy range 2-8 keV (1-12 keV) for a Crab-like spectrum will be reduced of a factor about 4.
4. **Calibration source A (Cal A)** This source will produce polarized X-ray photons with precisely-known energy and polarization state, to monitor the modulation factor of the instrument at two energies in the IXPE energy band. A single ^{55}Fe nuclide is used. X-rays from ^{55}Fe at 5.9 keV and 6.5 keV are partially absorbed by a thin silver foil mounted in front of the ^{55}Fe nuclide to produce fluorescence at 3.0 keV and 3.15 keV.
5. **Calibration source B (Cal B)**. This source produces a collimated beam of unpolarized photons, to monitor the absence of a spurious modulation. A ^{55}Fe radioactive sources glued in a holder and screwed in a cylindrical body. At the other end of the body, a diaphragm with an aperture of 1 mm collimate X-rays to produce a spot of about 3 mm on the GPD such a spot has a size which is representative of the source image of a point-like source when the spacecraft pointing jitter is included.
6. **Calibration source C (Cal C)**. This source illuminates all the detector sensitive area to map the gain at one energy. This source will be composed of a ^{55}Fe iron radioactive source, glued in a holder

which is screwed in a body. A collimator allows X-ray photons to impinge on the detector sensitive area only when the source is in front of the GPD.

7. **Calibration source D (Cal D)**. This source illuminates all the detector sensitive area as Cal C, to map the gain at another energy. Cal D is based on a ^{55}Fe source, glued in an aluminium holder which illuminates a Si target mounted on a body to extract Kα fluorescence from Calcium at 1.7 keV, which impinges on the detector.

3.3.7 Stray-light collimator (SLC)

A stray-light collimator (STL) shield the GPD from background X-ray not coming from the optics. Figure 3-7 shows a drawing of the current design of the SLC.
At the bottom of the SLC, a UV filter is mounted to prevent UV photons entering in the DU.
Basic characteristics of the UV filter are:

- Free-standing filter, 1 µm thick polyimide, ≤50 nm aluminium on one side.
- Diameter: 31 mm Ø.
- Transparency >90% at 2.0 keV.

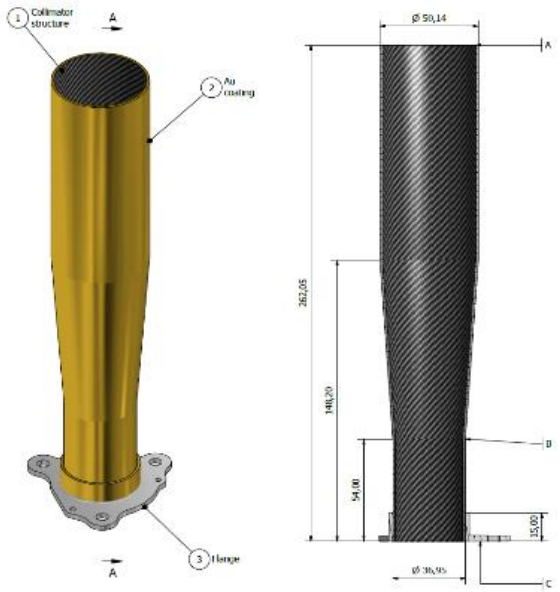


Figure 3-7: Drawing of the stray-light collimator.

3.4 Detector Service Unit

The Detector Service Unit (DSU) consists of two redundant boards and one backplane for internal DSU

signal routing:

- Single Board Computer (SBC)
- Power & Service Board (PSB)

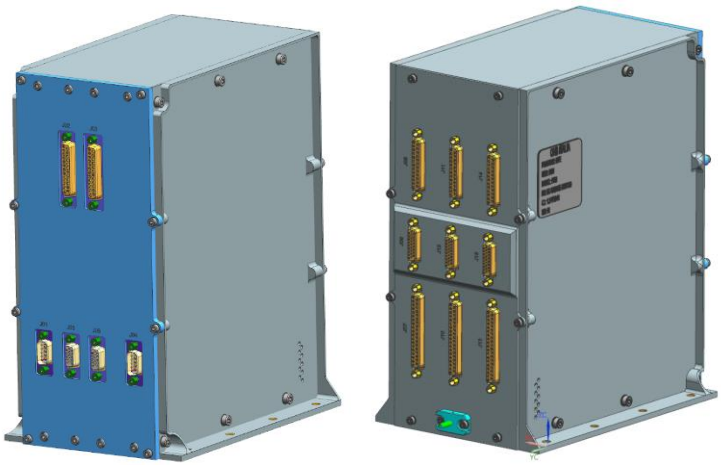


Figure 3-8: DSU mechanical box: front (left) and rear (right) view

Figure 3-8 reports the mechanical design of DSU and Figure 3-9 reports the proposed architecture of the DSU.

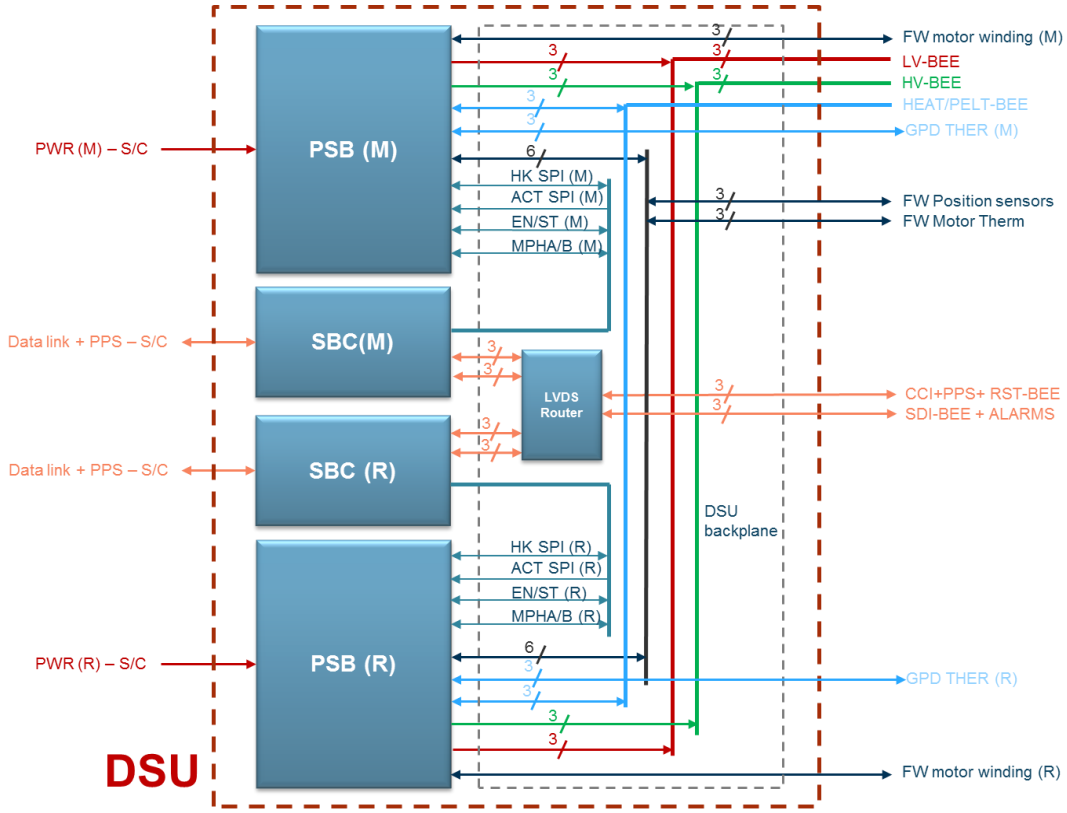


Figure 3-9: DSU architecture.

The SBC is in charge to implement:

- instrument control and configuration
- instrument data processing and formatting

The PSB is in charge to perform different tasks relevant to power management; in particular, this board hosts the following main functional blocks:

- Power converters aimed at generation of required supply voltages both for DSU electronics and DU
- Drivers for DU thermal actuators (heater and Peltier cells)
- Signal conditioning for RTD sensors dedicated to DU temperature control
- FCW motor drivers
- Signal conditioning for motor position sensors and temperature

DSU architecture supports redundancy philosophy based on cold-sparing approach.

Power outputs on the PSB dedicated to drive each DU power interface has been provided with output diodes in order to comply with cold-sparing approach. Consequently, each LV-BEE and HV-BEE power lines are driven by both PSBs. The only one exception is power I/F towards each FCW motor that is equipped with redundant coil for each motor phase. In this case the motor driver is not provided with output diodes.

For each motor phase, the main coil is connected to the main PSB motor driver and the redundant coil to the redundant PSB motor driver.
The same approach, adopted for I/F towards FCW motor, has been adopted for GPD temperature measurement; the GPD is provided with two temperature sensors. Only one sensor is used by the SBC S/W for GPD temperature control. For this reason, one sensor is connected to the main PSB and the other one to the redundant PSB.
Data interface between DSU and each DU consists of the following set of signal lines:

- Three Command and Communication Interfaces (CCI) for command transmission from DSU to each DU
- Three Serial Data Interfaces (SDI) for sensor data transmission from each DU to DSU
- Three reset lines, one for each DU
- Six input alarm lines, two for each DU, used for monitoring of secondary DU internal voltages
- Three output timing signals for DU internal acquisition timing verification

Physical layer of all signal lines between DSU and DU complies with LVDS standard. According to adopted redundancy philosophy, each set of the above reported signal connects one DU with both SBC inside the DSU.
The connection is implemented via the block LVDS router located onto DSU backplane. This block operates as signal repeater and its circuit configuration is based on the fact the LVDS drivers and receivers selected for DSU support cold-sparing operation.
A basic description of the Single Board Computer and Power & Service Board follows; mode details can be found in [RD 5].

3.4.1 Single Board Computer (SBC)

The Single Board Computer is devoted to the instrument management, S/C data communication and hosts the applicative SW.
The SBC main tasks are the following:

- Manage the payload operational modes.
- Implement the instrument FDIR functions.
- Manage the three interfaces (TC/TM, PPS, SC Data) to the three DUs.
- Manage interfaces (CMDs & TOD, PPS, H&S, SC Data) with the S/C.
- Retrieve science data and housekeeping data from the BEE, compress and format them and provide them to the On-Board Data Handling system (OBDH) in the S/C.
- Manage the PPS signal and the time synchronization of the DUs.
- Manage the Filter and Calibration Wheels (FCW's)
- Drive the Peltier coolers and heaters that are used to control the temperatures of the GPDs and DU.

A companion FPGA, belonging to RTAX family by MICROSEMI, will be included to support the processor

operation and to provide management of data interfaces required by IXPE instrument and not included in the ASIC.
Single Board Computer (SBC) will be based on LEON3FT CPU. The proposed architecture is reported in Figure 3-10.

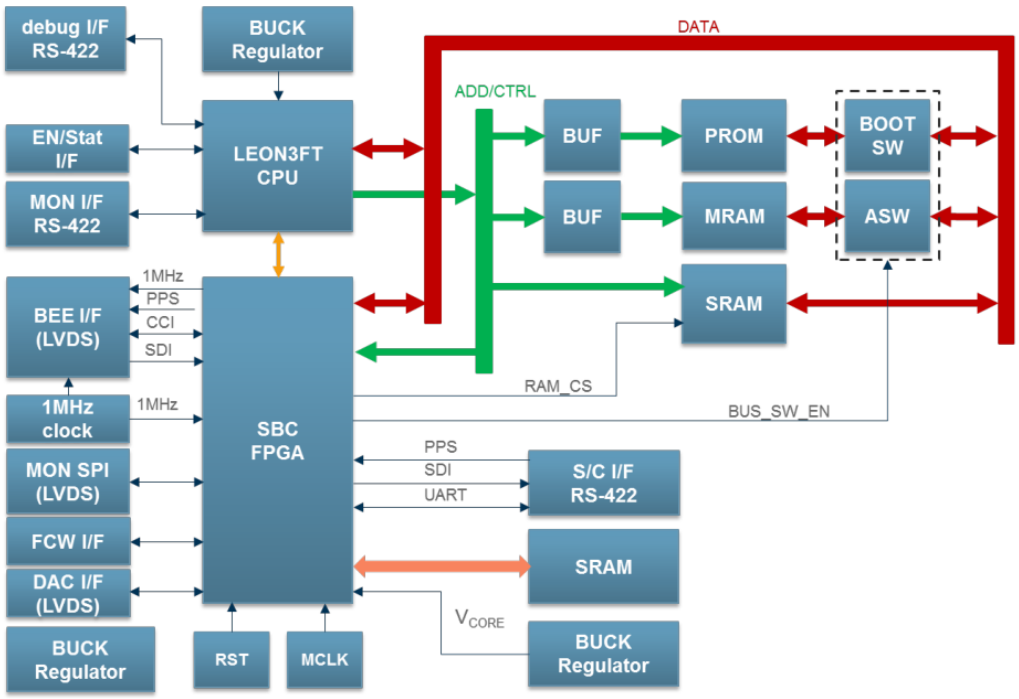


Figure 3-10: SBC block diagram.

3.4.2 Power & Service Board (PSB)

The PSB is in charge of generating regulated supply voltages for the SBC and for the DU items from the S/C unregulated bus voltage. The DSU interfaces the Spacecraft with two (one Nominal and one Redundant) unregulated power lines on separate connectors.
The nominal voltage of the power lines is +28 V. The architecture of PSB is reported in Figure 3-11.
The PSB tasks are:

- To convert the non-regulated primary power from the Spacecraft bus into regulated power supply lines for the three Detector Units.
- To drive the FCW's motors for the three DU units
- To drive the Peltier/Heater for the three DU
- To provide DSU HK data to the SBC via digital I/F (SPI)

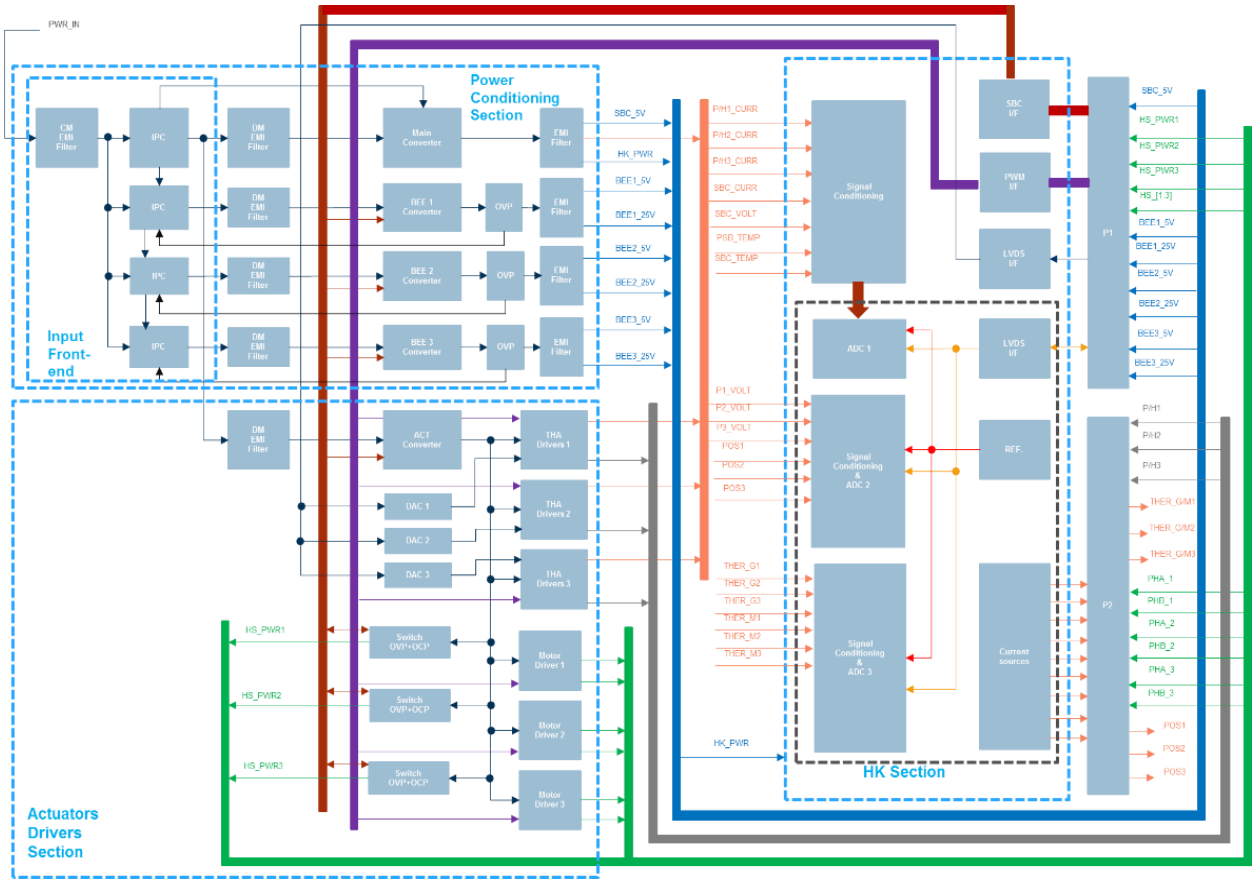


Figure 3-11: PSB architecture.

3.5 Software

The IXPE DSU On-Board Software is a software product running on the DSU (Detector Service Unit) computer and includes the software items:

- Basic Software (BSW)
  - Boot SW (BOOTSW)
  - Operating System (RTOS)
  - Hardware Dependent SW (HDSW)
- Application Software (ASW)

The main purpose of the IXPE DSU Application Software is to provide software functionalities that enable the ground operator to control and supervise the IXPE DSU and detectors operations. The high-level functionalities of the ASW encompass:

- DSU - S/C data interface management

- TC handling according to the defined standard
- TM handling according to the defined standard
- Power distribution Monitoring & Control
- Scientific data acquisition from the DUs and transmission to the platform
- Thermal Control and temperature sensors monitoring
- Distribution of the time and synchronization signals from S/C to DUs
- FDIR functions

The deployment diagram of Figure 3-12 shows the OBSW in the context of the entire IXPE instrument hardware. The figure illustrates the interfaces between the OBSW and the hardware and details the kind of data exchanged (i.e. information flow) over these interfaces with the other hardware and software components.

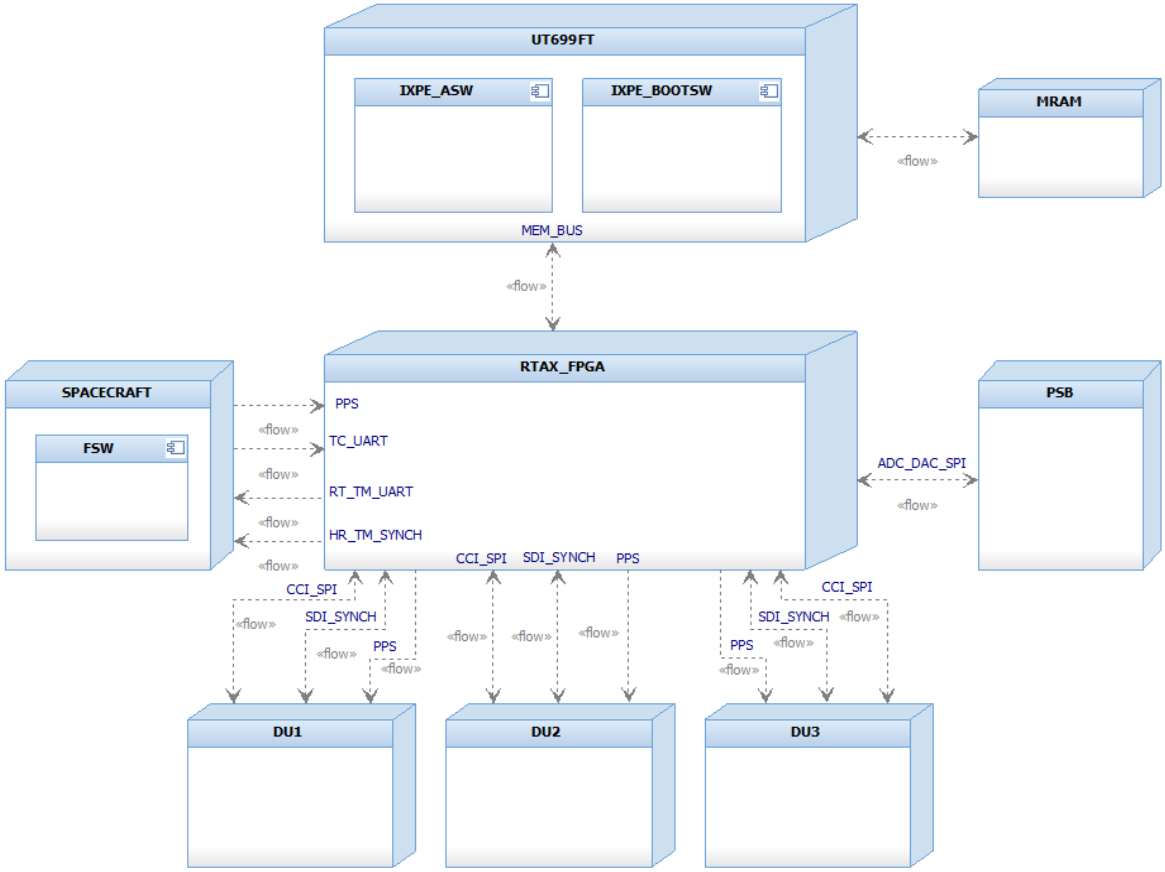


Figure 3-12: OBSW deployment diagram

The UT699FT, the RTAX_FPGA and the MRAM are composing the Detectors Service Unit (DSU). The ASW is running on the UT699FT module and it is interfaced with the other two main components of the DSU. The ASW receives telecommands and sends telemetries from/to the Spacecraft Flight Software (FSW) which is running on the satellite platform.

The communication with the other units of the IXPE instrument (i.e. the DUs and the PSB) is performed via SPI or synchronous links as depicted in the figure above.
The deployment diagram focuses on the main operational scenario where the application software is controlling the instrument. Nevertheless, the whole software running on the IXPE DSU is composed by several items as depicted in Figure 3-13 and listed in the following:

- BOOT SW: software in charge to load the ASW image in SRAM at instrument start-up (i.e. power on or reset) and then transfer control to the downloaded and verified ASW image. It also includes a maintenance mode to perform operations on instrument memories (e.g. load, dump, check).
- ASW: Main software component in charge of control the instrument behaviour, implement TC/TM interface.
- HDSW: Hardware Dependent Software in charge of allow the ASW to interact with the underlying hardware components.

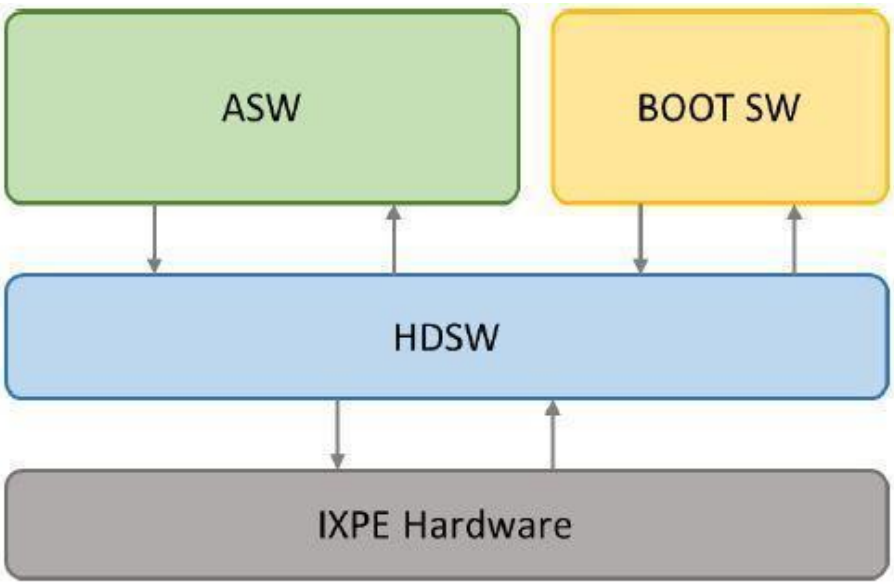


Figure 3-13: OBSW software components

The interaction between software items as arranged in Figure 3-13 is only in vertical direction. This means for example that the ASW only interacts with the HDSW directly and no direct interaction between the ASW and the Boot SW is established.

4. INSTRUMENT HANDLING AND TRANSPORTATION

4.1 General

All the handling and transportation activities of the equipment shall meet the following requirements:

- Handling and transportation shall be performed by authorized personnel and qualified in accordance with the relevant unit procedure.
- Manual handling and transportation of IXPE Units shall always be handled by at least two persons.
- The equipment shall always be transported using the related transport container, with protections to prevent shocks and to protect against hostile environmental conditions.
- The transport container shall be opened only in a clean room ISO 8 Class (100.000)
- The unit shall always be kept in a clean room when out of its transport container

4.2 DSU HANDLING AND TRANSPORTATION

For DSU Handling and Transportation procedures can be found in [AD6].

4.3 DUs HANDLING AND TRANSPORTATION

For DUs Handling and Transportation procedures can be found in [RD7].

5. INSTRUMENT START-UP AND CONFIGURATION

5.1 GENERAL

All IXPE Application Software operations are exploited by sending telecommands and receiving telemetries. Telemetries can be either replies to processed telecommands or unsolicited events notifications. Telecommands and telemetries formats are detailed in IXPE Software Telemetry-Telecommand Definitions [RD 4] and are compliant with the ECSS-E-70-41A [RD 8].
All telecommand are verified on-board at reception time (centralized check) and either a successful or unsuccessful command acceptance report telemetry is accordingly sent to ground. Additionally, either at start of execution or command execution completion (distributed check), a successful or unsuccessful report is sent to ground.
This is the list of verification reports generated by IXPE ASW:

- Successful command acceptance report (TM APID 1210)
- Unsuccessful command acceptance report (TM APID 1211)
- Successful command starts execution report (TM APID 1212)
- Unsuccessful command starts execution report (TM APID 1213)
- Successful command execution report (TM APID 1214)
- Unsuccessful command execution report (TM APID 1215)

The verification reports generated by each received telecommand and the reasons for unsuccessful reports are listed in ANNEX A.5.

5.2 OPERATIVE MODES

The IXPE Instrument operate in the following modes [RD6]:

- Boot (transitional mode)
- Maintenance
- Stand-By
- Observation
- SAA
- SAFE
- Reboot (transitional mode)

5.2.1 Mode Specifications

Boot mode is operated automatically when the DSU is power up.
ASW operative modes transitions are depicted in Table 5-1 . The list of telecommands to trigger a transition is:

- Enter STAND-BY mode (TC APID 1040)

- Enter MAINTENANCE mode (TC APID 1041)
- Enter SAA mode (TC APID 1042)
- Enter OBSERVATION mode (TC APID 1043)
- Enter SAFE mode (TC APID 1044)
- Reboot (TC APID 1045)

The SAFE operative mode is also entered autonomously by IXPE ASW upon FDIR action trigger regardless active operative mode. The Table 5-1 reports allowed operative modes transitions.

Table 5-1: Mode transition

		Destination State					
Current State		STAND-BY	MAINTENANCE	OBSERVATION	SAA	SAFE	REBOOT
	STAND-BY	▶	▶	▶	▶	▶	
	MAINTENANCE	▶	▶			▶	
	OBSERVATION	▶		▶	▶	▶	
	SAA	▶		▶	▶	▶	
	SAFE	▶	▶			▶	▶
	REBOOT						

All operative mode transition requests produce either an **Operative mode successful change report** (TM APID 1230) or an **Operative mode failed change report** (TM APID 1231).
Requesting an operative mode transition to the same operative mode doesn't produce an Unsuccessful command execution report, nonetheless the Operative mode successful/failed change report is not sent. A Successful command execution report is sent to ground.

5.2.1.1 BOOT

BOOT is the start-up mode at power on. A limited SW application, called Boot Software runs from the PROM in order to perform all the checks and the initialization of instrument resources and items.

The Boot Software loads (from MRAM memory to SRAM memory) and execute an Application Software image (code and configuration data).

The IXPE DSU BootSW consists of two logical stage:

- The first stage is composed by the Loader and INITSW SW components. It has in charge to initialize the CPU, perform the self-tests and activate the ASW or the BootSW second stage.
- The second stage is composed by Safe Patch and Dump (SafePD) SW component. It provides a minimal TC/TM interface to patch the ASW images and investigate the cause of a failure.

During the first stage the BootSW copies itself from PROM to the SRAM area before performing the self-tests.
After the self-test execution, if the identifier of ASW to load is valid and the ASW stored in MRAM is not corrupted, the first stage copies the ASW from MRAM to SRAM and activate it.
In case that the ASW selected can not be loaded, the SafePD (second stage) will be activated. More details can be found in RD [6]

The BootSW implements a mechanism whereby the ASW must confirm its correct execution before trigger a requested reboot telecommand (warm reset). To confirm its correct execution, the ASW must write a magic word to a fixed address in SRAM.
This procedure avoids losing control of the DSU section when the ASW has a failure during the execution so it cannot refresh the watchdog and the DSU enters in an infinite reboot loop (see par. 7.2).
When a warm reset occurs and the magic word is not set, the SafePD will be activated.
The magic word is reset to zero during the BootSW first stage.
The SafePD doesn't set the magic word because it will be always activated. See RD [6] for more details.

The ASW, once started, completes the initialization sequence execution by entering the instrument in STAND-BY mode or SAFE mode.
In the nominal case the ASW completes the initialization sequence execution by entering the instrument in STAND-BY.
The ASW enter in SAFE mode if some FCWs has been left not closed before the last power off or if a warm reset (watchdog reset) is triggered.
Report of the boot activities is stored into memory and delivered in telemetry (APID 1220).

5.2.1.2 MAINTENANCE

MAINTENANCE is reserved to support the in-orbit maintenance program. This mode can be reached on request when the DSU SW mode is in Stand-By and it is dedicated to memory management operations like code and data load/download in/from MRAM and SRAM.
The **Enter MAINTENANCE mode** operation allows to change operative mode to MAINTENANCE. The MAINTENANCE mode supports the following activities:

- Patch, dump and check DSU memories
- Set and get configurable parameters
- Handle the Time of Day message
- Handle the thermal regulation
- Collect, monitor and generate the housekeeping TM

5.2.1.3 STANDBY

Nominally, at the end of the bootstrap phase, the DSU moves in STANDBY mode to start the instrument monitoring and control. The Application Software runs from the SRAM and performs the data handling function.
The **Enter STAND-BY mode** operation allows to change operative mode to STAND-BY. The STAND-BY mode supports the following activities:

- Start and handle the thermal regulation
- Power on/off the instrument items
- Process allowed incoming TC and generate the related TM
- Handle the Time of Day message
- Handle the thermal regulation
- Collect, monitor and generate the housekeeping TM
- Configure the detector units and the science data processing.

5.2.1.4 OBSERVATION

From the point of view of the DSU, all instrument calibration and scientific modes are managed into an unique OBSERVATION mode that is preventively configured while in STANDBY mode. The DSU effectively apply entering the OBSERVATION mode so that the instrument can issue its science data and the DSU can start the science data processing.
The **Enter OBSERVATION mode** operation allows to change operative mode to OBSERVATION. The OBSERVATION mode supports the following activities:

- Handle the thermal regulation
- Handle the Time of Day message
- Collect, monitor and generate the housekeeping TM
- Enable scientific data generation

5.2.1.5 SAA

This mode is used when the instrument cross the South Atlantic Anomaly.
The **Enter SAA mode** operation allows to change operative mode to SAA. The SAA mode supports the following activities:

- Configure the HVs to low voltages
- Disable the science data generation
- Handle the Time of Day message
- Handle the thermal regulation
- Collect, monitor and generate the housekeeping TM

5.2.1.6 SAFE

This mode is used before to switch off the Instrument or to perform a SW reboot. Also, it is used to manage FDIR conditions.
The **Enter SAFE mode** operation allows to change operative mode to SAFE. The SAFE mode supports the following activities

- Preserve DUs and HVs status
- Collect, monitor and generate the housekeeping TM
- Generate death report TM

SAFE operative mode can be entered either by telecommand or FDIR action. When entered by telecommand its only purpose is to preserve current DUs and HVs status (i.e. no ramp-off or switch off are performed on hardware). When entered by FDIR action it can be selected if HVs ramp-off, DUs switch off and FCW rotation to CLOSE have to be performed (RECOVERY), or if the hardware status has to be preserved.
Only during the SAFE mode is possible to perform a reboot of the ASW (par 5.3).

5.2.2 Mode Transitions

The DSU control and manage the operating modes and their transitions according to the diagram in Figure 5-1

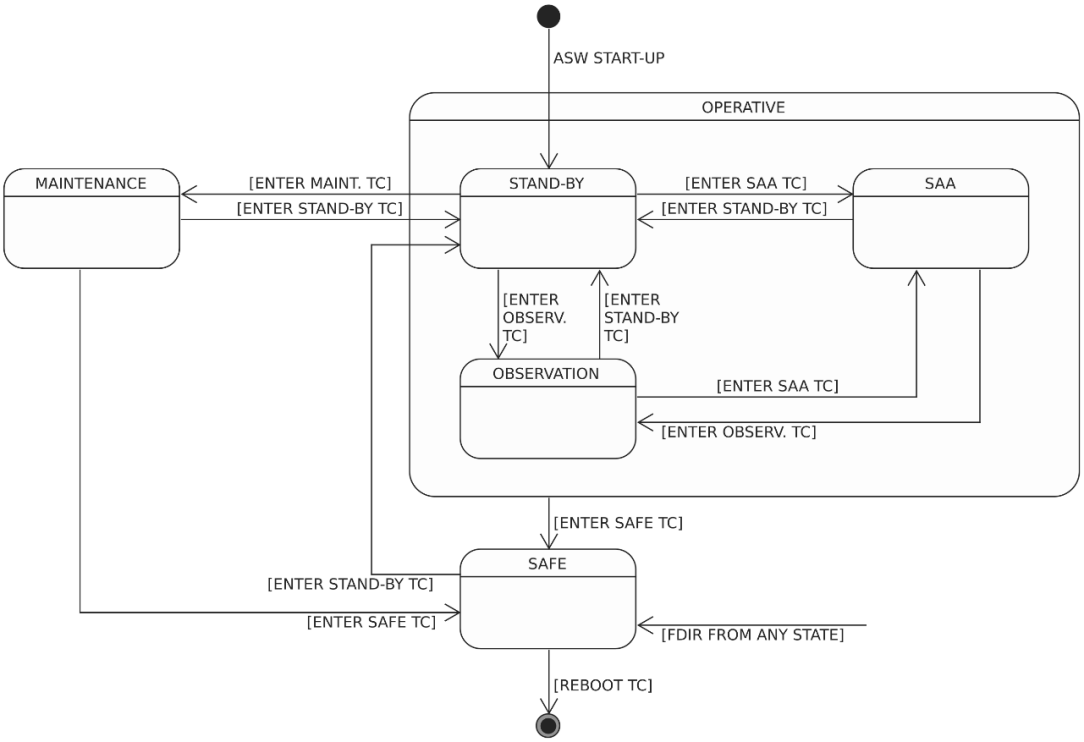


Figure 5-1: Transitions between DSU operational modes

5.3 DSU POWER ON AND REBOOT

At the DSU switch-on, after the BOOT SW activities described in paragraph 5.2, the ASW is loaded into SRAM end executed. The ASW checks the position of the Filters and Calibration Wheels and the status of the Detector Units and High Voltages Boards.
If the FCWs are closed and the HVBs are off the ASW moves to STAND-BY mode.
If the FCWs are no closed or if the HVBs are ON, the ASW performs the following action:

- moves the FCWs to CLOSED position
- performs the ramp-off procedure if HVBs voltages are greater than zero
- switch off the DUs
- moves SW operative mode to SAFE
- and switches-off the DUs, performing a ramp-off procedure if HVBs voltages are greater than zero.

The boot phase last around 60 seconds.
The RTOS tasks are then started by the ASW. The ASW start-up sequence completes by sending to ground the following telemetries:

- Boot report (TM APID 1220)
- ASW start report (TM APID 1221)

- Configurable parameters dump 1 (TM APID 1232)
- Configurable parameters dump 2 (TM APID 1233)

The Boot report is prepared by the BOOT SW as detailed in paragraph 5.2.

The ASW start report provides the following information:

- Initial operative mode (SAFE or STAND-BY depending by the status of the FCWs and DUs/HVBs)
- Active DSU board (MAIN or REDUNDANT)
- Status of +5V and +25V of the three DUs
- Status of the Vdrift, Vbottom and Vgem DACs of the three DUs
- Position of the three FCWs
- DSU FPGA, HDSW, ASW components and DB versions
- Task identifiers of all RTOS active tasks
- SRAM memory address to be used for testing purposes

The Configurable parameters dump 1 and 2 provide the dump of all the configurable parameters stored in MRAM at ASW start-up time [RD 4].

In order to restart the ASW the following telecommand is provided:

- Reboot (TC APID 1045).

The reboot (warm reset) procedure cannot be aborted. Once requested a reboot, the ASW writes the magic number 0xD501E7FC into defined area to notify the BOOT SW the nominal restart operation (see chapter 6). After CPU reset, the BOOT SW is executed.

It is also possible to perform the **Perform connection test** in order to check link between the ground segment and the IXPE DSU:

- Perform connection test (TC APID 1070)

The **Perform connection test** operation receives a **Connection test report** (TM APID 1270) reply.

5.3.1 DSU HK Report

After the boot the ASW starts to produce the **DSU Housekeeping Report** (TM APID 1200)
These telemetry packets provide general information regarding the status of the IXPE ASW status and DSU monitored hardware parameters.

The default sampling time at start-up is 1 second.
Anyway, it is possible to:

- Enable HK report generation (TC APID 1010)
- Disable HK report generation (TC APID 1011)
- Report active HK (TC APID 1012)
- Set HK report generation period (TC APID 1013)

The **Enable HK report generation** operation allows to enable the generation of specified housekeeping report telemetry packet.
The **Disable HK report generation** operation allows to disable the generation of specified housekeeping report telemetry packet.
The **Report active HK** reports operation allows to request an **Active HK reports report** (TM APID 1201) containing the generation report of the enabled housekeeping reports telemetry packets.
The generation period of disabled housekeeping reports telemetry packets is set to zero.
The **Set HK report generation period** operation allows to modify the generation period of specified housekeeping report telemetry packet. The generation period must be expressed in seconds.
The minimum sampling time for the DSU HK report is 1 second.

5.4 DSU MEMORY MANAGEMENT AND CONFIGURATION SETUP

All configuration activities involving memory access are performed in MAINTENANCE operative mode and include:

- Load DSU memory (TC APID 1020)
- Dump DSU memory (TC APID 1021)
- Check DSU memory (TC APID 1022)
- Set integer parameter (TC APID 1023)
- Set unsigned integer parameter (TC APID 1024)
- Get parameter (TC APID 1025)
- Configure memory EDAC (TC APID 1027)

The **Load DSU memory** operation allows to modify the content of any of the DSU memories. The length of the memory content is expressed in bytes and must be a multiple of the memory Smallest Addressable Unit (SAU, 4 bytes) as well the memory address.
The maximum length is fixed to 988 bytes.
The **Dump DSU memory** operation allows to dump the content of any of the DSU memories. The length of the memory content is expressed in bytes and must be a multiple of the memory SAU as well the memory address.
The successful completion of this operation produces a **DSU memory dump report** (TM APID 1260) telemetry containing the requested memory dump.

The **Check DSU memory** operation allows to compute the CRC-16-CCITT checksum of the content of any of the DSU memories. The length of the memory content is expressed in bytes and must be a multiple of the memory SAU as well the memory address. The successful completion of this operation produces a **DSU memory check report** (TM APID 1260) telemetry containing the requested CRC value. The SAU of all DSU memories is 4 bytes.
The **Set integer parameter** and **Set unsigned integer parameter** operations allow to modify the value of an onboard configurable parameter stored in MRAM.
The list of configurable parameters is reported in ANNEX B.1.
The successful completion of this operation produces a **Get integer parameter report** (TM APID 1262) or a **Get unsigned integer parameter report** (TM APID 1263) telemetry containing the requested configurable parameter value. On-board configurable parameters can be modified only in MAINTENANCE mode. Some of these are updated at RUNTIME, others require a REBOOT of the ASW to be effectively used.

The **Configure memory EDAC** operation allows to enable or disable the hardware EDAC protection of selected DSU memories.

The SW DSU Procedure is reported in annex C.2

5.4.1 Thermal Control MRAM Parameters

The thermal control parameters configurable on MRAM are:

TEC target
TEC threshold
HOP threshold
HOP target
TEC Kp
TEC Ki
HOP Kp
HOP Ki
TEC max current
HOP max current

The Thermal control parameters can be customized for each DUs.
In the Annex B.2 are reported the default values.

The thermal control algorithm is described in the par (5.5).

5.4.2 HV Calibration MRAM Parameters

All the HVB on board the DUs are characterized by different calibration curves for configuration and monitor values.
In order to indicate to the DSU which calibration curve has to be used for each DU is it possible to load in MRAM different parameters.

Values to be set during the SAA mode:

Vbottom engineering SAA
Vgem engineering SAA

These Values are the same for the three DUs (in Volt).

Calibration curves used by the on-board SW for the HV values into the Ramp Set TC are modelled using parameters:

ctrl Vdrift scaled multiplier
ctrl Vdrift scaled offset
ctrl Vbottom scaled multiplier
ctrl Vbottom scaled offset
ctrl Vgem scaled multiplier
ctrl Vgem scaled offset

We remark here that the Ramp Set TCs accept input in Volt. The parameters listed above are used by the on-board SW to command the DAC values in the HVBs.

Calibration curves used by the on-board SW for the HV monitor of the HVB:

mon Vdrift scaled multiplier
mon Vdrift scaled offset
mon Vbottom scaled multiplier
mon Vbottom scaled offset
mon Vtop scaled multiplier
mon Vtop scaled offset

Similarly, the parameters listed above are used by the on-board SW to convert the HV Monitor values into

Volts.

HV Operation range (in Volt):

Vdrift engineering min
Vdrift engineering max
Vbottom engineering min
Vbottom engineering max
Vgem engineering min
Vgem engineering max

HV delta tollerance (in Volt):

Vdrift engineering tolerance
Vbottom engineering tolerance
Vgem engineering tolerance

In the Annex B.3 are reported the default values.
The HVB nominal operations are described in the par 5.9.6.

5.4.3 DSU MRAM Parameters

Mission epoch in seconds
Scrub memory chunk size in bytes
SDI retry number
SDI buffer limit
DU1 CCI speed divider
DU2 CCI speed divider
DU3 CCI speed divider

In the Annex B.4 are reported the default values.

5.5 THERMAL CONTROL OPERATIONS

The Thermal control task is performed by the DSU in order to maintain the GPD temperature into the range defined and stored in MRAM.

The Thermal control is powered and operated directly by the DSU even if the DUs are switched OFF.

Thermal control operations allow to:

- Thermal controller enables (TC APID 1140)
- Thermal controller disables (TC APID 1141)

The **Thermal controller enable** operation allows to activate the thermal control of a Detector Unit using configured parameters.
The thermal loop implements a PI controller to maintain the GPD temperature within configured temperature range defined in MRAM by activating/deactivating Thermo Electric Cooler (TEC) or Heater Operative (HOP) devices.
The thermal control parameters configurable are reported in par 5.4.1 and they can be changed using TC MRAM telecommands in the Maintenance Operative Mode. The default configuration is reported in Annex B.2.
The main rule checked by the SW when these parameters are changed is:
TEC target > TEC Threshold > HOP threshold > HOP target

- HOP loop is activated if Tgpd ≤ HOP targe; deactivated if TGPD ≥ HOP threshold
- TEC loop activated if TGPD ≥ TEC target; deactivated if TGPD ≤ TEC Threshold
- Temperature acquisition accuracy is ±2°C
- IDLE loop frequency 1Hz
- HOP and TEC frequency 10Hz

Figure 5-2 shows parameters of the thermal controller.

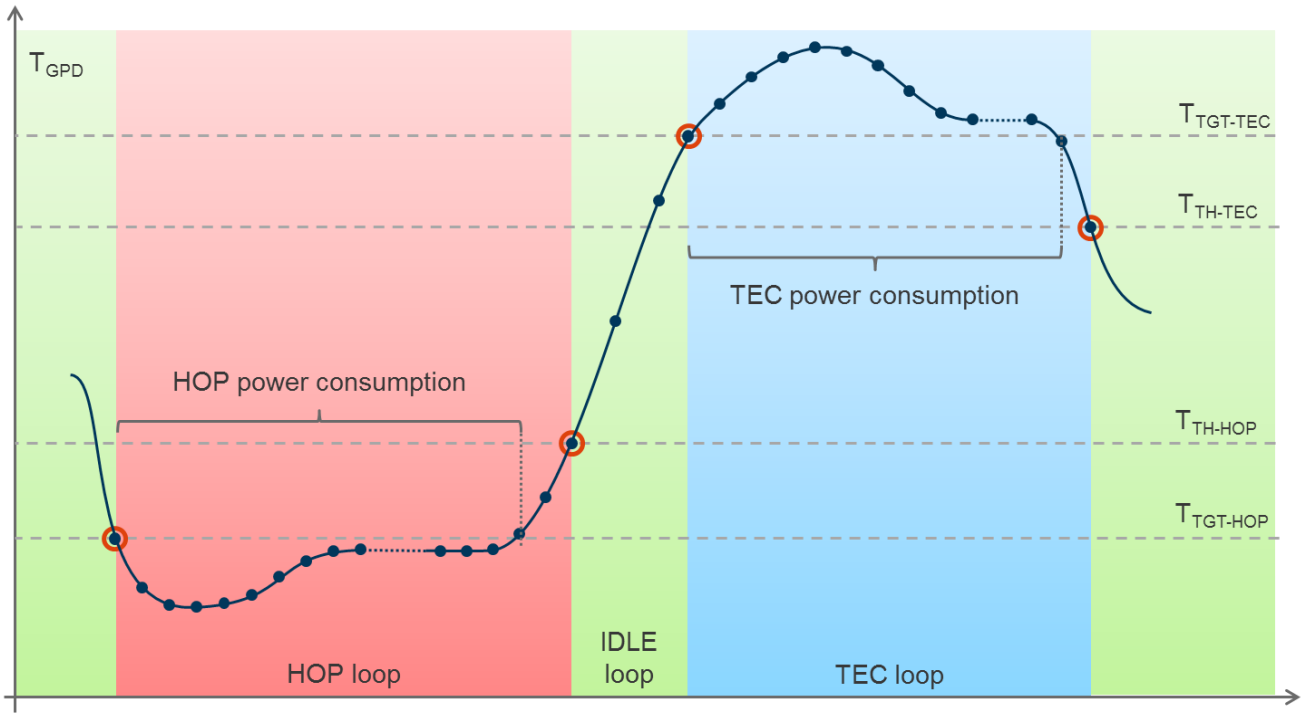


Figure 5-2: Thermal Control

The **Thermal controller disable** operation allows to deactivate the thermal control of a Detector Unit.

5.6 TIMING OPERATIONS

DSU timing operations allow to:

- Time of Day message processing enable (TC APID 1051)
- Time of Day message processing disable (TC APID 1052)
- DSU OBT time set (TC APID 1050)

The **Time of Day message processing enable** operation allows to enable the processing of the Time of Day message received from the spacecraft. In case of manual time set from ground the Time of Day message must be disabled.

The **Time of Day message processing disable** operation allows to disable the processing of the Time of Day message received from the spacecraft. This operation must be performed before setting the DSU OBT time.

The **DSU OBT time set** operation allows to set the DSU master on-board time seconds counter to a specific value. The counter of microseconds cannot be modified from ground, since it must be synchronized with

PPS signal. The OBT seconds counter will be actuated by DSU FPGA at the reception of next PPS signal. If a PPS signal is received during the execution of this operation, an unsuccessful telemetry report is sent to ground. Before performing this operation, it is required that the Time of Day message processing is disabled, otherwise the next received Time of Day message will overwrite the configuration set from ground.

The DSU Master OBT seconds counter is stored on the MRAM and It is maintained across DSU reboots. At the start-up the DSU is enabled to receive the TOD by default.

Refers to the Annex B.4 for the default values.

5.7 RUN ID SETUP

- Set run identifier (TC APID 1046)

The **Set run identifier** operation allows to force the run identifier to a specific value. The run identifier is a persistent counter incremented by the ASW at every operative mode successful transition. Its content is maintained between DSU reboots.

The main real time telemetries and the high rate telemetries report the run id [RD 04].

The default range during on ground testing has been 100000:299999 for the main section and 300000:499999 for the redundant.

5.8 DU POWER ON/OFF

Power operations allow to:

- DU power on 5V (TC APID 1193)
- DU power on 25V (TC APID 1194)
- DU power off (TC APID 1195)

WARNING: DU power on 5V and DU power on 25V must be executed in sequence. This is important in order to have a complete configuration of the lines related to the DAC HVBs.

The **DU power on 5V** operation allows to switch-on the +5V power line of the selected Detector Unit. This operation takes less than 1 second.

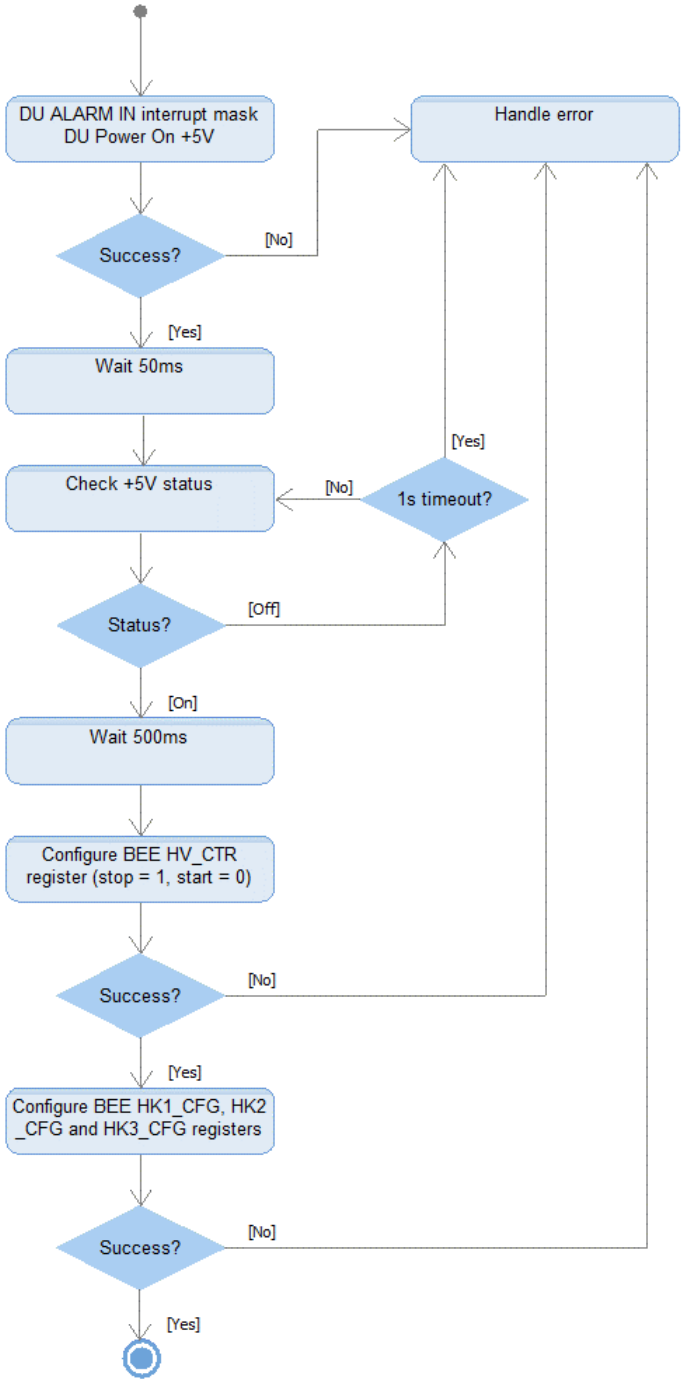


Figure 5-3: Detector Unit +5V power on sequence diagram

The **DU power on 25V** operation allows to switch-on the +25V power line of the selected Detector Unit. This operation is permitted only if the DU 5V are powered.

This operation is permitted only if the DU Power ON 5V has been successfully performed.

The operation takes less than 1 second.

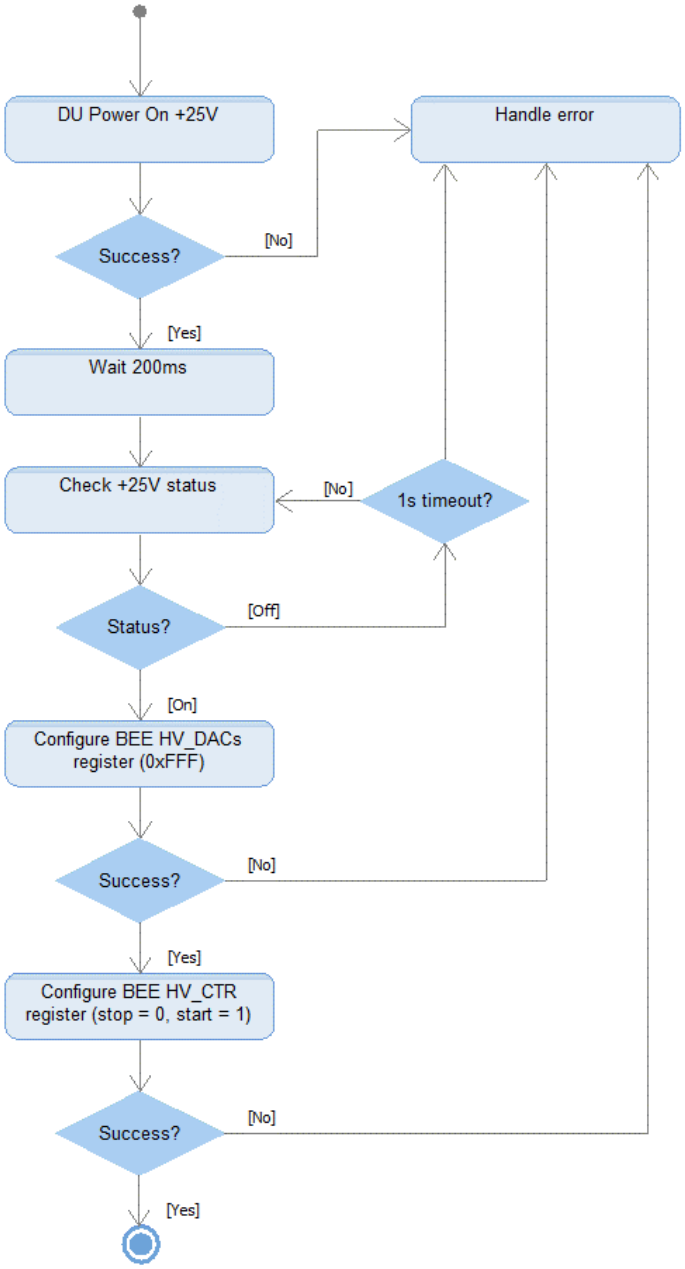


Figure 5-4: Detector Unit +25V power on sequence diagram

The **DU power off** operation allows to switch-of the +5V and +25V power lines of the selected Detector Unit. ***This operation is permitted only if the High Voltages are ramped down.***

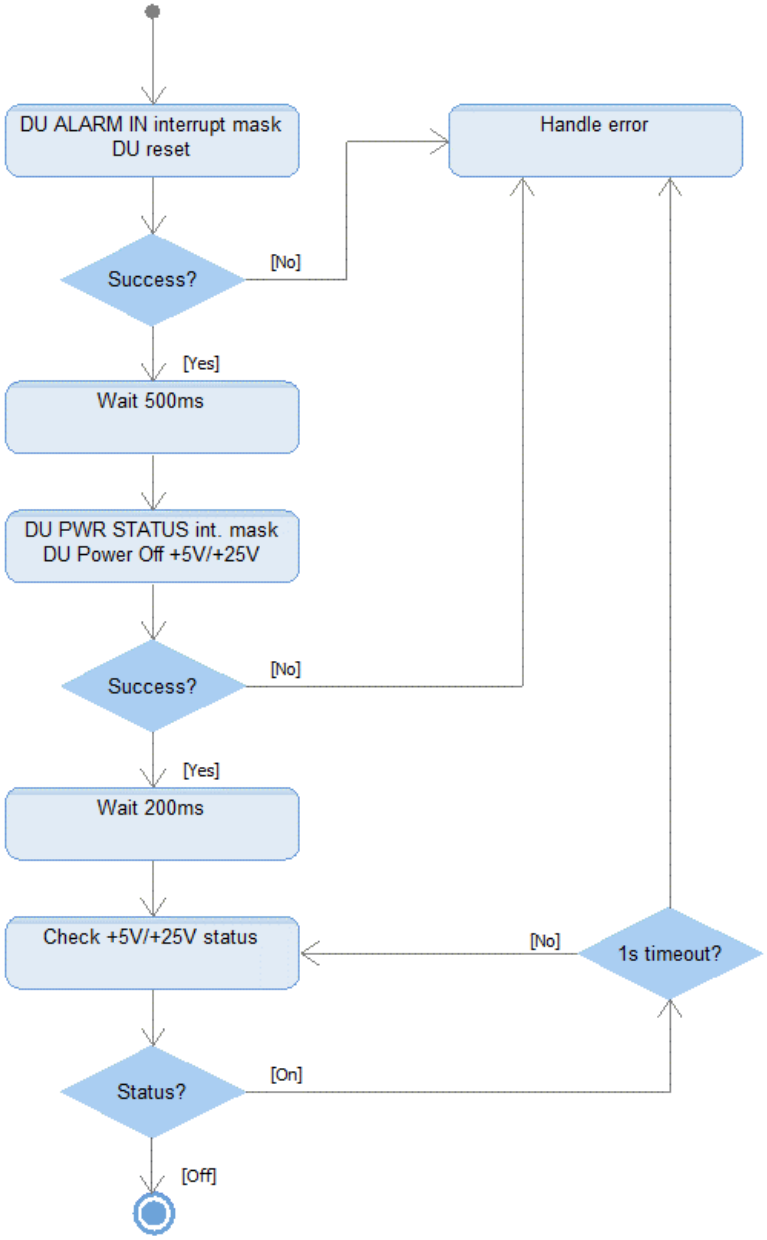


Figure 5-5: Detector Unit power off sequence diagram

5.8.1 DU Housekeeping Report

After +5V power-on sequence completes each Detector Unit starts to provide information about monitors and configuration into the BEE bank register.
The DSU SW collects this information and provide the following telemetries:

- Detector Unit 1 high rate housekeeping (TM APID 1321)
- Detector Unit 2 high rate housekeeping (TM APID 1322)
- Detector Unit 3 high rate housekeeping (TM APID 1323)
- Detector Unit 1 low rate housekeeping (TM APID 1324)
- Detector Unit 2 low rate housekeeping (TM APID 1325)
- Detector Unit 3 low rate housekeeping (TM APID 1326)

The **high rate reports** contain the main housekeeping monitors (Voltages, Currents, Temperatures).
The **Low rate report** contain mainly configuration information.

The default sampling time at start-up for the high rate housekeeping reports is 1 second.
The default sampling time at start-up for the low rate housekeeping reports is 30 seconds.

As already described for the DSU HK report (par 5.3.1) is always possible to:

- Enable HK report generation (TC APID 1010)
- Disable HK report generation (TC APID 1011)
- Report active HK (TC APID 1012)
- Set HK report generation period (TC APID 1013)

The minimum sampling time for the High and low rate reports are respectively 1 and 5 seconds.

5.9 DU CONFIGURATION

5.9.1 DU Low-Level Register Operations

The DSU can operate reading and writing the BEE Bank Registers located in the DUs.
Memory and registers operations allow to:

- BEE Load registers (TC APID 1100)
- BEE Dump registers (TC APID 1101)
- BEE Load critical registers (TC APID 1104)
- BEE Load SRAM (TC APID 1102)
- BEE Dump SRAM (TC APID 1103)
- BEE authorize (TC APID 1162)

The **BEE Load registers** operation allows to load up to 8 DU's registers at same time. In case of successful execution, **a BEE registers dump report** (TM APID 1450) telemetry is generated with the previous registers

content and sent to ground.
The **BEE Dump registers** operation allows to request the dump up to 8 DU's registers at same time. In case of successful execution, a **BEE registers dump report** (TM APID 1450) telemetry is generated with the registers content and sent to ground.
The **BEE Load critical registers** operation allows to load up to 8 DU's registers at same time (either critical on not critical). In case of successful execution, a BEE registers dump report (TM APID 1450) telemetry is generated with the previous registers content and sent to ground.
This BEE Load critical registers operation must be previously authorized by sending BEE Authorize telecommand (TC APID 1162).

The **BEE Load SRAM** operation allows to modify the content of the Detector Unit SRAM memory. The length of the memory content is expressed in bytes and must be a multiple of the memory Smallest Addressable Unit (SAU) as well the memory address.

The **BEE Dump SRAM** operation allows to dump the content of the Detector Unit SRAM memory. The length of the memory content is expressed in bytes and must be a multiple of the memory SAU as well the memory address. The successful completion of this operation produces a **BEE SRAM memory dump** (TM APID 1451) telemetry containing the requested memory dump.

The SAU of the Detector unit SRAM memory is 2 bytes.

5.9.2 DU BEE Setup

Configuration operations allow to:

- BEE configuration setup (TC APID 1156)
- BEE configuration setup load (TC APID 1157)
- BEE configuration setup store (TC APID 1158)

The BEE configuration setup operation allows to configure an acquisition setup on the Detector Unit.
The BEE configuration setup load and BEE configuration setup store operations allow to load/store from/to DSU MRAM a configuration setup. It is possible to store up to 32 setups. Setups are persistent between reboots.

With the BEE configuration Setup is it possible to configure the following parameters:

Mnemonic	Parameter Name	Default Value
UUU0256X	DAC V TH CTRL	-
UUU0257X	DAC V TEST CTRL	200
UUU0258X	SDI START ADDR	8192

UUU0259X	SDI CLK DIVIDER	4
UUU0260N	SDI RTX WAIT	250
UUU0261X	WIN D UPPER LIMIT	-
UUU0262X	WIN D LOW LIMIT	-
UUU0263X	ADC XPOL CLK DIV	8
UUU0264N	CLK PER CYCLES	8
UUU0265N	CLK SHIFT CYCLES	0
UUU0266S	ADC XPOL CLK DF CSN	ON
UUU0267S	ADC XPOL G0	OFF
UUU0268S	ADC XPOL G1	OFF
UUU0269S	ADC TYPE	ST
UUU0270X	PHA ULIM THR	-
UUU0271X	PHA LLIM THR	-
UUU0272N	DIAG EVENTS PERIOD	-
UUU0273X	XPOL DISCH WIDTH	25000
UUU0274X	XPOL MH CYCLES	320
UUU0275X	XPOL ZS THR	-
UUU0276N	XPOL PED NUMBER	-
UUU0277X	XPOL INJ WIDTH	-
UUU0278X	XPOL INJ PERIOD	-
UUU0279N	SCAN STEPS X	-
UUU0280N	SCAN STEPS Y	-
UUU0281N	SCAN DELTA X	-
UUU0282N	SCAN DELTA Y	-
UUU0283N	PULSES PER PIXEL	-
UUU0284X	XPOL X ADDR	-
UUU0285X	XPOL Y ADDR	-
UUU0286S	PIXEL SCAN ENABLE	-
UUU0287X	XPOL CONFIG REG	0x0E
UUU0288S	XPOL SI MODE	CORE_LOGIC
UUU0289S	MUX SELECT	-

UUU0290S	HK1 ENABLE	ENABLE
UUU0291S	HK2 ENABLE	ENABLE
UUU0292S	HK3 ENABLE	ENABLE
UUU0293X	HK1 CHANNEL MASK	0xff
UUU0294X	HK2 CHANNEL MASK	0xff
UUU0295X	HK3 CHANNEL MASK	0xff

DAC V TEST CTRL, SDI START ADDR, SDI CLK DIVIDER, SDI RTX WAIT, ADC XPOL CLK DIV, CLK PER CYCLES, CLK SHIFT CYCLES, ADC XPOL CLK DF CSN, ADC XPOL G0, ADC XPOL G1, ADC TYPE, XPOL DISCH WIDTH, XPOL MH CYCLES, XPOL CONFIG REG, XPOL SI MODE, MUX SELECT parameters are related to the electronics and logic of read out [AD 6].
The default values reported can be changed only after discussions with I2T.

HK1 ENABLE, HK2 ENABLE, HK3 ENABLE, HK1 CHANNEL MASK, HK2 CHANNEL MASK, HK3 CHANNEL MASK parameters are related to the monitoring and HK collection made by the DU FPGA.
The default configuration is all ENABLE.
The other parameters can be changed, and they are related to the Nominal Operations explained in chapter 6.

5.9.2.1 DU BEE Setup preset retrieving

There is not a specific TC to get the BEE Setup presets stored on board.

The presets stored con the MRAM can be dumped from the Operational Mode Maintenance using the following addresses and dump length.

Memory ID:
UT699FT_MRAM

Length:
BEE_SETUP_TC_SLOT_SIZE = 80

Addresses of the 32 slots:
DU1_STORED_PRESETS_BEE_SETUP[0] = 0x10305180
DU1_STORED_PRESETS_BEE_SETUP[1] = 0x103051D0
DU1_STORED_PRESETS_BEE_SETUP[2] = 0x10305220
DU1_STORED_PRESETS_BEE_SETUP[3] = 0x10305270
DU1_STORED_PRESETS_BEE_SETUP[4] = 0x103052C0
DU1_STORED_PRESETS_BEE_SETUP[5] = 0x10305310

DU1_STORED_PRESETS_BEE_SETUP[6] = 0x10305360
DU1_STORED_PRESETS_BEE_SETUP[7] = 0x103053B0
DU1_STORED_PRESETS_BEE_SETUP[8] = 0x10305400
DU1_STORED_PRESETS_BEE_SETUP[9] = 0x10305450
DU1_STORED_PRESETS_BEE_SETUP[10] = 0x103054A0
DU1_STORED_PRESETS_BEE_SETUP[11] = 0x103054F0
DU1_STORED_PRESETS_BEE_SETUP[12] = 0x10305540
DU1_STORED_PRESETS_BEE_SETUP[13] = 0x10305590
DU1_STORED_PRESETS_BEE_SETUP[14] = 0x103055E0
DU1_STORED_PRESETS_BEE_SETUP[15] = 0x10305630
DU1_STORED_PRESETS_BEE_SETUP[16] = 0x10305680
DU1_STORED_PRESETS_BEE_SETUP[17] = 0x103056D0
DU1_STORED_PRESETS_BEE_SETUP[18] = 0x10305720
DU1_STORED_PRESETS_BEE_SETUP[19] = 0x10305770
DU1_STORED_PRESETS_BEE_SETUP[20] = 0x103057C0
DU1_STORED_PRESETS_BEE_SETUP[21] = 0x10305810
DU1_STORED_PRESETS_BEE_SETUP[22] = 0x10305860
DU1_STORED_PRESETS_BEE_SETUP[23] = 0x103058B0
DU1_STORED_PRESETS_BEE_SETUP[24] = 0x10305900
DU1_STORED_PRESETS_BEE_SETUP[25] = 0x10305950
DU1_STORED_PRESETS_BEE_SETUP[26] = 0x103059A0
DU1_STORED_PRESETS_BEE_SETUP[27] = 0x103059F0
DU1_STORED_PRESETS_BEE_SETUP[28] = 0x10305A40
DU1_STORED_PRESETS_BEE_SETUP[29] = 0x10305A90
DU1_STORED_PRESETS_BEE_SETUP[30] = 0x10305AE0
DU1_STORED_PRESETS_BEE_SETUP[32] = 0x10305B30

DU2_STORED_PRESETS_BEE_SETUP[0] = 0x10307300
DU2_STORED_PRESETS_BEE_SETUP[1] = 0x10307350
DU2_STORED_PRESETS_BEE_SETUP[2] = 0x103073A0
DU2_STORED_PRESETS_BEE_SETUP[3] = 0x103073F0
DU2_STORED_PRESETS_BEE_SETUP[4] = 0x10307440
DU2_STORED_PRESETS_BEE_SETUP[5] = 0x10307490
DU2_STORED_PRESETS_BEE_SETUP[6] = 0x103074E0
DU2_STORED_PRESETS_BEE_SETUP[7] = 0x10307530
DU2_STORED_PRESETS_BEE_SETUP[8] = 0x10307580
DU2_STORED_PRESETS_BEE_SETUP[9] = 0x103075D0
DU2_STORED_PRESETS_BEE_SETUP[10] = 0x10307620
DU2_STORED_PRESETS_BEE_SETUP[11] = 0x10307670
DU2_STORED_PRESETS_BEE_SETUP[12] = 0x103076C0
DU2_STORED_PRESETS_BEE_SETUP[13] = 0x10307710
DU2_STORED_PRESETS_BEE_SETUP[14] = 0x10307760
DU2_STORED_PRESETS_BEE_SETUP[15] = 0x103077B0
DU2_STORED_PRESETS_BEE_SETUP[16] = 0x10307800
DU2_STORED_PRESETS_BEE_SETUP[17] = 0x10307850
DU2_STORED_PRESETS_BEE_SETUP[18] = 0x103078A0
DU2_STORED_PRESETS_BEE_SETUP[19] = 0x103078F0

DU2_STORED_PRESETS_BEE_SETUP[20] = 0x10307940
DU2_STORED_PRESETS_BEE_SETUP[21] = 0x10307990
DU2_STORED_PRESETS_BEE_SETUP[22] = 0x103079E0
DU2_STORED_PRESETS_BEE_SETUP[23] = 0x10307A30
DU2_STORED_PRESETS_BEE_SETUP[24] = 0x10307A80
DU2_STORED_PRESETS_BEE_SETUP[25] = 0x10307AD0
DU2_STORED_PRESETS_BEE_SETUP[26] = 0x10307B20
DU2_STORED_PRESETS_BEE_SETUP[27] = 0x10307B70
DU2_STORED_PRESETS_BEE_SETUP[28] = 0x10307BC0
DU2_STORED_PRESETS_BEE_SETUP[29] = 0x10307C10
DU2_STORED_PRESETS_BEE_SETUP[30] = 0x10307C60
DU2_STORED_PRESETS_BEE_SETUP[31] = 0x10307CB0

DU3_STORED_PRESETS_BEE_SETUP[0] = 0x10309480
DU3_STORED_PRESETS_BEE_SETUP[1] = 0x103094D0
DU3_STORED_PRESETS_BEE_SETUP[2] = 0x10309520
DU3_STORED_PRESETS_BEE_SETUP[3] = 0x10309570
DU3_STORED_PRESETS_BEE_SETUP[4] = 0x103095C0
DU3_STORED_PRESETS_BEE_SETUP[5] = 0x10309610
DU3_STORED_PRESETS_BEE_SETUP[6] = 0x10309660
DU3_STORED_PRESETS_BEE_SETUP[7] = 0x103096B0
DU3_STORED_PRESETS_BEE_SETUP[8] = 0x10309700
DU3_STORED_PRESETS_BEE_SETUP[9] = 0x10309750
DU3_STORED_PRESETS_BEE_SETUP[10] = 0x103097A0
DU3_STORED_PRESETS_BEE_SETUP[11] = 0x103097F0
DU3_STORED_PRESETS_BEE_SETUP[12] = 0x10309840
DU3_STORED_PRESETS_BEE_SETUP[13] = 0x10309890
DU3_STORED_PRESETS_BEE_SETUP[14] = 0x103098E0
DU3_STORED_PRESETS_BEE_SETUP[15] = 0x10309930
DU3_STORED_PRESETS_BEE_SETUP[16] = 0x10309980
DU3_STORED_PRESETS_BEE_SETUP[17] = 0x103099D0
DU3_STORED_PRESETS_BEE_SETUP[18] = 0x10309A20
DU3_STORED_PRESETS_BEE_SETUP[19] = 0x10309A70
DU3_STORED_PRESETS_BEE_SETUP[20] = 0x10309AC0
DU3_STORED_PRESETS_BEE_SETUP[21] = 0x10309B10
DU3_STORED_PRESETS_BEE_SETUP[22] = 0x10309B60
DU3_STORED_PRESETS_BEE_SETUP[23] = 0x10309BB0
DU3_STORED_PRESETS_BEE_SETUP[24] = 0x10309C00
DU3_STORED_PRESETS_BEE_SETUP[25] = 0x10309C50
DU3_STORED_PRESETS_BEE_SETUP[26] = 0x10309CA0
DU3_STORED_PRESETS_BEE_SETUP[27] = 0x10309CF0
DU3_STORED_PRESETS_BEE_SETUP[28] = 0x10309D40
DU3_STORED_PRESETS_BEE_SETUP[29] = 0x10309D90
DU3_STORED_PRESETS_BEE_SETUP[30] = 0x10309DE0
DU3_STORED_PRESETS_BEE_SETUP[31] = 0x10309E30

5.9.3 DU Pixel Mask

Individual pixels can be masked using the following configuration operations:

- BEE mask pixels (TC APID 1153)
- BEE mask pixels preset load (TC APID 1154)
- BEE mask pixels preset store (TC APID 1155)

The **BEE mask pixels** operation allows to load onto the Detector Unit a map of pixels to be masked during science data acquisition.
It is possible to mask 32 pixels at same time.
The structure of the TC is the follow:

UUU0170S	ENABLE ALL
UUU0171N	PIXELS NUMBER
UUU0172X	PIXEL1 X POS
UUU0173X	PIXEL1 Y POS
UUU0174X	PIXEL2 X POS
UUU0175X	PIXEL2 Y POS
…..	….

The TC acts directly on indicated DU loading in corresponding ASIC the pixels that must be masked.
The parameter "ENABLE ALL" at the beginning of the TC indicates if the pixel mask configuration already loaded has to be reset before to mask the pixels indicated.
In case of more than 32 pixels to mask, it needs to send more than one TC. Please note that the successive TCs to the first one must have the parameter "ENABLE ALL" disabled in order to not reset the previous pixels masked.

The **BEE mask pixels preset load** and **BEE mask pixels preset store** operations allow to load/store from/to DSU MRAM a mask pixels preset. It is possible to store up to 32 presets. Presets are persistent between reboots.

Each DU has a specific list of noisy pixels evaluated during GPD acceptance test, DU AIV/T, DU Calibration and Instrument E2E Test.
The main aim of pixel masking is to avoid to report fake triggers on telemetry and so to impact the High Rate data rate. This list can be evaluated and updated on board at any time if new noisy pixels appear.

New pixels noisy can be detected on the ground SW pipeline with specific algorithm analysing nominal acquisitions, both from celestial sources or calibration sources. If a pixel is masked its signal does not contribute to the trigger within its mini-cluster. It is worth noticing that since the trigger is formed by groups of 4 pixels, masking only one or two of the same mini-cluster has a small effect on the trigger efficiency if the threshold is reasonably low.

During nominal operation, the status of pixel noisy will be monitored and, if necessary, update by I2T.

The DUs pixel masks stored on board (see annex B.7) are valid at the time of the Instrument E2E test.

5.9.3.1 DU Pixel Mask preset retrieving

There is not a specific TC to get the BEE mask pixels presets stored on board.

These presets stored can be dumped from the Operational Mode Maintenance using the following addresses and dump length.

Memory ID:
UT699FT_MRAM

Length:
BEE_SETUP_TC_SLOT_SIZE = 148

Addresses of the 32 slots:

DU1_STORED_PRESETS_BEE_PIXELS_MASK[0] = 0x10303F00
DU1_STORED_PRESETS_BEE_PIXELS_MASK[1] = 0x10303F94
DU1_STORED_PRESETS_BEE_PIXELS_MASK[2] = 0x10304028
DU1_STORED_PRESETS_BEE_PIXELS_MASK[3] = 0x103040BC
DU1_STORED_PRESETS_BEE_PIXELS_MASK[4] = 0x10304150
DU1_STORED_PRESETS_BEE_PIXELS_MASK[5] = 0x103041E4
DU1_STORED_PRESETS_BEE_PIXELS_MASK[6] = 0x10304278
DU1_STORED_PRESETS_BEE_PIXELS_MASK[7] = 0x1030430C
DU1_STORED_PRESETS_BEE_PIXELS_MASK[8] = 0x103043A0
DU1_STORED_PRESETS_BEE_PIXELS_MASK[9] = 0x10304434
DU1_STORED_PRESETS_BEE_PIXELS_MASK[10] = 0x103044C8
DU1_STORED_PRESETS_BEE_PIXELS_MASK[11] = 0x1030455C
DU1_STORED_PRESETS_BEE_PIXELS_MASK[12] = 0x103045F0
DU1_STORED_PRESETS_BEE_PIXELS_MASK[13] = 0x10304684
DU1_STORED_PRESETS_BEE_PIXELS_MASK[14] = 0x10304718
DU1_STORED_PRESETS_BEE_PIXELS_MASK[15] = 0x103047AC
DU1_STORED_PRESETS_BEE_PIXELS_MASK[16] = 0x10304840

DU1_STORED_PRESETS_BEE_PIXELS_MASK[17] = 0x103048D4
DU1_STORED_PRESETS_BEE_PIXELS_MASK[18] = 0x10304968
DU1_STORED_PRESETS_BEE_PIXELS_MASK[19] = 0x103049FC
DU1_STORED_PRESETS_BEE_PIXELS_MASK[20] = 0x10304A90
DU1_STORED_PRESETS_BEE_PIXELS_MASK[21] = 0x10304B24
DU1_STORED_PRESETS_BEE_PIXELS_MASK[22] = 0x10304BB8
DU1_STORED_PRESETS_BEE_PIXELS_MASK[23] = 0x10304C4C
DU1_STORED_PRESETS_BEE_PIXELS_MASK[24] = 0x10304CE0
DU1_STORED_PRESETS_BEE_PIXELS_MASK[25] = 0x10304D74
DU1_STORED_PRESETS_BEE_PIXELS_MASK[26] = 0x10304E08
DU1_STORED_PRESETS_BEE_PIXELS_MASK[27] = 0x10304E9C
DU1_STORED_PRESETS_BEE_PIXELS_MASK[28] = 0x10304F30
DU1_STORED_PRESETS_BEE_PIXELS_MASK[99] = 0x10304FC4
DU1_STORED_PRESETS_BEE_PIXELS_MASK[30] = 0x10305058
DU1_STORED_PRESETS_BEE_PIXELS_MASK[31] = 0x103050EC

DU2_STORED_PRESETS_BEE_PIXELS_MASK[0] = 0x10306080
DU2_STORED_PRESETS_BEE_PIXELS_MASK[1] = 0x10306114
DU2_STORED_PRESETS_BEE_PIXELS_MASK[2] = 0x103061A8
DU2_STORED_PRESETS_BEE_PIXELS_MASK[3] = 0x1030623C
DU2_STORED_PRESETS_BEE_PIXELS_MASK[4] = 0x103062D0
DU2_STORED_PRESETS_BEE_PIXELS_MASK[5] = 0x10306364
DU2_STORED_PRESETS_BEE_PIXELS_MASK[6] = 0x103063F8
DU2_STORED_PRESETS_BEE_PIXELS_MASK[7] = 0x1030648C
DU2_STORED_PRESETS_BEE_PIXELS_MASK[8] = 0x10306520
DU2_STORED_PRESETS_BEE_PIXELS_MASK[9] = 0x103065B4
DU2_STORED_PRESETS_BEE_PIXELS_MASK[10] = 0x10306648
DU2_STORED_PRESETS_BEE_PIXELS_MASK[11] = 0x103066DC
DU2_STORED_PRESETS_BEE_PIXELS_MASK[12] = 0x10306770
DU2_STORED_PRESETS_BEE_PIXELS_MASK[13] = 0x10306804
DU2_STORED_PRESETS_BEE_PIXELS_MASK[14] = 0x10306898
DU2_STORED_PRESETS_BEE_PIXELS_MASK[15] = 0x1030692C
DU2_STORED_PRESETS_BEE_PIXELS_MASK[16] = 0x103069C0
DU2_STORED_PRESETS_BEE_PIXELS_MASK[17] = 0x10306A54
DU2_STORED_PRESETS_BEE_PIXELS_MASK[18] = 0x10306AE8
DU2_STORED_PRESETS_BEE_PIXELS_MASK[19] = 0x10306B7C
DU2_STORED_PRESETS_BEE_PIXELS_MASK[20] = 0x10306C10
DU2_STORED_PRESETS_BEE_PIXELS_MASK[21] = 0x10306CA4
DU2_STORED_PRESETS_BEE_PIXELS_MASK[22] = 0x10306D38
DU2_STORED_PRESETS_BEE_PIXELS_MASK[23] = 0x10306DCC
DU2_STORED_PRESETS_BEE_PIXELS_MASK[24] = 0x10306E60
DU2_STORED_PRESETS_BEE_PIXELS_MASK[25] = 0x10306EF4
DU2_STORED_PRESETS_BEE_PIXELS_MASK[26] = 0x10306F88
DU2_STORED_PRESETS_BEE_PIXELS_MASK[27] = 0x1030701C
DU2_STORED_PRESETS_BEE_PIXELS_MASK[28] = 0x103070B0
DU2_STORED_PRESETS_BEE_PIXELS_MASK[29] = 0x10307144
DU2_STORED_PRESETS_BEE_PIXELS_MASK[30] = 0x103071D8

DU2_STORED_PRESETS_BEE_PIXELS_MASK[31] = 0x1030726C

DU3_STORED_PRESETS_BEE_PIXELS_MASK[0] = 0x10308200
DU3_STORED_PRESETS_BEE_PIXELS_MASK[1] = 0x10308294
DU3_STORED_PRESETS_BEE_PIXELS_MASK[2] = 0x10308328
DU3_STORED_PRESETS_BEE_PIXELS_MASK[3] = 0x103083BC
DU3_STORED_PRESETS_BEE_PIXELS_MASK[4] = 0x10308450
DU3_STORED_PRESETS_BEE_PIXELS_MASK[5] = 0x103084E4
DU3_STORED_PRESETS_BEE_PIXELS_MASK[6] = 0x10308578
DU3_STORED_PRESETS_BEE_PIXELS_MASK[7] = 0x1030860C
DU3_STORED_PRESETS_BEE_PIXELS_MASK[8] = 0x103086A0
DU3_STORED_PRESETS_BEE_PIXELS_MASK[9] = 0x10308734
DU3_STORED_PRESETS_BEE_PIXELS_MASK[10] = 0x103087C8
DU3_STORED_PRESETS_BEE_PIXELS_MASK[11] = 0x1030885C
DU3_STORED_PRESETS_BEE_PIXELS_MASK[12] = 0x103088F0
DU3_STORED_PRESETS_BEE_PIXELS_MASK[13] = 0x10308984
DU3_STORED_PRESETS_BEE_PIXELS_MASK[14] = 0x10308A18
DU3_STORED_PRESETS_BEE_PIXELS_MASK[15] = 0x10308AAC
DU3_STORED_PRESETS_BEE_PIXELS_MASK[16] = 0x10308B40
DU3_STORED_PRESETS_BEE_PIXELS_MASK[17] = 0x10308BD4
DU3_STORED_PRESETS_BEE_PIXELS_MASK[18] = 0x10308C68
DU3_STORED_PRESETS_BEE_PIXELS_MASK[19] = 0x10308CFC
DU3_STORED_PRESETS_BEE_PIXELS_MASK[20] = 0x10308D90
DU3_STORED_PRESETS_BEE_PIXELS_MASK[21] = 0x10308E24
DU3_STORED_PRESETS_BEE_PIXELS_MASK[22] = 0x10308EB8
DU3_STORED_PRESETS_BEE_PIXELS_MASK[23] = 0x10308F4C
DU3_STORED_PRESETS_BEE_PIXELS_MASK[24] = 0x10308FE0
DU3_STORED_PRESETS_BEE_PIXELS_MASK[25] = 0x10309074
DU3_STORED_PRESETS_BEE_PIXELS_MASK[26] = 0x10309108
DU3_STORED_PRESETS_BEE_PIXELS_MASK[27] = 0x1030919C
DU3_STORED_PRESETS_BEE_PIXELS_MASK[28] = 0x10309230
DU3_STORED_PRESETS_BEE_PIXELS_MASK[29] = 0x103092C4
DU3_STORED_PRESETS_BEE_PIXELS_MASK[30] = 0x10309358
DU3_STORED_PRESETS_BEE_PIXELS_MASK[31] = 0x103093EC

5.9.4 DU BEE Alarm

Configuration operations allow to:
BEE alarm configuration (TC APID 1159)
BEE alarm configuration load (TC APID 1160)
BEE alarm configuration store (TC APID 1161)

The **BEE alarm configuration** operation allows to enable and set the thresholds to detect an alarm and rise the ALARM OUT signal from the Detector Unit.

The **BEE alarm configuration load** and **BEE alarm configuration store** operations allow to load/store from/to DSU MRAM an alarm configuration. It is possible to store up to 32 alarm configurations. Configurations stored are persistent between reboots.

The HK that can be monitored are:

UUU0310S	ALARM RESET
UUU0311S	ALARM MASK
UUU0312U	VOLT DRIFT THR
UUU0313I	CURR DRIFT THR
UUU0314U	VOLT BOTTOM THR
UUU0315I	CURR BOTTOM THR
UUU0316U	VOLT TOP THR
UUU0317I	CURR GEM THR
UUU0318I	CURR 5V THR
UUU0319I	CURR 3V3 THR
UUU0320I	CURR 1V8 THR
UUU0321I	CURR 1V5 THR

The alarm presets stored on board (see Annex B.6) have been validate during the Instrument E2E test.

5.9.4.1 DU BEE alarm preset retrieving

There is not a specific TC to get the BEE mask pixels presets stored on board.

These presets stored can be dumped from the Operational Mode Maintenance using the following addresses and dump length.

Memory ID:
UT699FT_MRAM

Length:
BEE_SETUP_TC_SLOT_SIZE = 40

Addresses of the 32 slots:

DU1_STORED_PRESETS_ALARM_CFG[0] = 0x10305B80

DU1_STORED_PRESETS_ALARM_CFG[1] = 0x10305BA8
DU1_STORED_PRESETS_ALARM_CFG[2] = 0x10305BD0
DU1_STORED_PRESETS_ALARM_CFG[3] = 0x10305BF8
DU1_STORED_PRESETS_ALARM_CFG[4] = 0x10305C20
DU1_STORED_PRESETS_ALARM_CFG[5] = 0x10305C48
DU1_STORED_PRESETS_ALARM_CFG[6] = 0x10305C70
DU1_STORED_PRESETS_ALARM_CFG[7] = 0x10305C98
DU1_STORED_PRESETS_ALARM_CFG[8] = 0x10305CC0
DU1_STORED_PRESETS_ALARM_CFG[9] = 0x10305CE8
DU1_STORED_PRESETS_ALARM_CFG[10] = 0x10305D10
DU1_STORED_PRESETS_ALARM_CFG[11] = 0x10305D38
DU1_STORED_PRESETS_ALARM_CFG[12] = 0x10305D60
DU1_STORED_PRESETS_ALARM_CFG[13] = 0x10305D88
DU1_STORED_PRESETS_ALARM_CFG[14] = 0x10305DB0
DU1_STORED_PRESETS_ALARM_CFG[15] = 0x10305DD8
DU1_STORED_PRESETS_ALARM_CFG[16] = 0x10305E00
DU1_STORED_PRESETS_ALARM_CFG[17] = 0x10305E28
DU1_STORED_PRESETS_ALARM_CFG[18] = 0x10305E50
DU1_STORED_PRESETS_ALARM_CFG[19] = 0x10305E78
DU1_STORED_PRESETS_ALARM_CFG[20] = 0x10305EA0
DU1_STORED_PRESETS_ALARM_CFG[21] = 0x10305EC8
DU1_STORED_PRESETS_ALARM_CFG[22] = 0x10305EF0
DU1_STORED_PRESETS_ALARM_CFG[23] = 0x10305F18
DU1_STORED_PRESETS_ALARM_CFG[24] = 0x10305F40
DU1_STORED_PRESETS_ALARM_CFG[25] = 0x10305F68
DU1_STORED_PRESETS_ALARM_CFG[26] = 0x10305F90
DU1_STORED_PRESETS_ALARM_CFG[27] = 0x10305FB8
DU1_STORED_PRESETS_ALARM_CFG[28] = 0x10305FE0
DU1_STORED_PRESETS_ALARM_CFG[29] = 0x10306008
DU1_STORED_PRESETS_ALARM_CFG[30] = 0x10306030
DU1_STORED_PRESETS_ALARM_CFG[31] = 0x10306058

DU2_STORED_PRESETS_ALARM_CFG[0] = 0x10307D00
DU2_STORED_PRESETS_ALARM_CFG[1] = 0x10307D28
DU2_STORED_PRESETS_ALARM_CFG[2] = 0x10307D50
DU2_STORED_PRESETS_ALARM_CFG[3] = 0x10307D78
DU2_STORED_PRESETS_ALARM_CFG[4] = 0x10307DA0
DU2_STORED_PRESETS_ALARM_CFG[5] = 0x10307DC8
DU2_STORED_PRESETS_ALARM_CFG[6] = 0x10307DF0
DU2_STORED_PRESETS_ALARM_CFG[7] = 0x10307E18
DU2_STORED_PRESETS_ALARM_CFG[8] = 0x10307E40
DU2_STORED_PRESETS_ALARM_CFG[9] = 0x10307E68
DU2_STORED_PRESETS_ALARM_CFG[10] = 0x10307E90
DU2_STORED_PRESETS_ALARM_CFG[11] = 0x10307EB8
DU2_STORED_PRESETS_ALARM_CFG[12] = 0x10307EE0
DU2_STORED_PRESETS_ALARM_CFG[13] = 0x10307F08

DU2_STORED_PRESETS_ALARM_CFG[14] = 0x10307F30
DU2_STORED_PRESETS_ALARM_CFG[15] = 0x10307F58
DU2_STORED_PRESETS_ALARM_CFG[16] = 0x10307F80
DU2_STORED_PRESETS_ALARM_CFG[17] = 0x10307FA8
DU2_STORED_PRESETS_ALARM_CFG[18] = 0x10307FD0
DU2_STORED_PRESETS_ALARM_CFG[19] = 0x10307FF8
DU2_STORED_PRESETS_ALARM_CFG[20] = 0x10308020
DU2_STORED_PRESETS_ALARM_CFG[21] = 0x10308048
DU2_STORED_PRESETS_ALARM_CFG[22] = 0x10308070
DU2_STORED_PRESETS_ALARM_CFG[23] = 0x10308098
DU2_STORED_PRESETS_ALARM_CFG[24] = 0x103080C0
DU2_STORED_PRESETS_ALARM_CFG[25] = 0x103080E8
DU2_STORED_PRESETS_ALARM_CFG[26] = 0x10308110
DU2_STORED_PRESETS_ALARM_CFG[27] = 0x10308138
DU2_STORED_PRESETS_ALARM_CFG[28] = 0x10308160
DU2_STORED_PRESETS_ALARM_CFG[29] = 0x10308188
DU2_STORED_PRESETS_ALARM_CFG[30] = 0x103081B0
DU2_STORED_PRESETS_ALARM_CFG[31] = 0x103081D8

DU3_STORED_PRESETS_ALARM_CFG[0] = 0x10309E80
DU3_STORED_PRESETS_ALARM_CFG[1] = 0x10309EA8
DU3_STORED_PRESETS_ALARM_CFG[2] = 0x10309ED0
DU3_STORED_PRESETS_ALARM_CFG[3] = 0x10309EF8
DU3_STORED_PRESETS_ALARM_CFG[4] = 0x10309F20
DU3_STORED_PRESETS_ALARM_CFG[5] = 0x10309F48
DU3_STORED_PRESETS_ALARM_CFG[6] = 0x10309F70
DU3_STORED_PRESETS_ALARM_CFG[7] = 0x10309F98
DU3_STORED_PRESETS_ALARM_CFG[8] = 0x10309FC0
DU3_STORED_PRESETS_ALARM_CFG[9] = 0x10309FE8
DU3_STORED_PRESETS_ALARM_CFG[10] = 0x1030A010
DU3_STORED_PRESETS_ALARM_CFG[11] = 0x1030A038
DU3_STORED_PRESETS_ALARM_CFG[12] = 0x1030A060
DU3_STORED_PRESETS_ALARM_CFG[13] = 0x1030A088
DU3_STORED_PRESETS_ALARM_CFG[14] = 0x1030A0B0
DU3_STORED_PRESETS_ALARM_CFG[15] = 0x1030A0D8
DU3_STORED_PRESETS_ALARM_CFG[16] = 0x1030A100
DU3_STORED_PRESETS_ALARM_CFG[17] = 0x1030A128
DU3_STORED_PRESETS_ALARM_CFG[18] = 0x1030A150
DU3_STORED_PRESETS_ALARM_CFG[19] = 0x1030A178
DU3_STORED_PRESETS_ALARM_CFG[20] = 0x1030A1A0
DU3_STORED_PRESETS_ALARM_CFG[21] = 0x1030A1C8
DU3_STORED_PRESETS_ALARM_CFG[22] = 0x1030A1F0
DU3_STORED_PRESETS_ALARM_CFG[23] = 0x1030A218
DU3_STORED_PRESETS_ALARM_CFG[24] = 0x1030A240
DU3_STORED_PRESETS_ALARM_CFG[25] = 0x1030A268
DU3_STORED_PRESETS_ALARM_CFG[26] = 0x1030A290
DU3_STORED_PRESETS_ALARM_CFG[27] = 0x1030A2B8

DU3_STORED_PRESETS_ALARM_CFG[28] = 0x1030A2E0
DU3_STORED_PRESETS_ALARM_CFG[29] = 0x1030A308
DU3_STORED_PRESETS_ALARM_CFG[30] = 0x1030A330
DU3_STORED_PRESETS_ALARM_CFG[31] = 0x1030A358

5.9.5 DU Observation Setup

Configuration operations allow to:

- BEE observation setup (TC APID 1163)

The **BEE observation setup** operation allows to select the event type generated by the Detector Unit and enable/disable the orphan pixels removal. Allowed configurations are:

- Nominal acquisition
- Pixels scan
- Pedestal calibration
- Stand-by

The BEE observation mode selected is activated when the SW Operation Mode change to Observation from Stand-By.

5.9.6 HVB Configurations

High Voltages Boards operations allow to:

- HVB ramp set (TC APID 1175)
- HVB DAC Vdrift reg set (TC APID 1176)
- HVB DAC Vbottom reg set (TC APID 1178)
- HVB DAC Vgem reg set (TC APID 1177)
- HVB control reg set (TC APID 1179)

The **HVB ramp set** operation allows to perform a ramp-on or ramp-off operation. Target voltages must be within the configurable operative range. If not, the TC is not accepted.
In table 5-2 are reported the default values for the operative range.

Table 5-2: Default Voltage Operative Ranges

DU Model	V drift Min [V]	V drift Max [V]	V bottom Min [V]	V bottom Max [V]	V Gem Min [V]	V Gem Max [V]
DU1	-3000	-1900	-430	-300	-469	-350

DU2	-3000	-1900	-430	-300	-454	-350
DU3	-3000	-1900	-430	-300	-454	-350

HVB ramp set telecommand accepts engineering values.
The nominal acquisition values (August 2021, Observatory TVAC) are reported in Table 5-3.

Table 5-3: Nominal engineering Values for DU models

DU Model	V drift [V]	V bottom [V]	V Gem [V]
FM1	-2800	-400	-470
FM2	-2800	-400	-458
FM3	-2800	-400	-444
FM4	-2800	-400	-444

Ramp-on operation is performed by first setting Vdrift voltage and then setting Vbottom and Vgem voltages.
When performing the ramps, the on-board SW checks the monitored voltage value before performing the next ramp step and aborts the procedure if a discrepancy greater than a configurable value (table 5-4) is detected.

Table 5-4: Default Ramp Up/Down voltages tolerances

DU Model	Vdrift engineering tolerance [V]	Vbottom engineering tolerance [V]	Vgem engineering tolerance [V]
DU1	80	80	80
DU2	20	20	20
DU3	35	35	35

The worst case of a ramp execution time is around 32 seconds.
The **HVB DAC Vdrift reg set**, **HVB DAC Vbottom reg set** and **HVB DAC Vgem reg set** operations allow to set content of Vdrift, Vbottom or Vgem DAC registers.
The TCs accept RAW values that must be calculated using the calibration curves loaded in MRAM and indicated in ANNEX B.3.
The content with respect to previous register value must be less than specified in table 5-4. This operation must be previously authorized by sending BEE Authorize telecommand.
The **HVB control reg set** operation allows to set content of HV Control register.

This operation must be previously authorized by sending BEE Authorize telecommand.

5.9.7 Filter and Calibration Wheels Operations

Filter and Calibration Wheels operations allow to:

- FCW set position (TC APID 1130)
- FCW step movement (TC APID 1131)
- FCW abort (TC APID 1132)

A complete wheel rotation of 360° takes 10 seconds to complete and is composed by 2000 steps.
The **FCW set position** operation allows to move the FCW with the centroid algorithm exploiting hall sensors detection.

During nominal operations the parameter 'HI POWER' has to be set to DISABLE. It can be enabled only in contingency cases with the support of the I2T.

The **FCW step movement** operation allows to move the FCW by a fixed number of steps. A maximum amount of 2000 steps (a complete rotation) can be requested with a single telecommand.

The **FCW abort** operation allows to abort any currently running movement, either using the centroid algorithm or fixed steps number.

The Baseline Operation is to alternate CW and CCW rotations on a regular basis: e.g. starting from Open position move CW (CCW) to the target position and then move CCW (CW) back to Open position.

Filter and Calibration Wheels are powered and operated directly by the DSU even if the DU 5V and 25V are switched OFF.

WARNING: In case of 14 seconds movement timeout an abort is automatically triggered by ASW. A DSU housekeeping parameter reports the number of FCW movement timeouts detected by the ASW.

WARNING: During ground operation, at ambient pressure, the FCW can be operated only if the HV values (Vdrift, Vbottom and Vgem) are 0.

5.9.8 DU Timing Configurations

DU Timing operations allow to:

- DU OBT time synchronization (TC APID 1110)

The DU OBT time synchronization operation allows to request a synchronization between the DSU master on-board time and the Detector Unit load on-board time. The synchronization is performed by writing the content of the Detector Unit OBT seconds counter with the value of the DSU OBT seconds counter, after the reception of a PPS signal.
This procedure is automatically triggered by the IXPE ASW after a successful +5V power-on sequence complete, nonetheless can be forced by sending this telecommand (e.g. after a leap second compensation).

6. INSTRUMENT NOMINAL OPERATION

Instrument nominal operations can be configured from STAND-BY operative mode by positioning the Filter and Calibration Wheels, switching-on (5V and 25V) and configuring the Detector Units, and performing ramp-on on High Voltages Boards (see chap. 5.).

6.1 Instrument Observation

The scientific data acquisition can be activate entering OBSERVATION operative mode.
Entering OBSERVATION operative mode either a successful observation report or an unsuccessful observation report event telemetry packet is sent to ground for each DU.
As soon as a DU successfully starts observation, depending on active configuration, events report and DSU ratemeters report telemetries start to be generated:

- Detector Unit events report (TM APID 1118)
- Detector Unit pixel scan events report (TM APID 1119)
- Detector Unit pedestal calibration events report (TM APID 1120)
- DSU ratemeters report (TM APID 1203)

Science data generation can be disabled from OBSERVATION operative mode by entering STAND-BY operative mode.

6.1.1 Nominal Acquisition

Preliminary activities to the nominal acquisition are:

- HV Ramp Set at nominal values.
- Move FCW in open position to collect photons from celestial sources or in calibration positions (Cal A, Cal B, Cal C and Cal D).
- configure the pixel mask setup
- configure the BEE Setup

In order to setup the DU for a nominal acquisition the following green parameters into the BEE Setup must be configured:

Mnemonic	Parameter Name	Default Value
UUU0256X	DAC V TH CTRL	-
UUU0257X	DAC V TEST CTRL	200
UUU0258X	SDI START ADDR	8192
UUU0259X	SDI CLK DIVIDER	4
UUU0260N	SDI RTX WAIT	250
UUU0261X	WIN D UPPER LIMIT	-

UUU0262X	WIN D LOW LIMIT	-
UUU0263X	ADC XPOL CLK DIV	8
UUU0264N	CLK PER CYCLES	8
UUU0265N	CLK SHIFT CYCLES	0
UUU0266S	ADC XPOL CLK DF CSN	ON
UUU0267S	ADC XPOL G0	OFF
UUU0268S	ADC XPOL G1	OFF
UUU0269S	ADC TYPE	ST
UUU0270X	PHA ULIM THR	-
UUU0271X	PHA LLIM THR	-
UUU0272N	DIAG EVENTS PERIOD	-
UUU0273X	XPOL DISCH WIDTH	25000
UUU0274X	XPOL MH CYCLES	320
UUU0275X	XPOL ZS THR	-
UUU0276N	XPOL PED NUMBER	-
UUU0277X	XPOL INJ WIDTH	0
UUU0278X	XPOL INJ PERIOD	0
UUU0279N	SCAN STEPS X	0
UUU0280N	SCAN STEPS Y	0
UUU0281N	SCAN DELTA X	0
UUU0282N	SCAN DELTA Y	0
UUU0283N	PULSES PER PIXEL	0
UUU0284X	XPOL X ADDR	0
UUU0285X	XPOL Y ADDR	0
UUU0286S	PIXEL SCAN ENABLE	DISABLED
UUU0287X	XPOL CONFIG REG	0x0E
UUU0288S	XPOL SI MODE	CORE_LOGIC
UUU0289S	MUX SELECT	CL_XPOL_WRITE
UUU0290S	HK1 ENABLE	ENABLE
UUU0291S	HK2 ENABLE	ENABLE
UUU0292S	HK3 ENABLE	ENABLE
UUU0293X	HK1 CHANNEL MASK	0xff
UUU0294X	HK2 CHANNEL MASK	0xff
UUU0295X	HK3 CHANNEL MASK	0xff

DAC V TH CTR - Trigger threshold: it is a fundamental parameter for detector operations. Typical values for trigger threshold are around 200—250 mV above VREF.

WIN D UPPER LIMIT - Maximum ROI size to start event readout in the BEE: these parameters are used to

avoid reading too big. The maximum size is usually set between 1000 and 3952 pixels.
WIN D LOW LIMIT - Minimum ROI size to start event readout in the BEE: these parameters are used to avoid reading too small. The minimum theoretical ROI size for a corner pixel is 120.
PHA ULIM THR - Maximum Threshold for the counter of events that have a pulse height greater then this value
PHA LLIM THR – Minimum Threshold for the counter of events that have a pulse height less than this value
DIAG EVENTS PERIOD - The period of diagnostic events has to be set in a way compatible with the available bandwidth. For ground testing and small event rate a value of 1 in the diagnostic_events_refresh_period register maximizes the amount of information saved to disk. The best value for flight operation must be of the order of 100 or higher.
XPOL ZS THR - this parameter is used for event compression and formatting. It's the most important parameter in order to lower the events packet size.

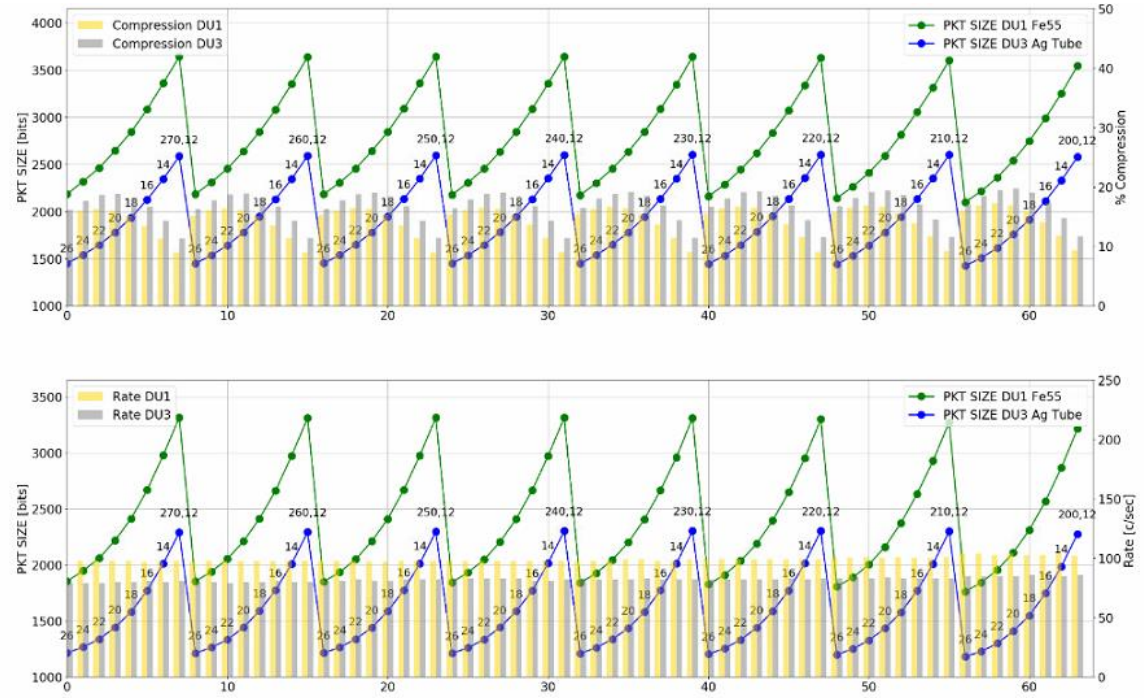


Figure 6-1: PKT SIZE variation respect XPOL_ZS_THR and DAC_V_TH_CTR

Fig 6-1

In Figure 6-1 is reported the PKT SIZE varying XPOL ZS THR and DAC V TH CTR respectively between 12 and 26 DAC and between 270 and 200 DAC. XPOL ZS THR effect strongly the packet dimension instead **DAC V TH CTR** effect less the packet dimension and has relevant effect on noise triggering rate.
XPOL PED NUMBER - the number of pedestal samples to be acquired for the event-by-event pedestal subtraction, usually set to 1.

6.1.2 Pixel Scan

This mode is used for diagnostic purposes.
Preliminary activities to the nominal acquisition are:

- HV Ramp Set at 0 values.
- Move FCW to close position (not mandatory)
- configure the pixel mask setup
- configure the BEE Setup

In order to setup the DU for a pixel scan the following green parameter of the DU BEE Setup has to be configured:

Mnemonic	Parameter Name	Default Value
UUU0256X	DAC V TH CTRL	-
UUU0257X	DAC V TEST CTRL	200
UUU0258X	SDI START ADDR	8192
UUU0259X	SDI CLK DIVIDER	4
UUU0260N	SDI RTX WAIT	250
UUU0261X	WIN D UPPER LIMIT	-
UUU0262X	WIN D LOW LIMIT	-
UUU0263X	ADC XPOL CLK DIV	8
UUU0264N	CLK PER CYCLES	8
UUU0265N	CLK SHIFT CYCLES	0
UUU0266S	ADC XPOL CLK DF CSN	ON
UUU0267S	ADC XPOL G0	OFF
UUU0268S	ADC XPOL G1	OFF
UUU0269S	ADC TYPE	ST
UUU0270X	PHA ULIM THR	-
UUU0271X	PHA LLIM THR	-
UUU0272N	DIAG EVENTS PERIOD	0
UUU0273X	XPOL DISCH WIDTH	25000
UUU0274X	XPOL MH CYCLES	320
UUU0275X	XPOL ZS THR	0
UUU0276N	XPOL PED NUMBER	-
UUU0277X	XPOL INJ WIDTH	-
UUU0278X	XPOL INJ PERIOD	-
UUU0279N	SCAN STEPS X	-
UUU0280N	SCAN STEPS Y	-
UUU0281N	SCAN DELTA X	-

UUU0282N	SCAN DELTA Y	-
UUU0283N	PULSES PER PIXEL	-
UUU0284X	XPOL X ADDR	-
UUU0285X	XPOL Y ADDR	-
UUU0286S	PIXEL SCAN ENABLE	ENABLED
UUU0287X	XPOL CONFIG REG	0x0E
UUU0288S	XPOL SI MODE	CORE_LOGIC
UUU0289S	MUX SELECT	CL_XPOL_WRITE
UUU0290S	HK1 ENABLE	ENABLE
UUU0291S	HK2 ENABLE	ENABLE
UUU0292S	HK3 ENABLE	ENABLE
UUU0293X	HK1 CHANNEL MASK	0xff
UUU0294X	HK2 CHANNEL MASK	0xff
UUU0295X	HK3 CHANNEL MASK	0xff

DAC V TH CTR - Trigger threshold: it is a fundamental parameter for detector operation. Typical values for trigger threshold are around 200—250 mV above VREF.
WIN D UPPER LIMIT - Maximum ROI size to start event readout in the BEE: these parameters are used to avoid reading too big. The maximum size is usually set between 1000 and 3952 pixels.
WIN D LOW LIMIT - Minimum ROI size to start event readout in the BEE: these parameters are used to avoid reading too small. The minimum theoretical ROI size for a corner pixel is 120.
PHA ULIM THR - Maximum Threshold for the counter of events that have a pulse height greater then this value
PHA LLIM THR – Minimum Threshold for the counter of events that have a pulse height less then this value
XPOL PED NUMBER - the number of pedestal samples to be acquired for the event-by-event pedestal subtraction usually set to 1.
XPOL INJ WIDTH - Indicate the width of the write pulse, expressed in ASIC-clock cycles.
XPOL INJ PERIOD - Indicate the charge injection period expressed in ASIC-clock cycles.
SCAN STEPS X, SCAN STEPS Y, SCAN DELTA X, SCAN DELTA Y, PULSES PER PIXEL, XPOL X ADDR, XPOL Y ADDR - When enabled, the pixel scan starts at the pixel with coordinate (XPOL X ADDR, XPOL Y ADDR) and then this coordinate changes by adding SCAN DELTA X pixels on the column, for SCAN STEPS X times. This is repeated for SCAN STEPS Y times on the rows, with a delta of SCAN DELTA Y. For each pixel, the DU acquires PULSES PER PIXEL events.

It is also possible to stimulate one pixel (XPOL X ADDR, XPOL Y ADDR) only setting SCAN STEPS X, SCAN STEPS Y, SCAN DELTA X, SCAN DELTA Y equal to 0. This special Pixel Scan is called Charge Injection.
Notice that if there is a non-functional pixel the sequence may be stuck in that pixel, since it never reaches

that required number of events per pixels. To avoid this problem, it is recommended to have a small rate of noisy pixels, by lowering the trigger threshold a bit with respect to nominal operation.

6.1.3 Pedestal Calibration

The Pedestal Calibration mode is configured as the pixel scan.
The only difference is the number of pedestals that are automatically set by the DSU SW to zero.
Events are downloaded without pedestals subtraction.

6.1.4 Timing Calibration

This mode is used for diagnostic purposes in order to check the timing registers alignment in the DSU and DUs.
Preliminary activities to the nominal acquisition are:

- HV Ramp Set at 0 values.
- Move FCW to close position (not mandatory)
- configure the pixel mask setup
- configure the BEE Setup

In order to setup the DU to receive signals from the DSU the following green parameter of the DU BEE Setup has to be configured:

Mnemonic	Parameter Name	Default Value
UUU0256X	DAC V TH CTRL	250
UUU0257X	DAC V TEST CTRL	200
UUU0258X	SDI START ADDR	8192
UUU0259X	SDI CLK DIVIDER	4
UUU0260N	SDI RTX WAIT	250
UUU0261X	WIN D UPPER LIMIT	3952
UUU0262X	WIN D LOW LIMIT	120
UUU0263X	ADC XPOL CLK DIV	8
UUU0264N	CLK PER CYCLES	8
UUU0265N	CLK SHIFT CYCLES	0
UUU0266S	ADC XPOL CLK DF CSN	ON
UUU0267S	ADC XPOL G0	OFF
UUU0268S	ADC XPOL G1	OFF
UUU0269S	ADC TYPE	ST
UUU0270X	PHA ULIM THR	1050
UUU0271X	PHA LLIM THR	1051

UUU0272N	DIAG EVENTS PERIOD	0
UUU0273X	XPOL DISCH WIDTH	25000
UUU0274X	XPOL MH CYCLES	320
UUU0275X	XPOL ZS THR	18
UUU0276N	XPOL PED NUMBER	1
UUU0277X	XPOL INJ WIDTH	0
UUU0278X	XPOL INJ PERIOD	0
UUU0279N	SCAN STEPS X	0
UUU0280N	SCAN STEPS Y	0
UUU0281N	SCAN DELTA X	0
UUU0282N	SCAN DELTA Y	0
UUU0283N	PULSES PER PIXEL	0
UUU0284X	XPOL X ADDR	130
UUU0285X	XPOL Y ADDR	150
UUU0286S	PIXEL SCAN ENABLE	DISABLED
UUU0287X	XPOL CONFIG REG	0x0E
UUU0288S	XPOL SI MODE	CORE_LOGIC
UUU0289S	MUX SELECT	ALARM_IN
UUU0290S	HK1 ENABLE	ENABLE
UUU0291S	HK2 ENABLE	ENABLE
UUU0292S	HK3 ENABLE	ENABLE
UUU0293X	HK1 CHANNEL MASK	0xff

Timing operations allow to:

- DU pulse start (TC APID 1191)
- DU pulse stop (TC APID 1192)

The DU pulse start operation allows to start sending a pulse train on the ALARM IN line of a specified Detector Unit at a defined time.

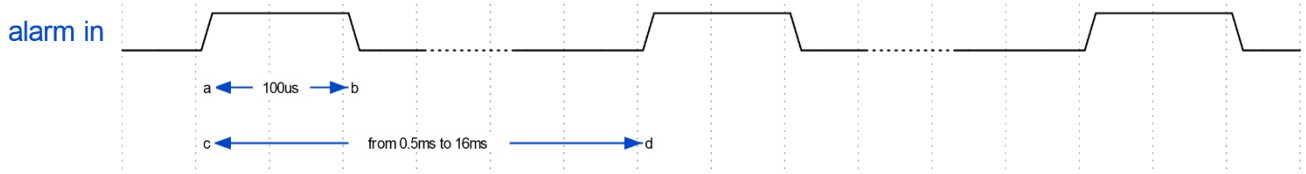


Figure 6-2: Alarm in pulse

The telecommand allows to set an absolute start time at which the alarm in pulse will be generated by the DSU FPGA and a pulse period expressed in milliseconds (with 0.5ms granularity). The duration of the spike is fixed to 100µs.

The **DU pulse stop** operation allows to stop sending a pulse train on the ALARM IN line of a specified Detector Unit.

6.2 Instrument South Atlantic Anomaly Crossing

During the South Atlantic Area crossing SAA operative mode must be entered in order to:

- Disable science data acquisition
- Ramp-off HVBs to lowest Vbottom and Vgem values

SAA operative mode can be left by entering either STAND-BY or OBSERVATION operative modes.
Exiting the SAA operative mode, a ramp-on to previous voltages is performed on all HVBs.
Science data generation is enabled only if OBSERVATION operative mode is entered.

7. INSTRUMENT ON-BOARD MONITORING AND CONTINGENCIES

7.1 Instrument Fault Detection and Isolation Recovery (FDIR)

All the HKs and Scientific Ratemeters collected by the DSU SW can be checked on-board to verify that they are acceptable for the safety of the Instrument.
In case this check produces a negative result, the SW reacts autonomously in order to try to guarantee the Instrument safety.
The IXPE application software FDIR feature is based on a configurable list of rules to monitor a set of parameters and to act in case of rule violation. The user can configure up to 128 rules, checking any of the parameters stored into the on-board data-pool and reported in Table 7-8. The FDIR rules are checked at a frequency of 10Hz. The list of available checks is:

- LESS THAN
- MORE THAN
- EQUAL TO
- NOT EQUAL TO
- IN RANGE
- OUT RANGE
- DELTA EXCEED

LESS THAN, MORE THAN, EQUAL TO and NOT EQUAL TO check a parameter with respect to a reference value. IN RANGE and OUT RANGE check a parameter with respect to a range composed by a minimum and a maximum value. DELTA EXCEED checks a parameter increment with respect to its previous value, where previous value is the value of the parameter at the previous FDIR loop execution; If the FDIR rules is evaluated positively, then an optional action can be performed by the on-board software. The list of available actions is:

- NO ACTION
- DU1 HV RAMP OFF
- DU1 POWER OFF
- DU2 HV RAMP OFF
- DU2 POWER OFF
- DU3 HV RAMP OFF
- DU3 POWER OFF
- DU ALL POWER OFF
- ENTER RECOVERY
- ENTER SAFE

NO ACTION doesn't perform any action, but the rule evaluation result (either TRUE or FALSE) is stored on-board into the data-pool, and thus available to compose more complex rules as described below.
DUx HV RAMP OFF performs a ramp-off on the selected Detector Unit without switching the Detector

Unit off.
DUx POWER OFF performs a complete shut-down of the selected Detector Unit, by performing a ramp-off and then by switching-off both +5V and +25V.
DU ALL POWER OFF performs a complete switch-off of all three Detector Units.
ENTER RECOVERY performs a complete switch-off of all three Detector Units and selects CLOSED position on all three Filter and Calibration Wheels, then the operative mode is changed to SAFE.
ENTER SAFE changes the operative mode to SAFE, preserving the current status of the Detector Units and the Filter and Calibration Wheels.
If an action involving the Detector Units is executed, then the selected Detector Unit rejects any telecommand from ground for 45 seconds to avoid collisions between FDIR and ground control.
Each FDIR rule has a configurable flag that enable or disable the rule evaluation. Rule evaluation can be controlled also by the value of up to three other parameters stored on-board. On each of the three control parameters a mask can be applied, and the resulting value is compared with respect to a reference value. The three comparisons are composed in logical AND operation and used to decide if the FDIR rule must be evaluated or not (e.g. a housekeeping parameter stored in a Detector Unit BEE register can be checked only if the Detector Unit status is ON and the corresponding bit in the housekeeping control register is set to 1).
FDIR rules definitions can be controlled with the following telecommands:

- FDIR rule set (TC APID 1060)
- FDIR rule get (TC APID 1061)

The **FDIR rule set** operation allows to configure on-board the details of the selected FDIR rule.
The **FDIR rule get** operation allows to receive an **FDIR rule report** (TM APID 1280) containing the details of the selected on-board configured FDIR rule.
If an FDIR rule is evaluated positively, then an **FDIR rule violation report** (TM APID 1236) is generated and sent to ground.
Refers to the Annex C for the list of configuration parameters and Annex B for the FDIR already stored on board by I2T.

7.1.1 DU Fault Detection and Isolation Recovery

Some monitor parameters implemented into the DU are checked directly by the BEE FPGA in order to react immediately to an out of range (<1ms).

In this case an alarm signal is sent through a dedicate line to the DSU that immediately switch of drastically the DU in contingency.

See chap. 5.9.4 and Annex B.8 for details on alarm configuration and default.

7.2 Internal Error Conditions

Specific ASW error conditions are detected and reported by sending unsolicited events telemetry:

- Buffer desaturation report (TM APID 1400)
- Buffer saturation report (TM APID 1401)
- Unsuccessful observation report (TM APID 1402)
- Successful observation report (TM APID 1403)
- Power failure report (TM APID 1404)
- Health check failure report (TM APID1405)
- SDI reset report (TM APID1406)

Buffer desaturation report is sent to ground when the SDI FPGA internal buffers are available to receive new data.
Buffer saturation report is sent to ground when DSU FPGA detects a saturation of its internal buffers used to store science data from the Detector Units. The DSU FPGA temporary inhibits science data generation until the buffer is processed and available to receive new data.
Unsuccessful observation report is sent to ground when by entering the OBSERVATION operative mode, the Detector Unit fails started generating science data.
Successful observation report is sent to ground when by entering the OBSERVATION operative mode, the Detector Unit successfully starts generating science data.
Power failure report is sent to ground when a problem is detected on either +5V or +25V power lines by the DSU, or an ALARM OUT signal is received from the DU. The failure report includes a parameter indicating which DU has been affected and the source of the detected problem.

Health check failure report is sent to ground when one of the following monitored DU housekeeping parameters exceeds a configurable threshold:

- LVPS 5V current monitor
- LVPS 3.3V current monitor
- LVPS 1.8V current monitor
- LVPS 1.5V temperature
- LVPS 1.8V temperature
- LVPS 3.3V temperature
- HV temperature 1
- HV temperature 2
- HV current monitor 1
- HV current monitor 2
- GPD temperature
- Temperature DAQ 1

- Temperature DAQ 2
- LVPS 1.5V current monitor
- HV drift voltage monitor
- HV top voltage monitor
- HV bottom voltage monitor
- HV current monitor 3

The threshold values can be stored in MRAM. The failing DU is switched-off after a ramp-off to zero volts.

This functionality has been developed on the DSU SW when the FDIR task was not yet implemented. Actually, It has been outdated by the FDIR task (par 7.1) and all these checks are disable by default in MRAM.

The **SDI Reset report** is sent to ground if a science data interface reset occur.

In case of software errors of type:

- **LEON3 CPU traps**
- **Software asserts**
- **RTOS internal errors**
- **LEON3 hardware watchdog**

The IXPE ASW stores a death report for further analysis in a dedicated area of MRAM and then halts the LEON3 CPU triggering a restart. The area allows to store up to 4 reports in a circular buffer (older reports are over-written by newer ones). Latest report can be requested by sending the following telecommand when in SAFE operative mode:

- Get death report (TC APID 1090)

The **Get death report** operation allows to receive a **Death report** (TM APID 1300) telemetry packet.

Otherwise all the death reports must be dumped as normal MRAM memory areas.
The MRAM memory addresses to retrieve the death reports are:
Number of stored death reports: 4
Address of current death report index: 0x1030000C (4 bytes)
Address of death reports:
DEATH_REPORT_BUFF_PTR[0] = 0x10300010
DEATH_REPORT_BUFF_PTR[1] = 0x10300204
DEATH_REPORT_BUFF_PTR[2] = 0x103003F8
DEATH_REPORT_BUFF_PTR[3] = 0x103005EC

Size of a single death report slot: 500 bytes

The structure of the death report dump is equal to the data field of the **Death report** (TM APID 1300) telemetry packet (see RD [4]).

After a reboot (warm reset) due to so ftware errors, the DSU boot software moves to Safe Patch and Dump mode because the ASW doesn't writes the magic number (see par 5.2.1).
The Safe Patch and Dump mode will be activated in order to permit further investigation by the ground control and I2T.
These errors don't affect the status of the DUs so when the ASW will be restarted the DSU will find the DUs powered.
In this particular case, the ASW will execute the following steps:
- ramp down the HVs (if at nominal values)
- switch of DU 5V and 25V
- close the FCWs (if open)
- move to SAFE mode

In case of contingency due to these errors, all the recovery actions must be evalueted with I2T.

7.3 External Error Conditions

Error conditions detected by the spacecraft that need a DSU restart [RD 9] are handled by sending the IXPE ASW a request to shut-down the instrument:

- DSU Shutdown (TC APID 1047)

The **DSU Shut-down** operation allows to:

- Move the FCWs to CLOSE position if required
- Perform a ramp-off on all HVBs if required
- Switch-off all DUs if required

These tasks are performed within the 45 seconds timeout before the spacecraft switches-off the +32V power line.

7.4 DU Reset Contingency

This operation permits to reset the content of the Detector Unit BEE bank registers:
• BEE reset (TC APID 1150)

The **BEE reset** operation allows to assert the RESET signal of the Detector Unit.
This operation must be previously authorized by sending BEE Authorize telecommand.

<u>This telecommand creates a discrepancy between the status of the hardware and its representation into the BEE bank register. This is highly dangerous with respect to the HVB configuration.</u>
<u>After a BEE reset TC the reset the HVB can't be commanded because the registers are not recognized in safe condition by the SW.</u>

In order to restore the control of the DU the following two actions can be performed:

1. Send the DSU Shutdown (TC APID 1047) to switch off the Units. In this case the DSU SW can't ramp down the HV of the DU reset. Anyway, after a timeout, will power off the unit drastically.
2. Restore the previous HVB configuration using the atomic HV Telecommands:
   - Enable DU HK generation sending the BEE SETUP TC
   - Verify on the telemetry previous the reset the Vdrift, Vgem and Vbottom raw values
   - Restore values in BEE HVB Registers with atomic TCs (HVB DAC VDRIFT SET, HVB DAC VGEM SET, HVB DAC VBOTTOM SET)
   - Ramped Down the HV
   - DU Power OFF

<u>These operations can be used only in contingency cases and only after discussions with I2T.</u>

7.5 HKs validity range

The HKs Nominal Range and Alarm Thresholds are reported in [AD 3] and [AD 6].

7.6 Known Anomalies on the Instrument

7.6.1 Errors on DU indexes

During the Instrument E2E Test RD[10],, we found a misalignment on the DU-DSU SDI interface when it is strongly stressed (>= 300 counts per second).

This is due to wrong ROI indexes reported into the DU Events:

Case 1: Min X > Max X or Min Y > Max Y

Case 2: Max X > 299 or Max Y > 350

The Case 1 causes a block on the DSU processing algorithm (orphan pixel removal). When this block occurs, after 1 second the DSU SW resets the SDI interface, reporting the operation with a SDI RESET REPORT (APID 1406), and automatically restart the acquisition producing successful operation reports (APID 1403).

<u>Consequently, no operations are needed from ground.</u>

During on ground test, at the maximum rate (>300 counts per second), we reported 38 Case 1 and 43 Case 2 across over 768e6 events.

This anomaly is negligible and doesn't effect on the capability of the instrument to satisfy the scientific data rates acquisition requirements.

During the same test, at lower rates (around 180 counts per second), we reported 0 Case 1 and 0 Case 2 across over 112e6 events

7.6.2 Errors on Time Keeping

During the Instrument E2E Test RD[10], we found few errors on the DU Events Time Keeping and on the DU Packets Time keeping.

These errors occur when the SDI interface is strongly stressed (>= 300 counts per second) and the DU events or the DU packets are tagged when a new PPS is produced.

In these rare cases the DU event or DU Packet are tagged with a second more.

During on ground test, at maximum rate, we reported 19 cases across over 768e6 events.

ANNEX A - Telemetries and Telecommands

A.1 Telemetry List

APID	Name	Description
1210	SUCCESSFUL COMMAND ACCEPTANCE	This telemetry is sent to ground when a command has successfully been accepted.
1211	UNSUCCESSFUL COMMAND ACCEPTANCE	This telemetry is sent to ground when a command has not been accepted.
1212	SUCCESSFUL COMMAND START EXEC	This telemetry is sent to ground when a command has successfully started its execution.
1213	UNSUCCESSFUL COMMAND START EXEC	This telemetry is sent to ground when a command has failed starting its execution.
1214	SUCCESSFUL COMMAND EXECUTION	This telemetry is sent to ground when a command has successfully completed its execution.
1215	UNSUCCESSFUL COMMAND EXECUTION	This telemetry is sent to ground when a command has failed completing its execution.
1201	ACTIVE HK REPORT	This telemetry is send to ground to answer a request for enabled housekeeping telemetry report.
1200	DSU HOUSEKEEPING	This telemetry is periodically sent to ground with DSU housekeeping.
1203	DSU RATEMETERS	This telemetry is sent to ground with DSU ratemeters with a fixed frequency of 1 Hz.
1230	OPMODE SUCCESSFUL CHANGE REPORT	This telemetry is sent to ground when a new operative mode is successfully reached.
1231	OPMODE FAILED CHANGE REPORT	This telemetry is sent to ground when a new operative mode switch fails.
1221	ASW START REPORT	This telemetry is sent to ground when the ASW completes its start-up sequence.
1232	CFG PARAMETERS DUMP 1	This telemetry is sent to ground after a complete ASW start-up to dump the content of the configurable parameters area.
1233	CFG PARAMETERS DUMP 2	This telemetry is sent to ground after a complete ASW start-up to dump the content of the configurable parameters area.
1234	CRC MEMORY CHECK FAILED REPORT	This telemetry is sent to ground when a CRC memory check performed at ASW start-up fails. CRC memory checks are performed for:
1235	MRAM ACCESS FAILED REPORT	This telemetry is sent to ground when an MRAM access (either write or read) fails.
1236	FDIR RULE VIOLATION REPORT	This telemetry is sent to ground to notify a detected FDIR rule violation.
1260	DUMP DSU MEMORY REPORT	This telemetry is sent to ground when a DSU memory dump request has been received.
1261	CHECK DSU MEMORY REPORT	This telemetry is sent to ground when a DSU memory check request has been received.
1262	GET INTEGER PARAM REPORT	This telemetry is sent to ground when a get integer parameter request has been

APID	Name	Description
		received.
1263	GET UINTEGER PARAM REPORT	This telemetry is sent to ground when a get unsigned integer parameter request has been received.
1280	FDIR RULE REPORT	This telemetry is sent to ground when an FDIR rule definition is requested.
1270	CONNECTION TEST REPORT	Connection test report.
1300	DEATH REPORT	Death report.
1321	DU#1 HK HIGH RATE	This telemetry if enabled is sent to ground periodically (every 1 second) containing Detector Unit 1 housekeeping information.
1322	DU#2 HK HIGH RATE	This telemetry if enabled is sent to ground periodically (every 1 seconds) containing Detector Unit 2 housekeeping information.
1323	DU#3 HK HIGH RATE	This telemetry if enabled is sent to ground periodically (every 1 seconds) containing Detector Unit 3 housekeeping information.
1324	DU#1 HK LOW RATE	This telemetry if enabled is sent to ground periodically (every 10 seconds) containing Detector Unit 1 housekeeping information.
1325	DU#2 HK LOW RATE	This telemetry if enabled is sent to ground periodically (every 10 seconds) containing Detector Unit 2 housekeeping information.
1326	DU#3 HK LOW RATE	This telemetry if enabled is sent to ground periodically (every 10 seconds) containing Detector Unit 3 housekeeping information.
1400	BUFFER DESATURATION	This telemetry is sent to ground if a buffer de-saturation event occurs on-board.
1401	BUFFER SATURATION	This telemetry is sent to ground if a buffer saturation event occurs on-board.
1402	UNSUCCESSFUL OBSERVATION	This telemetry is sent to ground to report an unsuccessful observation start or stop.
1403	SUCCESSFUL OBSERVATION	This telemetry is sent to ground to report a successful observation start.
1404	POWER FAILURE	This telemetry is sent to ground if a DU power failure is detected on-board.
1405	HEALTH CHECK FAILURE	This telemetry is sent to ground if a DU health parameter exceeded the threshold.
1406	SDI RESET REPORT	This telemetry is sent to ground if a science data interface resets.
1450	BEE REGS DUMP	This telemetry is sent to ground as a response to BEE registers dump request telecommand.
1451	BEE SRAM DUMP	This telemetry is sent to ground as a response to BEE SRAM dump request telecommand.
1118	DU#1 EVENTS	This telemetry is defined in document DSU-DU Interface Document (I2C-IAPS-IFF-ICD-001).
1119	DU#1 PIXEL SCAN EVENTS	This telemetry is defined in document DSU-DU Interface Document (I2C-IAPS-IFF-ICD-001).
1120	DU#1 PEDESTAL CAL EVENTS	This telemetry is defined in document DSU-DU Interface Document (I2C-IAPS-IFF-ICD-001).
1118	DU#2 EVENTS	This telemetry is defined in document DSU-DU Interface Document (I2C-IAPS-IFF-ICD-001).

APID	Name	Description
1119	DU#2 PIXEL SCAN EVENTS	This telemetry is defined in document DSU-DU Interface Document (I2C-IAPS-IFF-ICD-001).
1120	DU#2 PEDESTAL CAL EVENTS	This telemetry is defined in document DSU-DU Interface Document (I2C-IAPS-IFF-ICD-001).
1118	DU#3 EVENTS	This telemetry is defined in document DSU-DU Interface Document (I2C-IAPS-IFF-ICD-001).
1119	DU#3 PIXEL SCAN EVENTS	This telemetry is defined in document DSU-DU Interface Document (I2C-IAPS-IFF-ICD-001).
1120	DU#3 PEDESTAL CAL EVENTS	This telemetry is defined in document DSU-DU Interface Document (I2C-IAPS-IFF-ICD-001).
1202	BOOT HK REPORT	This is the Boot SW HK report packet.
1220	BOOT SW REPORT	This is the Boot SW Report packet.

A.2 Telecommand supported verification reports

The following table summarises the verification reports generated by each received telecommand:

APID	TC Description	Accept	Start	Exec
1010	Enable HK report generation	•		•
1011	Disable HK report generation	•		•
1012	Report active HK reports	•		•
1013	Set HK report generation period	•		•
1020	Load DSU memory	•		•
1021	Dump DSU memory	•		•
1022	Check DSU memory	•		•
1023	Set integer parameter	•		•
1024	Set unsigned integer parameter	•		•
1025	Get parameter	•		•
1027	Configure memory EDAC	•		•

APID	TC Description	Accept	Start	Exec
1040	Enter STAND-BY mode	•		•
1041	Enter MAINTENANCE mode	•		•
1042	Enter SAA mode	•		•
1043	Enter OBSERVATION mode	•		•
1044	Enter SAFE mode	•		•
1045	Reboot	•	•	
1046	Set run identifier	•		•
1047	DSU Shut-down	•	•	
1050	DSU OBT time set	•		•
1051	Time of Day message processing enable	•		•
1052	Time of Day message processing disable	•		•
1060	Monitoring parameters	•		•
1070	Perform connection test	•		•
1080	Boot copy ASW image into SRAM	•		•
1081	Boot jump to loaded ASW image	•		•
1090	Get death report	•		•
1100	BEE Load registers	•		•
1101	BEE Dump registers	•		•
1102	BEE Load SRAM	•		•
1103	BEE Dump SRAM	•		•
1104	BEE Load critical registers	•		•
1110	DU OBT time synchronization	•		•
1130	FCW set position	•		•
1131	FCW step movement	•		•
1132	FCW abort	•	•	
1140	Thermal controller enable	•		•
1141	Thermal controller disable	•		•
1150	BEE reset	•		•
1153	BEE mask pixels	•		•
1154	BEE mask pixels preset load	•		•

APID	TC Description	Accept	Start	Exec
1155	BEE mask pixels preset store	•		•
1156	BEE configuration setup	•		•
1157	BEE configuration setup load	•		•
1158	BEE configuration setup store	•		•
1159	BEE alarm configuration	•		•
1160	BEE alarm configuration load	•		•
1161	BEE alarm configuration store	•		•
1162	BEE authorize	•		•
1163	BEE observation setup	•		•
1175	HVB ramp set	•		•
1176	HVB DAC Vdrift reg set	•		•
1177	HVB DAC Vgem reg set	•		•
1178	HVB DAC Vbottom reg set	•		•
1179	HVB control reg set	•		•
1191	DU pulse start	•		•
1192	DU pulse stop	•		•
1193	DU power on 5V	•		•
1194	DU power on 25V	•		•
1195	DU power off	•		•

A.3 Telecommands List

APID	Name	Description
1000	TIME OF DAY MESSAGE	Time of Day message.
1010	ENABLE HK REPORT GENERATION	This telecommand is used to enable the generation of specified housekeeping telemetry report.
1011	DISABLE HK REPORT GENERATION	This telecommand is used to disable the generation of specified housekeeping telemetry report.
1012	REPORT ACTIVE HK REPORTS	This telecommand is used to request the enabled housekeeping telemetry reports.
1013	SET HK REPORT GENERATION PERIOD	This telecommand is used to set the generation period of specified housekeeping telemetry report.

APID	Name	Description
1020	LOAD DSU MEMORY	This telecommand is used to load a memory area.
1021	DUMP DSU MEMORY	This telecommand is used to dump a memory area.
1022	CHECK DSU MEMORY	This telecommand is used to calculate the checksum of a memory area.
1023	SET INTEGER PARAMETER	This telecommand is used to set on-board configuration integer parameters. Parameters are stored in MRAM and preserved among reboots.
1024	SET UNSIGNED INTEGER PARAMETER	This telecommand is used to set on-board configuration unsigned integer parameters. Parameters are stored in MRAM and preserved among reboots.
1025	GET PARAMETER	This telecommand is used to get the value of on-board configuration parameters.
1027	CONFIGURE MEMORY EDAC	This telecommand is used to configure memory EDAC.
1040	ENTER STAND-BY MODE	This telecommand is used to enter the STAND-BY operative mode.
1041	ENTER MAINTENANCE MODE	This telecommand is used to enter the MAINTENANCE operative mode.
1042	ENTER SAA MODE	This telecommand is used to enter the SAA operative mode.
1043	ENTER OBSERVATION MODE	This telecommand is used to enter the OBSERVATION operative mode.
1044	ENTER SAFE MODE	This telecommand is used to enter the SAFE operative mode.
1045	REBOOT	This telecommand is used to start the DSU reboot process.
1046	SET RUN IDENTIFIER	This telecommand is used to reset the run identifier to a specified value.
1047	DSU SHUT-DOWN	This telecommand is used to switch-off the instrument when a safe condition occurs at satellite level. The DSU reacts to this telecommand by performing a ramp-off of the HVs if required, Dus switch-off and FCWs set to CLOSED position.
1050	DSU OBT TIME SET	This telecommand is used to manually set the DSU Master OBT. Before sending this command the Time of Day message processing must be disabled via TC.
1051	TIME OF DAY MESSAGE PROCESSING ENABLE	This telecommand is used to enable the processing of Time of Day message from the S/C. In case of manual time set from ground the Time of Day message must be disabled.
1052	TIME OF DAY MESSAGE PROCESSING DISABLE	This telecommand is used to disable the processing of Time of Day message from the S/C. In case of manual time set from ground the Time of Day message must be disabled.
1060	FDIR RULE SET	This telecommand is used to set an FDIR rule parameters.
1061	FDIR RULE GET	This telecommand is used to request parameters of a defined FDIR rule.
1070	PERFORM CONNECTION TEST	This telecommand is used to perform a connection test between ground and on-board software.
1090	GET DEATH REPORT	This telecommand is used to request the latest death report stored on-board.
1100	BEE LOAD REGISTERS	This telecommand is used to load up to 8 BEE registers.
1101	BEE DUMP REGISTERS	This telecommand is used to dump up to 8 BEE registers.
1102	BEE LOAD SRAM	This telecommand is used to load BEE SRAM content.
1103	BEE DUMP SRAM	This telecommand is used to dump BEE SRAM content.
1104	BEE LOAD CRITICAL REGISTERS	"This telecommand is used to load up to 8 BEE critical or not critical registers.

APID	Name	Description
1130	FCW SET POSITION	This telecommand is used to move the Filter and Calibration wheel in a predefined position using hall sensors and centroid algorithm.
1131	FCW STEP MOVEMENT	This telecommand is used to move the Filter and Calibration wheel by a relative number of steps with respect to current position.
1132	FCW ABORT	This telecommand is used to abort any Filter and Calibration wheel movement currently active.
1140	THERMAL CONTROLLER ENABLE	This telecommand is used to enable DUs the thermal controller.
1141	THERMAL CONTROLLER DISABLE	This telecommand is used to disable DUs the thermal controller.
1150	BEE RESET	This telecommand is used to reset the BEE.
1153	BEE MASK PIXELS	This telecommand is used to mask selected pixels on the GPD.
1154	BEE MASK PIXELS PRESET LOAD	This telecommand is used load from MRAM a preset to mask selected pixels on the GPD.
1155	BEE MASK PIXELS PRESET STORE	This telecommand is used store on MRAM a preset to mask selected pixels on the GPD.
1156	BEE CONFIGURATION SETUP	This telecommand is used to configure the parameters related to the operative configuration of the BEEs.
1157	BEE CONFIGURATION SETUP LOAD	This telecommand is used to load a preset from MRAM to configure the parameters related to the operative configuration of the BEEs.
1158	BEE CONFIGURATION SETUP STORE	This telecommand is used to store a preset on MRAM to configure the parameters related to the operative configuration of the BEEs.
1159	BEE ALARM CONFIGURATION	This telecommand is used to configure the threshold values used to trigger DU alarm state.
1160	BEE ALARM CONFIGURATION LOAD	This telecommand is used load a preset from MRAM to to configure the threshold values used to trigger DU alarm state.
1161	BEE ALARM CONFIGURATION STORE	This telecommand is used store a preset on MRAM to to configure the threshold values used to trigger DU alarm state.
1162	BEE AUTHORIZE TC EXECUTION	This telecommand is used to authorize the execution of protected telecommands. The authorization window lasts 5 seconds.
1163	BEE OBSERVATION SETUP	This telecommand is used to configure the parameters related to the observation configuration of the BEEs.
1175	HVB RAMP SET	This telecommand is used to generate a ramp-on or a ramp-off on the HVB from current voltages to target ones. Target voltages must be within the valid operative range or 0V.
1176	HVB DAC VDRIFT REG SET	This telecommand is used to set the High Voltage Board drift voltage DAC value.
1177	HVB DAC VGEM REG SET	This telecommand is used to set the High Voltage Board gem voltage DAC value.
1178	HVB DAC VBOTTOM REG SET	This telecommand is used to set the High Voltage Board bottom voltage DAC value.
1179	HVB HV CONTROL REG SET	This telecommand is used to set the High Voltage Board ON status flag and STOP

APID	Name	Description
		status flag of the control register.
1191	DU PULSE START	This telecommand is used to start the generation of a pulse signal on ALARM IN line of the DUs.
1192	DU PULSE STOP	This telecommand is used to stop the generation of a pulse signal on ALARM IN line of the DUs.
1193	DU POWER ON 5V	This telecommand is used to switch-on the +5V power line of the DU.
1194	DU POWER ON 25V	This telecommand is used to switch-on the +25V power line of the DU.
1195	DU POWER OFF	This telecommand is used to switch-off both the +5V and +25V power lines of the DU.
1110	DU OBT TIME SYNCRONIZATION	This telecommand is used to synchronize DU on-board time to DSU MOBT time.
1080	BOOT COPY ASW	This telecommand is used to perform the copy of ASW to RAM.
1081	BOOT JUMP TO ADDRESS	This telecommand is used to jump to ASW.

A.4 Telecommand vs DSU operational mode

Telecommands marked with ● are allowed. Telecommands marked with ● are allowed, but should be used only in contingency operations, since the DU behaviour is undefined.

APID	Name	STAND-BY	OBSERVATION	SAA	MAINTENANCE	SAFE
1000	TIME OF DAY MESSAGE	●	●	●	●	●
1010	ENABLE HK REPORT GENERATION	●	●	●	●	●
1011	DISABLE HK REPORT GENERATION	●	●	●	●	●
1012	REPORT ACTIVE HK REPORTS	●	●	●	●	●
1013	SET HK REPORT GENERATION PERIOD	●	●	●	●	●
1020	LOAD DSU MEMORY				●	●
1021	DUMP DSU MEMORY				●	●
1022	CHECK DSU MEMORY				●	●
1023	SET INTEGER PARAMETER				●	●

APID	Name	STAND-BY	OBSERVATION	SAA	MAINTENANCE	SAFE
1024	SET UNSIGNED INTEGER PARAMETER				●	●
1025	GET PARAMETER				●	●
1027	CONFIGURE MEMORY EDAC				●	●
1040	ENTER STAND-BY MODE	●	●	●	●	●
1041	ENTER MAINTENANCE MODE	●			●	●
1042	ENTER SAA MODE	●	●	●		
1043	ENTER OBSERVATION MODE	●	●	●		
1044	ENTER SAFE MODE	●	●	●	●	●
1045	REBOOT					●
1046	SET RUN IDENTIFIER	●	●	●	●	●
1047	DSU SHUT-DOWN	●	●	●	●	●
1050	DSU OBT TIME SET	●	●	●	●	●
1051	TIME OF DAY MESSAGE PROCESSING ENABLE	●	●	●	●	●
1052	TIME OF DAY MESSAGE PROCESSING DISABLE	●	●	●	●	●
1060	FDIR RULE SET				●	
1061	FDIR RULE GET				●	
1070	PERFORM CONNECTION TEST	●	●	●	●	●
1090	GET DEATH REPORT					●
1100	BEE LOAD REGISTERS	●				
1101	BEE DUMP REGISTERS	●				
1102	BEE LOAD SRAM	●				
1103	BEE DUMP SRAM	●				

APID	Name	STAND-BY	OBSERVATION	SAA	MAINTENANCE	SAFE
1104	BEE LOAD CRITICAL REGISTERS	●				
1130	FCW SET POSITION	●	●	●		
1131	FCW STEP MOVEMENT	●	●	●		
1132	FCW ABORT	●	●	●		
1140	THERMAL CONTROLLER ENABLE	●	●	●	●	●
1141	THERMAL CONTROLLER DISABLE	●	●	●	●	●
1150	BEE RESET	●				
1153	BEE MASK PIXELS	●		●		
1154	BEE MASK PIXELS PRESET LOAD	●		●		
1155	BEE MASK PIXELS PRESET STORE	●	●	●	●	●
1156	BEE CONFIGURATION SETUP	●		●		
1157	BEE CONFIGURATION SETUP LOAD	●		●		
1158	BEE CONFIGURATION SETUP STORE	●	●	●	●	●
1159	BEE ALARM CONFIGURATION	●		●		
1160	BEE ALARM CONFIGURATION LOAD	●		●		
1161	BEE ALARM CONFIGURATION STORE	●	●	●	●	●
1162	BEE AUTHORIZE TC EXECUTION	●		●		
1163	BEE OBSERVATION SETUP	●		●		
1175	HVB RAMP SET	●		●		
1176	HVB DAC VDRIFT REG SET	●		●		
1177	HVB DAC VGEM REG SET	●		●		
1178	HVB DAC VBOTTOM REG SET	●		●		

APID	Name	STAND-BY	OBSERVATION	SAA	MAINTENANCE	SAFE
1179	HVB HV CONTROL REG SET	●		●		
1191	DU PULSE START	●	●	●	●	●
1192	DU PULSE STOP	●	●	●	●	●
1193	DU POWER ON 5V	●	●	●		
1194	DU POWER ON 25V	●	●	●		
1195	DU POWER OFF	●	●	●		
1110	DU OBT TIME SYNCRONIZATION	●	●	●		
1080	BOOT COPY ASW	-	-	-	-	-
1081	BOOT JUMP TO ADDRESS	-	-	-	-	-

A.5 Unsuccessful report reasons

Unsuccessful reports include the reason of the failure as described in the following table:

Error Code	Description
0	TC primary header invalid CCSDS APID error code
1	TC primary header invalid CCSDS length error code
2	TC invalid checksum error code
5	TC illegal or inconsistent application data error code
6	TC invalid header error code

Error Code	Description
10	Generic error code
11	Memory type error code
12	Memory address error code
13	Memory data length error code
14	Unallowed operative mode transition error code
15	TC handler not registered
16	Resource busy error code
17	Timeout error code
18	OnBoard Time request error code
19	TC not allowed in current operative mode error code
20	Pulse running error code
21	Pulse not running error code
22	Unauthorized telecommand error code
23	Requested value out of allowed range
24	Execution abort error code
25	Unknown parameter identifier error code

ANNEX B - MRAM DEFAULT CONFIGURATION

All the MRAM configuration are based on the following Instrument Configuration:

DSU – DU Connector set	DU
1	FM2
2	FM3
3	FM4

B.1 MRAM configurable Parameters

On-board configurable parameters can be modified only in MAINTENANCE mode. Some of these are updated at RUN-TIME, others require a REBOOT of the ASW to be effectively used (see column Upd).

Parameter Id	Description	Type	Upd
MISSION_EPOCH	Mission epoch in seconds. This is the difference of the CDS time epoch (1st Jan 1958 00:00:00.0000) and IXPE epoch (1st Jan 2017 00:00:00.0000) expressed in seconds.	UINT32	LIVE
SCRUB_CHUNK_SIZE	Scrub memory chunk size in bytes. This is the amount of SRAM scrubbed every scrub cycle (1 second).	UINT32	LIVE
SDI_RETRY_NUM	SDI link corrupted events retransmission retry number.	UINT8	LIVE
SDI_BUFF_LIMIT	SDI DSU FPGA buffer full threshold.	UINT16	LIVE
DU1_HOP_SCALED_KP	DU1 HOP scaled PI Kp. The scale factor is 1000 (e.g. a value of 10000 means Kp = 10).	UINT32	LIVE
DU1_HOP_SCALED_KI	DU1 HOP scaled PI Ki. The scale factor is 1000 (e.g. a value of 1000 means Ki = 1).	UINT32	LIVE
DU1_HOP_RAW_I_MAX	DU1 HOP raw maximum current. Default 0.27A.	UINT16	LIVE
DU1_HOP_RAW_T_TH	DU1 HOP raw threshold temp. Default 14°C.	UINT16	LIVE
DU1_HOP_RAW_T_TGT	DU1 HOP raw target temp. Default 12°C.	UINT16	LIVE
DU1_TEC_SCALED_KP	DU1 TEC scaled PI Kp. The scale factor is 1000 (e.g. a value of 10000 means Kp = 10).	UINT32	LIVE

Parameter Id	Description	Type	Upd
DU1_TEC_SCALED_KI	DU1 TEC scaled PI Ki. The scale factor is 1000 (e.g. a value of 1000 means Ki = 1).	UINT32	LIVE
DU1_TEC_RAW_I_MAX	DU1 TEC raw maximum current. Default 0.5A.	UINT16	LIVE
DU1_TEC_RAW_T_TH	DU1 TEC raw threshold temp. Default 24°C.	UINT16	LIVE
DU1_TEC_RAW_T_TGT	DU1 TEC raw target temp. Default 26°C.	UINT16	LIVE
DU2_HOP_SCALED_KP	DU2 HOP scaled PI Kp. The scale factor is 1000 (e.g. a value of 10000 means Kp = 10).	UINT32	LIVE
DU2_HOP_SCALED_KI	DU2 HOP scaled PI Ki. The scale factor is 1000 (e.g. a value of 1000 means Ki = 1).	UINT32	LIVE
DU2_HOP_RAW_I_MAX	DU2 HOP raw maximum current. Default 0.27A.	UINT16	LIVE
DU2_HOP_RAW_T_TH	DU2 HOP raw threshold temp. Default 14°C.	UINT16	LIVE
DU2_HOP_RAW_T_TGT	DU2 HOP raw target temp. Default 12°C.	UINT16	LIVE
DU2_TEC_SCALED_KP	DU2 TEC scaled PI Kp. The scale factor is 1000 (e.g. a value of 10000 means Kp = 10).	UINT32	LIVE
DU2_TEC_SCALED_KI	DU2 TEC scaled PI Ki. The scale factor is 1000 (e.g. a value of 1000 means Ki = 1).	UINT32	LIVE
DU2_TEC_RAW_I_MAX	DU2 TEC raw maximum current. Default 0.5A.	UINT16	LIVE
DU2_TEC_RAW_T_TH	DU2 TEC raw threshold temp. Default 24°C.	UINT16	LIVE
DU2_TEC_RAW_T_TGT	DU2 TEC raw target temp. Default 26°C.	UINT16	LIVE
DU3_HOP_SCALED_KP	DU3 HOP scaled PI Kp. The scale factor is 1000 (e.g. a value of 10000 means Kp = 10).	UINT32	LIVE
DU3_HOP_SCALED_KI	DU3 HOP scaled PI Ki. The scale factor is 1000 (e.g. a value of 1000 means Ki = 1).	UINT32	LIVE
DU3_HOP_RAW_I_MAX	DU3 HOP raw maximum current. Default 0.27A.	UINT16	LIVE
DU3_HOP_RAW_T_TH	DU3 HOP raw threshold temp. Default 14°C.	UINT16	LIVE

Parameter Id	Description	Type	Upd
DU3_HOP_RAW_T_TGT	DU3 HOP raw target temp. Default 12°C.	UINT16	LIVE
DU3_TEC_SCALED_KP	DU3 TEC scaled PI Kp. The scale factor is 1000 (e.g. a value of 10000 means Kp = 10).	UINT32	LIVE
DU3_TEC_SCALED_KI	DU3 TEC scaled PI Ki. The scale factor is 1000 (e.g. a value of 1000 means Ki = 1).	UINT32	LIVE
DU3_TEC_RAW_I_MAX	DU3 TEC raw maximum current. Default 0.5A.	UINT16	LIVE
DU3_TEC_RAW_T_TH	DU3 TEC raw threshold temp. Default 24*C.	UINT16	LIVE
DU3_TEC_RAW_T_TGT	DU3 TEC raw target temp. Default 26°C.	UINT16	LIVE
DU1_CCI_SPEED_DIV	DU1 CCI link speed divider (i.e. 2 = 5 MHz; 3 = 2.5 MHz).	UINT8	LIVE
DU2_CCI_SPEED_DIV	DU2 CCI link speed divider (i.e. 2 = 5 MHz; 3 = 2.5 MHz).	UINT8	LIVE
DU3_CCI_SPEED_DIV	DU3 CCI link speed divider (i.e. 2 = 5 MHz; 3 = 2.5 MHz).	UINT8	LIVE
DU1_CTR_VDRFT_S_M*	DU1 ctrl Vdrift scaled multiplier. The scale factor is 100000 (e.g. a value of 110220 means multiplier = 1.1022)	INT32	BOOT
DU1_CTR_VDRFT_S_O*	DU1 ctrl Vdrift scaled offset. The scale factor is 100000 (e.g. a value of 410040000 means offset = 4100.4)	INT32	BOOT
DU1_CTR_VBTTM_S_M*	DU1 ctrl Vbottom scaled multiplier. The scale factor is 100000 (e.g. a value of 649560 means multiplier = 6.4956)	INT32	BOOT
DU1_CTR_VBTTM_S_O*	DU1 ctrl Vbottom scaled offset. The scale factor is 100000 (e.g. a value of 409310000 means offset = 4093.1)	INT32	BOOT
DU1_CTR_VGEM_S_M*	DU1 ctrl Vgem scaled multiplier. The scale factor is 100000 (e.g. a value of 649950 means multiplier = 6.4995)	INT32	BOOT
DU1_CTR_VGEM_S_O*	DU1 ctrl Vgem scaled offset. The scale factor is 100000 (e.g. a value of 410490000 means offset = 4104.9)	INT32	BOOT
DU1_MON_VDRFT_S_M*	DU1 mon Vdrift scaled multiplier. The scale factor is 100000 (e.g. a value of -93390 means multiplier = -0.9339)	INT32	BOOT
DU1_MON_VDRFT_S_O*	DU1 mon Vdrift scaled offset. The scale factor is 100000 (e.g. a value of 310840 means offset = 3.1084)	INT32	BOOT

Parameter Id	Description	Type	Upd
DU1_MON_VBTTM_S_M*	DU1 mon Vbottom scaled multiplier. The scale factor is 100000 (e.g. a value of -15880 means multiplier = -0.1588)	INT32	BOOT
DU1_MON_VBTTM_S_O*	DU1 mon Vbottom scaled offset. The scale factor is 100000 (e.g. a value of 525630 means offset = 5.2563)	INT32	BOOT
DU1_MON_VTOP_S_M*	DU1 mon Vtop scaled multiplier. The scale factor is 100000 (e.g. a value of -31580 means multiplier = -0.3158)	INT32	BOOT
DU1_MON_VTOP_S_O*	DU1 mon Vtop scaled offset. The scale factor is 100000 (e.g. a value of 344180 means offset = 3.4418)	INT32	BOOT
DU2_CTR_VDRFT_S_M*	DU2 ctrl Vdrift scaled multiplier. The scale factor is 100000 (e.g. a value of 110220 means multiplier = 1.1022)	INT32	BOOT
DU2_CTR_VDRFT_S_O*	DU2 ctrl Vdrift scaled offset. The scale factor is 100000 (e.g. a value of 410040000 means offset = 4100.4)	INT32	BOOT
DU2_CTR_VBTTM_S_M*	DU2 ctrl Vbottom scaled multiplier. The scale factor is 100000 (e.g. a value of 649560 means multiplier = 6.4956)	INT32	BOOT
DU2_CTR_VBTTM_S_O*	DU2 ctrl Vbottom scaled offset. The scale factor is 100000 (e.g. a value of 409310000 means offset = 4093.1)	INT32	BOOT
DU2_CTR_VGEM_S_M*	DU2 ctrl Vgem scaled multiplier. The scale factor is 100000 (e.g. a value of 649950 means multiplier = 6.4995)	INT32	BOOT
DU2_CTR_VGEM_S_O*	DU2 ctrl Vgem scaled offset. The scale factor is 100000 (e.g. a value of 410490000 means offset = 4104.9)	INT32	BOOT
DU2_MON_VDRFT_S_M*	DU2 mon Vdrift scaled multiplier. The scale factor is 100000 (e.g. a value of -93390 means multiplier = -0.9339)	INT32	BOOT
DU2_MON_VDRFT_S_O*	DU2 mon Vdrift scaled offset. The scale factor is 100000 (e.g. a value of 310840 means offset = 3.1084)	INT32	BOOT
DU2_MON_VBTTM_S_M*	DU2 mon Vbottom scaled multiplier. The scale factor is 100000 (e.g. a value of -15880 means multiplier = -0.1588)	INT32	BOOT
DU2_MON_VBTTM_S_O*	DU2 mon Vbottom scaled offset. The scale factor is 100000 (e.g. a value of 525630 means offset = 5.2563)	INT32	BOOT

Parameter Id	Description	Type	Upd
DU2_MON_VTOP_S_M*	DU2 mon Vtop scaled multiplier. The scale factor is 100000 (e.g. a value of -31580 means multiplier = -0.3158)	INT32	BOOT
DU2_MON_VTOP_S_O*	DU2 mon Vtop scaled offset. The scale factor is 100000 (e.g. a value of 344180 means offset = 3.4418)	INT32	BOOT
DU3_CTR_VDRFT_S_M*	DU3 ctrl Vdrift scaled multiplier. The scale factor is 100000 (e.g. a value of 110220 means multiplier = 1.1022)	INT32	BOOT
DU3_CTR_VDRFT_S_O*	DU3 ctrl Vdrift scaled offset. The scale factor is 100000 (e.g. a value of 410040000 means offset = 4100.4)	INT32	BOOT
DU3_CTR_VBTTM_S_M*	DU3 ctrl Vbottom scaled multiplier. The scale factor is 100000 (e.g. a value of 649560 means multiplier = 6.4956)	INT32	BOOT
DU3_CTR_VBTTM_S_O*	DU3 ctrl Vbottom scaled offset. The scale factor is 100000 (e.g. a value of 409310000 means offset = 4093.1)	INT32	BOOT
DU3_CTR_VGEM_S_M*	DU3 ctrl Vgem scaled multiplier. The scale factor is 100000 (e.g. a value of 649950 means multiplier = 6.4995)	INT32	BOOT
DU3_CTR_VGEM_S_O*	DU3 ctrl Vgem scaled offset. The scale factor is 100000 (e.g. a value of 410490000 means offset = 4104.9)	INT32	BOOT
DU3_MON_VDRFT_S_M*	DU3 mon Vdrift scaled multiplier. The scale factor is 100000 (e.g. a value of -93390 means multiplier = -0.9339)	INT32	BOOT
DU3_MON_VDRFT_S_O*	DU3 mon Vdrift scaled offset. The scale factor is 100000 (e.g. a value of 310840 means offset = 3.1084)	INT32	BOOT
DU3_MON_VBTTM_S_M*	DU3 mon Vbottom scaled multiplier. The scale factor is 100000 (e.g. a value of -15880 means multiplier = -0.1588)	INT32	BOOT
DU3_MON_VBTTM_S_O*	DU3 mon Vbottom scaled offset. The scale factor is 100000 (e.g. a value of 525630 means offset = 5.2563)	INT32	BOOT
DU3_MON_VTOP_S_M*	DU3 mon Vtop scaled multiplier. The scale factor is 100000 (e.g. a value of -31580 means multiplier = -0.3158)	INT32	BOOT
DU3_MON_VTOP_S_O*	DU3 mon Vtop scaled offset. The scale factor is 100000 (e.g. a value of 344180 means offset = 3.4418)	INT32	BOOT
DU1_VDRIFT_E_MIN	DU1 Vdrift engineering minimum value in volts.	INT16	BOOT

Parameter Id	Description	Type	Upd
DU1_VDRIFT_E_MAX	DU1 Vdrift engineering maximum value in volts.	INT16	BOOT
DU1_VBTTM_E_MIN	DU1 Vbottom engineering minimum value in volts.	INT16	BOOT
DU1_VBTTM_E_MAX	DU1 Vbottom engineering maximum value in volts.	INT16	BOOT
DU1_VGEM_E_MIN	DU1 Vgem engineering minimum value in volts.	INT16	BOOT
DU1_VGEM_E_MAX	DU1 Vgem engineering maximum value in volts.	INT16	BOOT
DU2_VDRIFT_E_MIN	DU2 Vdrift engineering minimum value in volts.	INT16	BOOT
DU2_VDRIFT_E_MAX	DU2 Vdrift engineering maximum value in volts.	INT16	BOOT
DU2_VBTTM_E_MIN	DU2 Vbottom engineering minimum value in volts.	INT16	BOOT
DU2_VBTTM_E_MAX	DU2 Vbottom engineering maximum value in volts.	INT16	BOOT
DU2_VGEM_E_MIN	DU2 Vgem engineering minimum value in volts.	INT16	BOOT
DU2_VGEM_E_MAX	DU2 Vgem engineering maximum value in volts.	INT16	BOOT
DU3_VDRIFT_E_MIN	DU3 Vdrift engineering minimum value in volts.	INT16	BOOT
DU3_VDRIFT_E_MAX	DU3 Vdrift engineering maximum value in volts.	INT16	BOOT
DU3_VBTTM_E_MIN	DU3 Vbottom engineering minimum value in volts.	INT16	BOOT
DU3_VBTTM_E_MAX	DU3 Vbottom engineering maximum value in volts.	INT16	BOOT
DU3_VGEM_E_MIN	DU3 Vgem engineering minimum value in volts.	INT16	BOOT
DU3_VGEM_E_MAX	DU3 Vgem engineering maximum value in volts.	INT16	BOOT
DU1_VDRIFT_E_TOL	DU1 Vdrift engineering checks tolerance value in volts.	INT32	BOOT
DU1_VBTTM_E_TOL	DU1 Vbottom engineering checks tolerance value in volts.	INT32	BOOT
DU1_VGEM_E_TOL	DU1 Vgem engineering checks tolerance value in volts.	INT32	BOOT
DU2_VDRIFT_E_TOL	DU2 Vdrift engineering checks tolerance value in volts.	INT32	BOOT
DU2_VBTTM_E_TOL	DU2 Vbottom engineering checks tolerance value in volts.	INT32	BOOT

Parameter Id	Description	Type	Upd
DU2_VGEM_E_TOL	DU2 Vgem engineering checks tolerance value in volts.	INT32	BOOT
DU3_VDRIFT_E_TOL	DU3 Vdrift engineering checks tolerance value in volts.	INT32	BOOT
DU3_VBTTM_E_TOL	DU3 Vbottom engineering checks tolerance value in volts.	INT32	BOOT
DU3_VGEM_E_TOL	DU3 Vgem engineering checks tolerance value in volts.	INT32	BOOT
DU1_5V_CUR_R_THR	DU1 LVPS 5V current monitor raw threshold as reported in DU register.	UINT16	BOOT
DU1_3V3_CUR_R_THR	DU1 LVPS 33V current monitor raw threshold as reported in DU register.	UINT16	BOOT
DU1_1V8_CUR_R_THR	DU1 LVPS 18V current monitor raw threshold as reported in DU register.	UINT16	BOOT
DU1_1V5_TMP_R_THR	DU1 LVPS 15V temperature raw threshold as reported in DU register.	UINT16	BOOT
DU1_1V8_TMP_R_THR	DU1 LVPS 18V temperature raw threshold as reported in DU register.	UINT16	BOOT
DU1_3V3_TMP_R_THR	DU1 LVPS 33V temperature raw threshold as reported in DU register.	UINT16	BOOT
DU1_HV_TMP1_R_THR	DU1 HV temperature 1 raw threshold as reported in DU register.	UINT16	BOOT
DU1_HV_TMP2_R_THR	DU1 HV temperature 2 raw threshold as reported in DU register.	UINT16	BOOT
DU1_HV_CUR1_R_THR	DU1 HV current monitor 1 raw threshold as reported in DU register.	UINT16	BOOT
DU1_HV_CUR2_R_THR	DU1 HV current monitor 2 raw threshold as reported in DU register.	UINT16	BOOT
DU1_GPD_TMP_R_THR	DU1 GPD temperature raw threshold as reported in DU register.	UINT16	BOOT
DU1_DQ1_TMP_R_THR	DU1 Temperature DAQ 1 raw threshold as reported in DU register.	UINT16	BOOT
DU1_DQ2_TMP_R_THR	DU1 Temperature DAQ 2 raw threshold as reported in DU register.	UINT16	BOOT
DU1_1V5_CUR_R_THR	DU1 LVPS 15V current monitor raw threshold as reported in DU register.	UINT16	BOOT
DU1_HV_DR_V_R_THR	DU1 HV drift voltage monitor raw threshold as reported in DU register.	UINT16	BOOT
DU1_HV_TP_V_R_THR	DU1 HV top voltage monitor raw threshold as reported in DU register.	UINT16	BOOT
DU1_HV_BT_V_R_THR	DU1 HV bottom voltage monitor raw threshold as reported in DU register.	UINT16	BOOT
DU1_HV_CUR3_R_THR	DU1 HV current monitor 3 raw threshold as reported in DU register.	UINT16	BOOT

Parameter Id	Description	Type	Upd
DU2_5V_CUR_R_THR	DU2 LVPS 5V current monitor raw threshold as reported in DU register.	UINT16	BOOT
DU2_3V3_CUR_R_THR	DU2 LVPS 33V current monitor raw threshold as reported in DU register.	UINT16	BOOT
DU2_1V8_CUR_R_THR	DU2 LVPS 18V current monitor raw threshold as reported in DU register.	UINT16	BOOT
DU2_1V5_TMP_R_THR	DU2 LVPS 15V temperature raw threshold as reported in DU register.	UINT16	BOOT
DU2_1V8_TMP_R_THR	DU2 LVPS 18V temperature raw threshold as reported in DU register.	UINT16	BOOT
DU2_3V3_TMP_R_THR	DU2 LVPS 33V temperature raw threshold as reported in DU register.	UINT16	BOOT
DU2_HV_TMP1_R_THR	DU2 HV temperature 1 raw threshold as reported in DU register.	UINT16	BOOT
DU2_HV_TMP2_R_THR	DU2 HV temperature 2 raw threshold as reported in DU register.	UINT16	BOOT
DU2_HV_CUR1_R_THR	DU2 HV current monitor 1 raw threshold as reported in DU register.	UINT16	BOOT
DU2_HV_CUR2_R_THR	DU2 HV current monitor 2 raw threshold as reported in DU register.	UINT16	BOOT
DU2_GPD_TMP_R_THR	DU2 GPD temperature raw threshold as reported in DU register.	UINT16	BOOT
DU2_DQ1_TMP_R_THR	DU2 Temperature DAQ 1 raw threshold as reported in DU register.	UINT16	BOOT
DU2_DQ2_TMP_R_THR	DU2 Temperature DAQ 2 raw threshold as reported in DU register.	UINT16	BOOT
DU2_1V5_CUR_R_THR	DU2 LVPS 15V current monitor raw threshold as reported in DU register.	UINT16	BOOT
DU2_HV_DR_V_R_THR	DU2 HV drift voltage monitor raw threshold as reported in DU register.	UINT16	BOOT
DU2_HV_TP_V_R_THR	DU2 HV top voltage monitor raw threshold as reported in DU register.	UINT16	BOOT
DU2_HV_BT_V_R_THR	DU2 HV bottom voltage monitor raw threshold as reported in DU register.	UINT16	BOOT
DU2_HV_CUR3_R_THR	DU2 HV current monitor 3 raw threshold as reported in DU register.	UINT16	BOOT
DU3_5V_CUR_R_THR	DU3 LVPS 5V current monitor raw threshold as reported in DU register.	UINT16	BOOT
DU3_3V3_CUR_R_THR	DU3 LVPS 33V current monitor raw threshold as reported in DU register.	UINT16	BOOT
DU3_1V8_CUR_R_THR	DU3 LVPS 18V current monitor raw threshold as reported in DU register.	UINT16	BOOT
DU3_1V5_TMP_R_THR	DU3 LVPS 15V temperature raw threshold as reported in DU register.	UINT16	BOOT

Parameter Id	Description	Type	Upd
DU3_1V8_TMP_R_THR	DU3 LVPS 18V temperature raw threshold as reported in DU register.	UINT16	BOOT
DU3_3V3_TMP_R_THR	DU3 LVPS 33V temperature raw threshold as reported in DU register.	UINT16	BOOT
DU3_HV_TMP1_R_THR	DU3 HV temperature 1 raw threshold as reported in DU register.	UINT16	BOOT
DU3_HV_TMP2_R_THR	DU3 HV temperature 2 raw threshold as reported in DU register.	UINT16	BOOT
DU3_HV_CUR1_R_THR	DU3 HV current monitor 1 raw threshold as reported in DU register.	UINT16	BOOT
DU3_HV_CUR2_R_THR	DU3 HV current monitor 2 raw threshold as reported in DU register.	UINT16	BOOT
DU3_GPD_TMP_R_THR	DU3 GPD temperature raw threshold as reported in DU register.	UINT16	BOOT
DU3_DQ1_TMP_R_THR	DU3 Temperature DAQ 1 raw threshold as reported in DU register.	UINT16	BOOT
DU3_DQ2_TMP_R_THR	DU3 Temperature DAQ 2 raw threshold as reported in DU register.	UINT16	BOOT
DU3_1V5_CUR_R_THR	DU3 LVPS 15V current monitor raw threshold as reported in DU register.	UINT16	BOOT
DU3_HV_DR_V_R_THR	DU3 HV drift voltage monitor raw threshold as reported in DU register.	UINT16	BOOT
DU3_HV_TP_V_R_THR	DU3 HV top voltage monitor raw threshold as reported in DU register.	UINT16	BOOT
DU3_HV_BT_V_R_THR	DU3 HV bottom voltage monitor raw threshold as reported in DU register.	UINT16	BOOT
DU3_HV_CUR3_R_THR	DU3 HV current monitor 3 raw threshold as reported in DU register.	UINT16	BOOT
VBTTM_E_SAA_LOW	Vbottom engineering SAA low voltage value in volts.	INT16	BOOT
VGEM_E_SAA_LOW	Vgem engineering SAA low voltage value in volts.	INT16	BOOT

WARNING: Parameters marked with * must be accordingly reconfigured each time a different DU is connected to the DSU.

In the following sections are reported the default values for these configurable parameters.

B.2 MRAM Thermal Control Default Configuration

DU1:

Paramenter-name	description	Eng [degC]	Raw [dec]
	GPD max	50	2835
DU1_TEC_RAW_T_TGT	TEC target	26	2457
DU1_TEC_RAW_T_TH	TEC thrshold	24	2426
DU1_HOP_RAW_T_TH	HOP threshold	14	2268
DU1_HOP_RAW_T_TGT	HOP target	12	2237
	GPD min	-35	1495
		Eng [A/°C]	**Raw [dec]**
DU1_TEC_SCALED_KP	TEC Kp	0.45	45216
DU1_HOP_SCALED_KP	HOP Kp	0.349	35068
		Eng [A/°C/s]	**Raw [dec]**
DU1_TEC_SCALED_KI	TEC Ki	0.006	603
DU1_HOP_SCALED_KI	HOP Ki	0.0047	472
		Eng [A]	**Raw [dec]**
DU1_TEC_RAW_I_MAX	TEC max current	0.5	846
DU1_HOP_RAW_I_MAX	HOP max current	0.27	481

DU2:

Paramenter-name	Description	Eng [degC]	Raw [dec]
	GPD max	50	2835
DU2_TEC_RAW_T_TGT	TEC target	26	2457
DU2_TEC_RAW_T_TH	TEC thrshold	24	2426
DU2_HOP_RAW_T_TH	HOP threshold	14	2268
DU2_HOP_RAW_T_TGT	HOP target	12	2237
	GPD min	-35	1495
		Eng [A/°C]	**Raw [dec]**
DU2_TEC_SCALED_KP	TEC Kp	0.45	45216
DU2_HOP_SCALED_KP	HOP Kp	0.349	35068
		Eng [A/°C/s]	**Raw [dec]**
DU2_TEC_SCALED_KI	TEC Ki	0.006	603
DU2_HOP_SCALED_KI	HOP Ki	0.0047	472
		Eng [A]	**Raw [dec]**
DU2_TEC_RAW_I_MAX	TEC max current	0.5	846
DU2_HOP_RAW_I_MAX	HOP max current	0.27	481

DU3:

Parameter-name	Description	Eng [degC]	Raw [dec]
	GPD max	50	2835
DU3_TEC_RAW_T_TGT	TEC target	26	2457
DU3_TEC_RAW_T_TH	TEC thrshold	24	2426
DU3_HOP_RAW_T_TH	HOP threshold	14	2268
DU3_HOP_RAW_T_TGT	HOP target	12	2237
	GPD min	-35	1495
		Eng [A/°C]	**Raw [dec]**
DU3_TEC_SCALED_KP	TEC Kp	0.45	45216
DU3_HOP_SCALED_KP	HOP Kp	0.349	35068
		Eng [A/°C/s]	**Raw [dec]**
DU3_TEC_SCALED_KI	TEC Ki	0.006	603
DU3_HOP_SCALED_KI	HOP Ki	0.0047	472
		Eng [A]	**Raw [dec]**
DU3_TEC_RAW_I_MAX	TEC max current	0.5	846
DU3_HOP_RAW_I_MAX	HOP max current	0.27	481

B.3 MRAM High Voltage Boards Default Configuration

Common	Description	Eng	Raw [dec]
VBTTM_E_SAA_LOW	Vbottom engineering SAA	-280	-280
VGEM_E_SAA_LOW	Vgem engineering SAA	-280	-280
DU1		Eng	Raw [dec]
DU1_CTR_VDRFT_S_M	DU1 ctrl Vdrift scaled multiplier	1.04914	104914
DU1_CTR_VDRFT_S_O	DU1 ctrl Vdrift scaled offset	3996.81	399681000
DU1_CTR_VBTTM_S_M	DU1 ctrl Vbottom scaled multiplier	5.38305	538305
DU1_CTR_VBTTM_S_O	DU1 ctrl Vbottom scaled offset	3409.29	340929000
DU1_CTR_VGEM_S_M	DU1 ctrl Vgem scaled multiplier	5.19012	519012
DU1_CTR_VGEM_S_O	DU1 ctrl Vgem scaled offset	3325.4	332540000
DU1_MON_VDRFT_S_M	DU1 mon Vdrift scaled multiplier	-0.93508	-93508
DU1_MON_VDRFT_S_O	DU1 mon Vdrift scaled offset	-15.15447	-1515447
DU1_MON_VBTTM_S_M	DU1 mon Vbottom scaled multiplier	-0.15439	-15439
DU1_MON_VBTTM_S_O	DU1 mon Vbottom scaled offset	-6.40505	-640505
DU1_MON_VTOP_S_M	DU1 mon Vtop scaled multiplier	-0.31493	-31493
DU1_MON_VTOP_S_O	DU1 mon Vtop scaled offset	1.79124	179124
		Eng [V]	Raw [dec]
DU1_VDRIFT_E_MIN	DU1 Vdrift engineering min	-3000	-3000

DU1_VDRIFT_E_MAX	DU1 Vdrift engineering max	-1900	-1900
DU1_VBTTM_E_MIN	DU1 Vbottom engineering min	-430	-430
DU1_VBTTM_E_MAX	DU1 Vbottom engineering max	-300	-300
DU1_VGEM_E_MIN	DU1 Vgem engineering min	-480	-469
DU1_VGEM_E_MAX	DU1 Vgem engineering max	-350	-350
DU1_VDRIFT_E_TOL	DU1 Vdrift engineering tolerance	80	80
DU1_VBTTM_E_TOL	DU1 Vbottom engineering tolerance	20	20
DU1_VGEM_E_TOL	DU1 Vgem engineering tolerance	35	35
DU2		Eng	Raw [dec]
DU2_CTR_VDRFT_S_M	DU2 ctrl Vdrift scaled multiplier	1.04002	104002
DU2_CTR_VDRFT_S_O	DU2 ctrl Vdrift scaled offset	3974.02	397402000
DU2_CTR_VBTTM_S_M	DU2 ctrl Vbottom scaled multiplier	5.34461	534461
DU2_CTR_VBTTM_S_O	DU2 ctrl Vbottom scaled offset	3392.1	339210000
DU2_CTR_VGEM_S_M	DU2 ctrl Vgem scaled multiplier	5.33386	533386
DU2_CTR_VGEM_S_O	DU2 ctrl Vgem scaled offset	3375.87	337587000
DU2_MON_VDRFT_S_M	DU2 mon Vdrift scaled multiplier	-0.93959	-93959
DU2_MON_VDRFT_S_O	DU2 mon Vdrift scaled offset	-9.47678	-947678
DU2_MON_VBTTM_S_M	DU2 mon Vbottom scaled multiplier	-0.1561	-15610
DU2_MON_VBTTM_S_O	DU2 mon Vbottom scaled offset	-2.91422	-291422
DU2_MON_VTOP_S_M	DU2 mon Vtop scaled multiplier	-0.3113	-31130
DU2_MON_VTOP_S_O	DU2 mon Vtop scaled offset	-6.50521	-650521
		Eng [V]	Raw [dec]
DU2_VDRIFT_E_MIN	DU2 Vdrift engineering min	-3000	-3000
DU2_VDRIFT_E_MAX	DU2 Vdrift engineering max	-1900	-1900
DU2_VBTTM_E_MIN	DU2 Vbottom engineering min	-430	-430
DU2_VBTTM_E_MAX	DU2 Vbottom engineering max	-300	-300
DU2_VGEM_E_MIN	DU2 Vgem engineering min	-466	-454
DU2_VGEM_E_MAX	DU2 Vgem engineering max	-350	-350
DU2_VDRIFT_E_TOL	DU2 Vdrift engineering tolerance	80	80
DU2_VBTTM_E_TOL	DU2 Vbottom engineering tolerance	20	20
DU2_VGEM_E_TOL	DU2 Vgem engineering tolerance	35	35
DU3		Eng	Raw [dec]
DU3_CTR_VDRFT_S_M	DU3 ctrl Vdrift scaled multiplier	1.03919	103919
DU3_CTR_VDRFT_S_O	DU3 ctrl Vdrift scaled offset	3970.72	397072000
DU3_CTR_VBTTM_S_M	DU3 ctrl Vbottom scaled multiplier	5.56732	556732
DU3_CTR_VBTTM_S_O	DU3 ctrl Vbottom scaled offset	3480.6	348060000
DU3_CTR_VGEM_S_M	DU3 ctrl Vgem scaled multiplier	5.35369	535369
DU3_CTR_VGEM_S_O	DU3 ctrl Vgem scaled offset	3386.75	338675000
DU3_MON_VDRFT_S_M	DU3 mon Vdrift scaled multiplier	-0.94551	-94551
DU3_MON_VDRFT_S_O	DU3 mon Vdrift scaled offset	7.03215	703215
DU3_MON_VBTTM_S_M	DU3 mon Vbottom scaled multiplier	-0.14948	-14948
DU3_MON_VBTTM_S_O	DU3 mon Vbottom scaled offset	-18.86118	-1886118

DU3_MON_VTOP_S_M	DU3 mon Vtop scaled multiplier	-0.30496	-30496
DU3_MON_VTOP_S_O	DU3 mon Vtop scaled offset	-22.59412	-2259412
		Eng [V]	Raw [dec]
DU3_VDRIFT_E_MIN	DU3 Vdrift engineering min	-3000	-3000
DU3_VDRIFT_E_MAX	DU3 Vdrift engineering max	-1900	-1900
DU3_VBTTM_E_MIN	DU3 Vbottom engineering min	-430	-430
DU3_VBTTM_E_MAX	DU3 Vbottom engineering max	-300	-300
DU3_VGEM_E_MIN	DU3 Vgem engineering min	-465	-454
DU3_VGEM_E_MAX	DU3 Vgem engineering max	-350	-350
DU3_VDRIFT_E_TOL	DU3 Vdrift engineering tolerance	80	80

B.4 MRAM DSU Default Configuration

Application Software		
		Raw [dec]
MISSION_EPOCH	Mission epoch in seconds	1861920000
SCRUB_CHUNK_SIZE	Scrub memory chunk size in bytes	32
SDI_RETRY_NUM	SDI retry number	2
SDI_BUFF_LIMIT	SDI buffer limit	8192
DU1_CCI_SPEED_DIV	DU1 CCI speed divider	3
DU2_CCI_SPEED_DIV	DU2 CCI speed divider	3
DU3_CCI_SPEED_DIV	DU3 CCI speed divider	3

B.5 BEE Configuration Setup Default

Below are reported the details of BEE configuration setup stored in MRAM. we report only the presets of DU1 because are identically for the three DUs, Functional presets follow the next table:

SLOT NUMER	Acquisition mode
0-20	Nominal Acquisition
21-25	Pixel Noisy check
26	Alarm In line Trigger (TEST)
27	Charge Injection
28-31	Pixel Scan

DU ID	DU1	DU1	DU1
SLOT NUMBER	0	1	2
PEDESTAL MEM OFFSET	4096	4096	4096
HK METERS INT	ENABLE	ENABLE	ENABLE
EXT 1MHZ ENABLE	ENABLE	ENABLE	ENABLE
FORCE SDI ENABLE	DISABLE	DISABLE	DISABLE
SDI RTX NUM	2	2	2
DAC V TH CTRL	250	250	250
DAC V TEST CTRL	200	200	200
SDI START ADDR	8192	8192	8192
SDI CLK DIVIDER	4	4	4
SDI RTX WAIT	250	250	250
WIN D UPPER LIMIT	3952	3952	3952
WIN D LOW LIMIT	120	120	120
ADC XPOL CLK DIV	8	8	8
CLK PER CYCLES	8	8	8
CLK SHIFT CYCLES	0	0	0
ADC XPOL CLK DF CSN	ON	ON	ON
ADC XPOL G0	OFF	OFF	OFF
ADC XPOL G1	OFF	OFF	OFF
ADC TYPE	ST	ST	ST
PHA ULIM THR	1050	1050	1050
PHA LLIM THR	1051	1051	1051
DIAG EVENTS PERIOD	100	100	100
XPOL DISCH WIDTH	25000	25000	25000
XPOL MH CYCLES	320	320	320
XPOL ZS THR	34	32	30
XPOL PED NUMBER	1	1	1
XPOL INJ WIDTH	0	0	0
XPOL INJ PERIOD	0	0	0
SCAN STEPS X	0	0	0
SCAN STEPS Y	0	0	0
SCAN DELTA X	0	0	0
SCAN DELTA Y	0	0	0
PULSES PER PIXEL	0	0	0
XPOL X ADDR	0	0	0
XPOL Y ADDR	0	0	0
PIXEL SCAN ENABLE	DISABLE	DISABLE	DISABLE
XPOL CONFIG REG	0x0E	0x0E	0x0E
XPOL SI MODE	CORE_LOGIC	CORE_LOGIC	CORE_LOGIC
MUX SELECT	CL_XPOL_WRITE	CL_XPOL_WRITE	CL_XPOL_WRITE
HK1 ENABLE	ENABLE	ENABLE	ENABLE
HK2 ENABLE	ENABLE	ENABLE	ENABLE
HK3 ENABLE	ENABLE	ENABLE	ENABLE
HK1 CHANNEL MASK	0xff	0xff	0xff
HK3 CHANNEL MASK	0xff	0xff	0xff
HK3 CHANNEL MASK	0xff	0xff	0xff

0xff	0xff	0xff	0xff	0xff
0xff	0xff	0xff	0xff	0xff
0xff	0xff	0xff	0xff	0xff
ENABLE	ENABLE	ENABLE	ENABLE	ENABLE
ENABLE	ENABLE	ENABLE	ENABLE	ENABLE
CL_XPOL_WRITE	CL_XPOL_WRITE	CL_XPOL_WRITE	CL_XPOL_WRITE	CL_XPOL_WRITE
CORE_LOGIC	CORE_LOGIC	CORE_LOGIC	CORE_LOGIC	CORE_LOGIC
0x0E	0x0E	0x0E	0x0E	0x0E
DISABLE	DISABLE	DISABLE	DISABLE	DISABLE
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
1	1	1	1	1
28	26	25	24	24
320	320	320	320	320
25000	25000	25000	25000	25000
100	100	100	100	100
1051	1051	1051	1051	1051
1050	1050	1050	1050	1050
ST	ST	ST	ST	ST
OFF	OFF	OFF	OFF	OFF
OFF	OFF	OFF	OFF	OFF
ON	ON	ON	ON	ON
0	0	0	0	0
8	8	8	8	8
8	8	8	8	8
120	120	120	120	120
3952	3952	3952	3952	3952
250	250	250	250	250
4	4	4	4	4
8192	8192	8192	8192	8192
200	200	200	200	200
250	250	250	250	250
2	2	2	2	2
DISABLE	DISABLE	DISABLE	DISABLE	DISABLE
ENABLE	ENABLE	ENABLE	ENABLE	ENABLE
ENABLE	ENABLE	ENABLE	ENABLE	ENABLE
4096	4096	4096	4096	4096
3	4	5	6	DU1
DU1	DU1	DU1	DU1	

0xff	0xff	0xff	0xff	0xff
0xff	0xff	0xff	0xff	0xff
0xff	0xff	0xff	0xff	0xff
ENABLE	ENABLE	ENABLE	ENABLE	ENABLE
ENABLE	ENABLE	ENABLE	ENABLE	ENABLE
CL_XPOL_WRITE	CL_XPOL_WRITE	CL_XPOL_WRITE	CL_XPOL_WRITE	CL_XPOL_WRITE
CORE_LOGIC	CORE_LOGIC	CORE_LOGIC	CORE_LOGIC	CORE_LOGIC
0x0E	0x0E	0x0E	0x0E	0x0E
DISABLE	DISABLE	DISABLE	DISABLE	DISABLE
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
1	1	1	1	1
23	22	21	20	19
320	320	320	320	320
25000	25000	25000	25000	25000
100	100	100	100	100
1051	1051	1051	1051	1051
1050	1050	1050	1050	1050
ST	ST	ST	ST	ST
OFF	OFF	OFF	OFF	OFF
OFF	OFF	OFF	OFF	OFF
ON	ON	ON	ON	ON
0	0	0	0	0
8	8	8	8	8
8	8	8	8	8
120	120	120	120	120
3952	3952	3952	3952	3952
250	250	250	250	250
4	4	4	4	4
8192	8192	8192	8192	8192
200	200	200	200	200
250	250	250	250	250
2	2	2	2	2
DISABLE	DISABLE	DISABLE	DISABLE	DISABLE
ENABLE	ENABLE	ENABLE	ENABLE	ENABLE
ENABLE	ENABLE	ENABLE	ENABLE	ENABLE
4096	4096	4096	4096	4096
7	8	9	10	11
DU1	DU1	DU1	DU1	DU1

0xff	0xff	0xff	0xff	0xff
0xff	0xff	0xff	0xff	0xff
0xff	0xff	0xff	0xff	0xff
ENABLE	ENABLE	ENABLE	ENABLE	ENABLE
ENABLE	ENABLE	ENABLE	ENABLE	ENABLE
CL_XPOL_WRITE	CL_XPOL_WRITE	CL_XPOL_WRITE	CL_XPOL_WRITE	CL_XPOL_WRITE
CORE_LOGIC	CORE_LOGIC	CORE_LOGIC	CORE_LOGIC	CORE_LOGIC
0x0E	0x0E	0x0E	0x0E	0x0E
DISABLE	DISABLE	DISABLE	DISABLE	DISABLE
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
1	1	1	1	1
19	18	17	16	15
320	320	320	320	320
25000	25000	25000	25000	25000
100	100	100	100	100
1051	1051	1051	1051	1051
1050	1050	1050	1050	1050
ST	ST	ST	ST	ST
OFF	OFF	OFF	OFF	OFF
OFF	OFF	OFF	OFF	OFF
ON	ON	ON	ON	ON
0	0	0	0	0
8	8	8	8	8
8	8	8	8	8
120	120	120	120	120
3952	3952	3952	3952	3952
250	250	250	250	250
4	4	4	4	4
8192	8192	8192	8192	8192
200	200	200	200	200
250	250	250	250	250
2	2	2	2	2
DISABLE	DISABLE	DISABLE	DISABLE	DISABLE
ENABLE	ENABLE	ENABLE	ENABLE	ENABLE
ENABLE	ENABLE	ENABLE	ENABLE	ENABLE
4096	4096	4096	4096	4096
11	12	13	14	15
DU1	DU1	DU1	DU1	DU1

0xff	0xff	0xff	0xff	0xff
0xff	0xff	0xff	0xff	0xff
0xff	0xff	0xff	0xff	0xff
ENABLE	ENABLE	ENABLE	ENABLE	ENABLE
ENABLE	ENABLE	ENABLE	ENABLE	ENABLE
CL_XPOL_WRITE	CL_XPOL_WRITE	CL_XPOL_WRITE	CL_XPOL_WRITE	CL_XPOL_WRITE
CORE_LOGIC	CORE_LOGIC	CORE_LOGIC	CORE_LOGIC	CORE_LOGIC
0x0E	0x0E	0x0E	0x0E	0x0E
DISABLE	DISABLE	DISABLE	DISABLE	DISABLE
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
1	1	1	1	1
15	14	12	10	8
320	320	320	320	320
25000	25000	25000	25000	25000
100	100	100	100	100
1051	1051	1051	1051	1051
1050	1050	1050	1050	1050
ST	ST	ST	ST	ST
OFF	OFF	OFF	OFF	OFF
OFF	OFF	OFF	OFF	OFF
ON	ON	ON	ON	ON
0	0	0	0	0
8	8	8	8	8
8	8	8	8	8
120	120	120	120	120
3952	3952	3952	3952	3952
250	250	250	250	250
4	4	4	4	4
8192	8192	8192	8192	8192
200	200	200	200	200
250	250	250	250	250
2	2	2	2	2
DISABLE	DISABLE	DISABLE	DISABLE	DISABLE
ENABLE	ENABLE	ENABLE	ENABLE	ENABLE
ENABLE	ENABLE	ENABLE	ENABLE	ENABLE
4096	4096	4096	4096	4096
15	16	17	18	19
DU1	DU1	DU1	DU1	DU1

0xff	0xff	0xff	0xff	0xff
0xff	0xff	0xff	0xff	0xff
0xff	0xff	0xff	0xff	0xff
ENABLE	ENABLE	ENABLE	ENABLE	ENABLE
ENABLE	ENABLE	ENABLE	ENABLE	ENABLE
ENABLE	ENABLE	ENABLE	ENABLE	ENABLE
CL_XPOL_WRITE	CL_XPOL_WRITE	CL_XPOL_WRITE	CL_XPOL_WRITE	CL_XPOL_WRITE
CORE_LOGIC	CORE_LOGIC	CORE_LOGIC	CORE_LOGIC	CORE_LOGIC
0x0E	0x0E	0x0E	0x0E	0x0E
DISABLE	DISABLE	DISABLE	DISABLE	DISABLE
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
1	1	1	1	1
8	0	18	18	18
320	320	320	320	320
25000	25000	25000	25000	25000
100	100	100	100	100
1051	1051	1051	1051	1051
1050	1050	1050	1050	1050
ST	ST	ST	ST	ST
OFF	OFF	OFF	OFF	OFF
OFF	OFF	OFF	OFF	OFF
ON	ON	ON	ON	ON
0	0	0	0	0
8	8	8	8	8
8	8	8	8	8
120	120	120	120	120
3952	3952	3952	3952	3952
250	250	250	250	250
4	4	4	4	4
8192	8192	8192	8192	8192
200	200	200	200	200
250	250	500	450	450
2	2	2	2	2
DISABLE	DISABLE	DISABLE	DISABLE	DISABLE
ENABLE	ENABLE	ENABLE	ENABLE	ENABLE
ENABLE	ENABLE	ENABLE	ENABLE	ENABLE
4096	4096	4096	4096	4096
19	20	21	22	23
DU1	DU1	DU1	DU1	DU1

0xff	0xff	0xff	0xff
0xff	0xff	0xff	0xff
0xff	0xff	0xff	0xff
ENABLE	ENABLE	ENABLE	ENABLE
ENABLE	ENABLE	ENABLE	ENABLE
ENABLE	ENABLE	ENABLE	ENABLE
CL_XPOL_WRITE	CL_XPOL_WRITE	CL_XPOL_WRITE	ALARM_IN
CORE_LOGIC	CORE_LOGIC	CORE_LOGIC	CORE_LOGIC
0x0E	0x0E	0x0E	0x0E
DISABLE	DISABLE	DISABLE	DISABLE
0	0	0	150
0	0	0	130
0	0	0	0
0	0	0	0
0	0	0	0
0	0	0	0
0	0	0	0
0	0	0	0
0	0	0	0
1	1	1	1
18	18	18	18
320	320	320	320
25000	25000	25000	25000
100	100	100	0
1051	1051	1051	1051
1050	1050	1050	1050
ST	ST	ST	ST
OFF	OFF	OFF	OFF
OFF	OFF	OFF	OFF
ON	ON	ON	ON
0	0	0	0
8	8	8	8
8	8	8	8
120	120	120	120
3952	3952	3952	3952
250	250	250	250
4	4	4	4
8192	8192	8192	8192
200	200	200	200
400	350	300	250
2	2	2	2
DISABLE	DISABLE	DISABLE	DISABLE
ENABLE	ENABLE	ENABLE	ENABLE
ENABLE	ENABLE	ENABLE	ENABLE
4096	4096	4096	4096
23	24	25	26
DU1	DU1	DU1	DU1

0xff	0xff	0xff	0xff	0xff
0xff	0xff	0xff	0xff	0xff
0xff	0xff	0xff	0xff	0xff
ENABLE	ENABLE	ENABLE	ENABLE	ENABLE
ENABLE	ENABLE	ENABLE	ENABLE	ENABLE
CL_XPOL_WRITE	CL_XPOL_WRITE	CL_XPOL_WRITE	CL_XPOL_WRITE	CL_XPOL_WRITE
CORE_LOGIC	CORE_LOGIC	CORE_LOGIC	CORE_LOGIC	CORE_LOGIC
0x0E	0x0E	0x0E	0x0E	0x0E
DISABLE	ENABLE	ENABLE	ENABLE	ENABLE
150	10	10	10	10
130	10	10	10	10
0	20	20	20	20
0	2	4	8	8
0	2	4	8	8
0	166	83	42	42
0	142	71	36	36
600	300	300	300	300
100	0	0	0	0
1	1	1	1	1
0	0	0	0	0
320	320	320	320	320
25000	25000	25000	25000	25000
0	0	0	0	0
1051	1051	1051	1051	1051
1050	1050	1050	1050	1050
ST	ST	ST	ST	ST
OFF	OFF	OFF	OFF	OFF
OFF	OFF	OFF	OFF	OFF
ON	ON	ON	ON	ON
0	0	0	0	0
8	8	8	8	8
8	8	8	8	8
120	120	120	120	120
3952	3952	3952	3952	3952
250	250	250	250	250
4	4	4	4	4
8192	8192	8192	8192	8192
200	200	200	200	200
250	250	250	250	250
2	2	2	2	2
DISABLE	DISABLE	DISABLE	DISABLE	DISABLE
ENABLE	ENABLE	ENABLE	ENABLE	ENABLE
ENABLE	ENABLE	ENABLE	ENABLE	ENABLE
4096	4096	4096	4096	4096
27	28	29	30	31
DU1	DU1	DU1	DU1	DU1

DU1	31	4096	ENABLE	ENABLE	DISABLE	2	250	200	8192	4	250	3952	120	8	8	0	ON	OFF	OFF	ST	1050	1051	0	25000	320	0	1	0	300	18	21	16	16	20	10	10	ENABLE	0x0E	CORE_LOGIC	CL_XPOL_WRITE	ENABLE	ENABLE	ENABLE	0xff	0xff	0xff

B.6 BEE Alarm Configuration Default

In the following table reported the BEE alarm configuration loaded in DSU MRAM to configure DU ALARMS thresholds. During the Instrument E2E test the has been used the slot 5.

MARGIN	DU ID	SLOT NUMBER	ALARM RESET	ALARM MASK	VOLT DRIFT THR	CURR DRIFT THR	VOLT BOTTOM THR	CURR BOTTOM THR	VOLT TOP THR	CURR GEM THR	CURR 5V THR	CURR 3V3 THR	CURR 1V8 THR	CURR 1V5 THR
10%	DU1	0	ENABLE	0	3192	0xFFF	2742	0xFFF	2968	0xFFF	0xFFF	3752	1424	169
20%	DU1	1	ENABLE	0	3192	0xFFF	2742	0xFFF	2968	0xFFF	0xFFF	4093	1554	184
30%	DU1	2	ENABLE	0	3192	0xFFF	2742	0xFFF	2968	0xFFF	0xFFF	4434	1683	200
40%	DU1	3	ENABLE	0	3192	0xFFF	2742	0xFFF	2968	0xFFF	0xFFF	4775	1813	215
50%	DU1	4	ENABLE	0	3192	0xFFF	2742	0xFFF	2968	0xFFF	0xFFF	5116	1942	231
60%	DU1	5	ENABLE	0	3192	0xFFF	2742	0xFFF	2968	0xFFF	0xFFF	5457	2072	246

10%	DU2	0	ENABLE	0	3192	0xFFF	2742	0xFFF	2968	0xFFF	0xFFF	3752	1424	169
20%	DU2	1	ENABLE	0	3192	0xFFF	2742	0xFFF	2968	0xFFF	0xFFF	4093	1554	184
30%	DU2	2	ENABLE	0	3192	0xFFF	2742	0xFFF	2968	0xFFF	0xFFF	4434	1683	200
40%	DU2	3	ENABLE	0	3192	0xFFF	2742	0xFFF	2968	0xFFF	0xFFF	4775	1813	215
50%	DU2	4	ENABLE	0	3192	0xFFF	2742	0xFFF	2968	0xFFF	0xFFF	5116	1942	231
60%	DU2	5	ENABLE	0	3192	0xFFF	2742	0xFFF	2968	0xFFF	0xFFF	5457	2072	246
10%	DU3	0	ENABLE	0	3192	0xFFF	2742	0xFFF	2968	0xFFF	0xFFF	3752	1424	169
20%	DU3	1	ENABLE	0	3192	0xFFF	2742	0xFFF	2968	0xFFF	0xFFF	4093	1554	184
30%	DU3	2	ENABLE	0	3192	0xFFF	2742	0xFFF	2968	0xFFF	0xFFF	4434	1683	200
40%	DU3	3	ENABLE	0	3192	0xFFF	2742	0xFFF	2968	0xFFF	0xFFF	4775	1813	215
50%	DU3	4	ENABLE	0	3192	0xFFF	2742	0xFFF	2968	0xFFF	0xFFF	5116	1942	231
60%	DU3	5	ENABLE	0	3192	0xFFF	2742	0xFFF	2968	0xFFF	0xFFF	5457	2072	246

B.7 BEE Pixel Mask Configuration Default

In the following table are reported the presets stored to be used for the DUs Pixel Mask Configuration:

DU	SLOT NUMER
1	2
2	3
3	4

The list of pixel noisy is reported in the following table.

SPARE		DU1		DU2		DU3	
DU FM1		DU FM2		DU FM3		DU FM4	
Number Of Pixels = 29		Number Of Pixels = 11		Number Of Pixels = 22		Number Of Pixels = 17	
X	Y	X	Y	X	Y	X	Y
238	213	39	226	181	121	246	286
212	25	69	24	102	186	104	93
163	47	105	59	172	244	218	154
23	41	133	251	138	86	273	255

285	11	162	31	65	21	153	241
146	88	205	277	128	266	140	295
76	131	242	189	16	26	30	143
65	265	276	66	11	90	133	17
254	246	135	251	184	259	125	8
211	62	264	273	58	88	125	9
278	72	254	261	121	348	249	146
167	305			2	306	101	281
192	38			262	326	47	182
3	159			107	324	50	308
223	181			163	272	234	194
271	302			66	336	40	301
108	90			55	348	46	226
68	261			202	271		
145	2			136	76		
241	147			15	76		
259	142			183	145		
43	170			29	275		
266	54						
207	203						

222	208						
124	346						
36	180						
37	180						
228	295						

Below are reported the commands used to store the DUs Pixel Mask Configuration (DU3 SLOT 4 updated during TVAC Test, August 2021):

DU1 – SLOT2

tcsend UUU11155 {UUU0001X DU1} {UUU0140N 2} {UUU0170S ENABLE} {UUU0171N 11} {UUU0172X 264} {UUU0173X 273} {UUU0174X 242} {UUU0175X 189} {UUU0176X 39} {UUU0177X 226} {UUU0178X 135} {UUU0179X 251} {UUU0180X 162} {UUU0181X 31} {UUU0182X 105} {UUU0183X 59} {UUU0184X 254} {UUU0185X 261} {UUU0186X 276} {UUU0187X 66} {UUU0188X 205} {UUU0189X 277} {UUU0190X 133} {UUU0191X 251} {UUU0192X 69} {UUU0193X 24} {UUU0194X 0} {UUU0195X 0} {UUU0196X 0} {UUU0197X 0} {UUU0198X 0 } {UUU0199X 0} {UUU0200X 0} {UUU0201X 0} {UUU0202X 0 } {UUU0203X 0} {UUU0204X 0 } {UUU0205X 0} {UUU0206X 0} {UUU0207X 0} {UUU0208X 0} {UUU0209X 0} {UUU0210X 0} {UUU0211X 0} {UUU0212X 0} {UUU0213X 0} {UUU0214X 0} {UUU0215X 0} {UUU0216X 0} {UUU0217X 0} {UUU0218X 0} {UUU0219X 0} {UUU0220X 0} {UUU0221X 0} {UUU0222X 0} {UUU0223X 0} {UUU0224X 0} {UUU0225X 0} {UUU0226X 0} {UUU0227X 0} {UUU0228X 0} {UUU0229X 0} {UUU0230X 0} {UUU0231X 0} {UUU0232X 0} {UUU0233X 0} {UUU0234X 0} {UUU0235X 0}

DU2 – SLOT3

tcsend UUU11155 {UUU0001X DU2} {UUU0140N 3} {UUU0170S ENABLE} {UUU0171N 22} {UUU0172X 136} {UUU0173X 76} {UUU0174X 55} {UUU0175X 348} {UUU0176X 172} {UUU0177X 244} {UUU0178X 2} {UUU0179X 306} {UUU0180X 102} {UUU0181X 186} {UUU0182X 202} {UUU0183X 271} {UUU0184X 138} {UUU0185X 86} {UUU0186X 121} {UUU0187X 348} {UUU0188X 58} {UUU0189X 88} {UUU0190X 107} {UUU0191X 324} {UUU0192X 163} {UUU0193X 272} {UUU0194X 262} {UUU0195X 326} {UUU0196X 181} {UUU0197X 121} {UUU0198X 11} {UUU0199X 90} {UUU0200X 29} {UUU0201X 275} {UUU0202X 65} {UUU0203X 21} {UUU0204X 128} {UUU0205X 266} {UUU0206X 183} {UUU0207X 145} {UUU0208X 66} {UUU0209X 336} {UUU0210X 184} {UUU0211X 259} {UUU0212X 15} {UUU0213X 76} {UUU0214X 16} {UUU0215X 26} {UUU0216X 0} {UUU0217X 0} {UUU0218X 0} {UUU0219X 0} {UUU0220X 0} {UUU0221X 0} {UUU0222X 0} {UUU0223X 0} {UUU0224X 0} {UUU0225X 0} {UUU0226X 0} {UUU0227X 0} {UUU0228X 0} {UUU0229X 0} {UUU0230X 0} {UUU0231X 0} {UUU0232X 0} {UUU0233X 0} {UUU0234X 0} {UUU0235X 0}

DU3 – SLOT4

tcsend UUU11155 {UUU0001X DU3} {UUU0140N 4} {UUU0170S ENABLE} {UUU0171N 17} {UUU0172X 246} {UUU0173X 286} {UUU0174X 104} {UUU0175X 93} {UUU0176X 218} {UUU0177X 154} {UUU0178X 273} {UUU0179X 255} {UUU0180X 153} {UUU0181X 241} {UUU0182X 140} {UUU0183X 295} {UUU0184X 30 } {UUU0185X 143} {UUU0186X 133} {UUU0187X 17} {UUU0188X 125} {UUU0189X 8} {UUU0190X 125} {UUU0191X 9} {UUU0192X 249} {UUU0193X 146} {UUU0194X 101} {UUU0195X 281} {UUU0196X 47} {UUU0197X 182} {UUU0198X 50 } {UUU0199X 308} {UUU0200X 234} {UUU0201X 194} {UUU0202X 40 } {UUU0203X 301} {UUU0204X 46 } {UUU0205X 226} {UUU0206X 0} {UUU0207X 0} {UUU0208X 0} {UUU0209X 0} {UUU0210X 0} {UUU0211X 0} {UUU0212X 0} {UUU0213X 0} {UUU0214X 0} {UUU0215X 0} {UUU0216X 0} {UUU0217X 0} {UUU0218X 0} {UUU0219X 0} {UUU0220X 0} {UUU0221X 0} {UUU0222X 0} {UUU0223X 0} {UUU0224X 0} {UUU0225X 0} {UUU0226X 0} {UUU0227X 0} {UUU0228X 0} {UUU0229X 0} {UUU0230X 0} {UUU0231X 0} {UUU0232X 0} {UUU0233X 0} {UUU0234X 0} {UUU0235X 0}

B.8 FDIR Rules Configuration Default

In the following table are reported the FDIR configured and activated at the power up of the DSU.

Slot ID	Parameter Under Control	Enabled	Inhibit (s)	Repeat (s)	Check	Min	Max	Action	Condition 1	Value	Condition 2	Value
0	D#1_TEMP_LVPS_1V5	ENABLED	100	10	OUT_RANGE	0°C	55°C	DU1_POWER_OFF	DU1 5V STATUS	ON		
1	D#1_TEMP_LVPS_1V8	ENABLED	100	10	OUT_RANGE	0°C	55°C	DU1_POWER_OFF	DU1 5V STATUS	ON		
2	D#1_TEMP_LVPS_3V3	ENABLED	100	10	OUT_RANGE	0°C	55°C	DU1_POWER_OFF	DU1 5V STATUS	ON		
3	D#1_TEMP_HV_1	ENABLED	100	10	OUT_RANGE	-20°C	55°C	DU1_POWER_OFF	DU1 5V STATUS	ON		
4	D#1_TEMP_HV_2	ENABLED	100	10	OUT_RANGE	-20°C	55°C	DU1_POWER_OFF	DU1 5V STATUS	ON		
5	D#1_TEMP_GPD	ENABLED	100	10	OUT_RANGE	0°C	40°C	DU1_POWER_OFF	DU1 5V STATUS	ON		
6	D#1_TEMP_DAQ_1	ENABLED	100	10	OUT_RANGE	0°C	72°C	DU1_POWER_OFF	DU1 5V STATUS	ON		
7	D#1_TEMP_DAQ_2	ENABLED	100	10	OUT_RANGE	0°C	72°C	DU1_POWER_OFF	DU1 5V STATUS	ON		
8	D#2_TEMP_LVPS_1V5	ENABLED	100	10	OUT_RANGE	0°C	55°C	DU2_POWER_OFF	DU2 5V STATUS	ON		
9	D#2_TEMP_LVPS_1V8	ENABLED	100	10	OUT_RANGE	0°C	55°C	DU2_POWER_OFF	DU2 5V STATUS	ON		
10	D#2_TEMP_LVPS_3V3	ENABLED	100	10	OUT_RANGE	0°C	55°C	DU2_POWER_OFF	DU2 5V STATUS	ON		
11	D#2_TEMP_HV_1	ENABLED	100	10	OUT_RANGE	-20°C	55°C	DU2_POWER_OFF	DU2 5V STATUS	ON		
12	D#2_TEMP_HV_2	ENABLED	100	10	OUT_RANGE	-20°C	55°C	DU2_POWER_OFF	DU2 5V STATUS	ON		
13	D#2_TEMP_GPD	ENABLED	100	10	OUT_RANGE	0°C	40°C	DU2_POWER_OFF	DU2 5V STATUS	ON		
14	D#2_TEMP_DAQ_1	ENABLED	100	10	OUT_RANGE	0°C	72°C	DU2_POWER_OFF	DU2 5V STATUS	ON		
15	D#2_TEMP_DAQ_2	ENABLED	100	10	OUT_RANGE	0°C	72°C	DU2_POWER_OFF	DU2 5V STATUS	ON		

16	D#3_TEMP_LVPS_1V5	ENABLED	100	10	OUT_RANGE	0°C	55°C	DU3_POWER_OFF	DU3 5V STATUS	ON		
17	D#3_TEMP_LVPS_1V8	ENABLED	100	10	OUT_RANGE	0°C	55°C	DU3_POWER_OFF	DU3 5V STATUS	ON		
18	D#3_TEMP_LVPS_3V3	ENABLED	100	10	OUT_RANGE	0°C	55°C	DU3_POWER_OFF	DU3 5V STATUS	ON		
19	D#3_TEMP_HV_1	ENABLED	100	10	OUT_RANGE	-20°C	55°C	DU3_POWER_OFF	DU3 5V STATUS	ON		
20	D#3_TEMP_HV_2	ENABLED	100	10	OUT_RANGE	-20°C	55°C	DU3_POWER_OFF	DU3 5V STATUS	ON		
21	D#3_TEMP_GPD	ENABLED	100	10	OUT_RANGE	0°C	40°C	DU3_POWER_OFF	DU3 5V STATUS	ON		
22	D#3_TEMP_DAQ_1	ENABLED	100	10	OUT_RANGE	0°C	72°C	DU3_POWER_OFF	DU3 5V STATUS	ON		
23	D#3_TEMP_DAQ_2	ENABLED	100	10	OUT_RANGE	0°C	72°C	DU3_POWER_OFF	DU3 5V STATUS	ON		
24	D#1_VREF_XPOL	ENABLED	100	10	OUT_RANGE	650mV	900mV	NO_ACTION	DU1 5V STATUS	ON		
25	D#2_VREF_XPOL	ENABLED	100	10	OUT_RANGE	650mV	900mV	NO_ACTION	DU2 5V STATUS	ON		
26	D#3_VREF_XPOL	ENABLED	100	10	OUT_RANGE	650mV	900mV	NO_ACTION	DU3 5V STATUS	ON		
30	DU1 EVT COUNT	ENABLED	100	20	LESS_THAN	1	1	NO_ACTION	DU1 5V STATUS	ON	CURRENT OP MODE	OBSERVATION
31	DU2 EVT COUNT	ENABLED	100	20	LESS_THAN	1	1	NO_ACTION	DU2 5V STATUS	ON	CURRENT OP MODE	OBSERVATION
32	DU3 EVT COUNT	ENABLED	100	20	LESS_THAN	1	1	NO_ACTION	DU3 5V STATUS	ON	CURRENT OP MODE	OBSERVATION
33	GPD1 TEMPERATURE	ENABLED	100	10	OUT_RANGE	0°C	40°C	DU1_POWER_OFF	DU1 5V STATUS	ON		
34	GPD2 TEMPERATURE	ENABLED	100	10	OUT_RANGE	0°C	40°C	DU2_POWER_OFF	DU2 5V STATUS	ON		
35	GPD3 TEMPERATURE	ENABLED	100	10	OUT_RANGE	0°C	40°C	DU3_POWER_OFF	DU3 5V STATUS	ON		

ANNEX C – FDIR PARAMETERS

C.1 FDIR Configurable Parameters

Parameter- name	Description	Mnemonic	Type
SLOW_RATE_SRAM_TEST_AREA	SRAM test area.	DDD9990X	UINT32
DCT_UNIT1_HK_DU1_DATA_VALIDITY	DU1 data validity.	UUU1113S	UINT8
DCT_UNIT1_HK_DU1_RUN_ID	DU1 run id.	UUU0007N	UINT32
DCT_UNIT1_HK_DU1_OBT_SECONDS	DU1 obt seconds.	UUU1115H	UINT32
DCT_UNIT1_HK_DU1_OBT_MICROSECONDS	DU1 obt microseconds.	UUU1116H	UINT32
DCT_UNIT1_HK_DU1_OBT_ERROR	DU1 obt error BEE register.	UUU1117H	INT32
DCT_UNIT1_HK_DU1_CONFIG_REGA	DU1 config rega BEE register.	UUU1000S	UINT16
DCT_UNIT1_HK_DU1_CONFIG_REGB	DU1 config regb BEE register.	UUU1001S	UINT16
DCT_UNIT1_HK_DU1_HK_1_CONFIG	DU1 hk 1 config BEE register.	UUU1002S	UINT16
DCT_UNIT1_HK_DU1_HK_2_CONFIG	DU1 hk 2 config BEE register.	UUU1003S	UINT16
DCT_UNIT1_HK_DU1_HK_3_CONFIG	DU1 hk 3 config BEE register.	UUU1004S	UINT16
DCT_UNIT1_HK_DU1_SPARE_LVPS_1	DU1 spare lvps 1 BEE register.	UUU1011U	UINT16
DCT_UNIT1_HK_DU1_SPARE_DAQ_1	DU1 spare daq 1 BEE register.	UUU1017U	UINT16
DCT_UNIT1_HK_DU1_CURRENT_PWR_IN	DU1 current pwr in BEE register.	UUU1021I	UINT16
DCT_UNIT1_HK_DU1_SPARE_LPVS_2	DU1 spare lpvs 2 BEE register.	UUU1022U	UINT16
DCT_UNIT1_HK_DU1_SPARE_DAQ_2	DU1 spare daq 2 BEE register.	UUU1028U	UINT16
DCT_UNIT1_HK_DU1_READ_TEST	DU1 read test BEE register.	UUU1029S	UINT16
DCT_UNIT1_HK_DU1_DAC_VTH_CTRL	DU1 dac vth ctrl BEE register.	UUU1030S	UINT16
DCT_UNIT1_HK_DU1_DAC_VTEST_CTRL	DU1 dac vtest ctrl BEE register.	UUU1031S	UINT16

DCT_UNIT1_HK_DU1_ADC_XPOL_TI_DATA_IN	DU1 adc xpol ti data in BEE register.	UUU1032S	UINT16
DCT_UNIT1_HK_DU1_ADC_XPOL_TI_DATA_OUT	DU1 adc xpol ti data out BEE register.	UUU1033S	UINT16
DCT_UNIT1_HK_DU1_ADC_XPOL_TI_CTRL	DU1 adc xpol ti ctrl BEE register.	UUU1034S	UINT16
DCT_UNIT1_HK_DU1_ADC_XPOL_CLK_DIVIDER	DU1 adc xpol clk divider BEE register.	UUU1035S	UINT16
DCT_UNIT1_HK_DU1_XPOL_RO_CTRL	DU1 xpol ro ctrl BEE register.	UUU1036S	UINT16
DCT_UNIT1_HK_DU1_XPOL_RO_DISCH_WIDTH	DU1 xpol ro disch width BEE register.	UUU1038S	UINT16
DCT_UNIT1_HK_DU1_XPOL_RO_MH_CYCLES	DU1 xpol ro mh cycles BEE register.	UUU1039S	UINT16
DCT_UNIT1_HK_DU1_ALARM_OUT_CONFIG	DU1 alarm out config BEE register.	UUU1040S	UINT16
DCT_UNIT1_HK_DU1_XPOL_RO_PEDSUB_NSMP	DU1 xpol ro pedsub nsmp BEE register.	UUU1041S	UINT16
DCT_UNIT1_HK_DU1_XPOL_RO_PEDSUB_PXTH	DU1 xpol ro pedsub pxth BEE register.	UUU1042S	UINT16
DCT_UNIT1_HK_DU1_WIN_D_UPP_LIM_LSW	DU1 win d upp lim lsw BEE register.	UUU1043S	UINT16
DCT_UNIT1_HK_DU1_WIN_D_UPP_LIM_MSW	DU1 win d upp lim msw BEE register.	UUU1044S	UINT16
DCT_UNIT1_HK_DU1_WIN_D_LOW_LIM	DU1 win d low lim BEE register.	UUU1045S	UINT16
DCT_UNIT1_HK_DU1_CK_PER_CYCLES	DU1 ck per cycles BEE register.	UUU1052S	UINT16
DCT_UNIT1_HK_DU1_CK_SHIFT_CYCLES	DU1 ck shift cycles BEE register.	UUU1053S	UINT16
DCT_UNIT1_HK_DU1_XPOL_RO_INJ_WIDTH	DU1 xpol ro inj width BEE register.	UUU1054S	UINT16
DCT_UNIT1_HK_DU1_XPOL_RO_INJ_PERIOD	DU1 xpol ro inj period BEE register.	UUU1055S	UINT16
DCT_UNIT1_HK_DU1_COMPR_START_ADDR	DU1 compr start addr BEE register.	UUU1056S	UINT16
DCT_UNIT1_HK_DU1_SDI_START_ADDR	DU1 sdi start addr BEE register.	UUU1057S	UINT16

DCT_UNIT1_HK_DU1_XPOL_READ_OUT	DU1 xpol read out BEE register.	UUU1058S	UINT16
DCT_UNIT1_HK_DU1_XPOL_X_ADDR	DU1 xpol x addr BEE register.	UUU1059S	UINT16
DCT_UNIT1_HK_DU1_XPOL_Y_ADDR	DU1 xpol y addr BEE register.	UUU1060S	UINT16
DCT_UNIT1_HK_DU1_XPOL_SI_CONF_RB	DU1 xpol si conf rb BEE register.	UUU1061S	UINT16
DCT_UNIT1_HK_DU1_XPOL_SI_ADDR_RB_LSB	DU1 xpol si addr rb lsb BEE register.	UUU1062S	UINT16
DCT_UNIT1_HK_DU1_XPOL_SI_ADDR_RB_MSB	DU1 xpol si addr rb msb BEE register.	UUU1063S	UINT16
DCT_UNIT1_HK_DU1_XPOL_CONF	DU1 xpol conf BEE register.	UUU1069S	UINT16
DCT_UNIT1_HK_DU1_BR_RAM_A_DATA_IN	DU1 br ram a data in BEE register.	UUU1070S	UINT16
DCT_UNIT1_HK_DU1_BR_RAM_A_ADD	DU1 br ram a add BEE register.	UUU1071S	UINT16
DCT_UNIT1_HK_DU1_BR_RAM_A_CTRLS	DU1 br ram a ctrls BEE register.	UUU1072S	UINT16
DCT_UNIT1_HK_DU1_BR_RAM_B_DATA_IN	DU1 br ram b data in BEE register.	UUU1073S	UINT16
DCT_UNIT1_HK_DU1_BR_RAM_B_ADD	DU1 br ram b add BEE register.	UUU1074S	UINT16
DCT_UNIT1_HK_DU1_BR_RAM_B_CTRLS	DU1 br ram b ctrls BEE register.	UUU1075S	UINT16
DCT_UNIT1_HK_DU1_HV_CTRL	DU1 hv ctrl BEE register.	UUU1076S	UINT16
DCT_UNIT1_HK_DU1_DAC_VBOTTOM_CONFIG	DU1 dac vbottom config BEE register.	UUU1077S	UINT16
DCT_UNIT1_HK_DU1_DAC_VGEM_CONFIG	DU1 dac vgem config BEE register.	UUU1078S	UINT16
DCT_UNIT1_HK_DU1_DAC_VDRIFT_CONFIG	DU1 dac vdrift config BEE register.	UUU1079S	UINT16
DCT_UNIT1_HK_DU1_CURRENT_HV1_ALARM_TH	DU1 current hv1 alarm th BEE register.	UUU1081S	UINT16
DCT_UNIT1_HK_DU1_CURRENT_HV2_ALARM_TH	DU1 current hv2 alarm th BEE register.	UUU1082S	UINT16
DCT_UNIT1_HK_DU1_CURRENT_HV3_ALARM_TH	DU1 current hv3 alarm th BEE register.	UUU1083S	UINT16

DCT_UNIT1_HK_DU1_CURRENT_5_V_ALARM_TH	DU1 current 5 v alarm th BEE register.	UUU1084S	UINT16
DCT_UNIT1_HK_DU1_CURRENT_3_V3_ALARM_TH	DU1 current 3 v3 alarm th BEE register.	UUU1085S	UINT16
DCT_UNIT1_HK_DU1_CURRENT_1_V8_ALARM_TH	DU1 current 1 v8 alarm th BEE register.	UUU1086S	UINT16
DCT_UNIT1_HK_DU1_CURRENT_1_V5_ALARM_TH	DU1 current 1 v5 alarm th BEE register.	UUU1087S	UINT16
DCT_UNIT1_HK_DU1_SDI_PARAMS	DU1 sdi params BEE register.	UUU1088S	UINT16
DCT_UNIT1_HK_DU1_SDI_RTX_WAIT_TIME	DU1 sdi rtx wait time BEE register.	UUU1089S	UINT16
DCT_UNIT1_HK_DU1_VOLTAGE_HV_DRIFT_TH	DU1 voltage hv drift th BEE register.	UUU1090S	UINT16
DCT_UNIT1_HK_DU1_VOLTAGE_HV_TOP_TH	DU1 voltage hv top th BEE register.	UUU1091S	UINT16
DCT_UNIT1_HK_DU1_VOLTAGE_HV_BOT_TH	DU1 voltage hv bot th BEE register.	UUU1092S	UINT16
DCT_UNIT1_HK_DU1_TS_SECS_PRESET_LSB	DU1 ts secs preset lsb BEE register.	UUU1093S	UINT16
DCT_UNIT1_HK_DU1_TS_SECS_PRESET_MSB	DU1 ts secs preset msb BEE register.	UUU1094S	UINT16
DCT_UNIT1_HK_DU1_TEST	DU1 test BEE register.	UUU1097S	UINT16
DCT_UNIT1_HK_DU1_PHA_ULIM_COUNTER	DU1 pha ulim counter BEE register.	UUU1098S	UINT16
DCT_UNIT1_HK_DU1_PHA_LLIM_COUNTER	DU1 pha llim counter BEE register.	UUU1099S	UINT16
DCT_UNIT1_HK_DU1_PHA_ULIM_TH	DU1 pha ulim th BEE register.	UUU1100S	UINT16
DCT_UNIT1_HK_DU1_PHA_LLIM_TH	DU1 pha llim th BEE register.	UUU1101S	UINT16
DCT_UNIT1_HK_DU1_PEDS_MEMORY_OFFSET	DU1 peds memory offset BEE register.	UUU1102S	UINT16
DCT_UNIT1_HK_DU1_HV_RAMP_CTRL	DU1 hv ramp ctrl BEE register.	UUU1103S	UINT16
DCT_UNIT1_HK_DU1_PIXEL_SCAN_CTRL	DU1 pixel scan ctrl BEE register.	UUU1104S	UINT16

DCT_UNIT1_HK_DU1_SCAN_NUMBER_STEPS_X	DU1 scan number steps x BEE register.	UUU1105S	UINT16
DCT_UNIT1_HK_DU1_SCAN_NUMBER_STEPS_Y	DU1 scan number steps y BEE register.	UUU1106S	UINT16
DCT_UNIT1_HK_DU1_SCAN_DELTA_X	DU1 scan delta x BEE register.	UUU1107S	UINT16
DCT_UNIT1_HK_DU1_SCAN_DELTA_Y	DU1 scan delta y BEE register.	UUU1108S	UINT16
DCT_UNIT1_HK_DU1_DIAG_EVT_REFRESH	DU1 diag evt refresh BEE register.	UUU1109S	UINT16
DCT_UNIT1_HK_DU1_PARITY_ERR_COUNTER	DU1 parity err counter BEE register.	UUU1110S	UINT16
DCT_UNIT2_HK_DU2_DATA_VALIDITY	DU2 data validity.	UUU2113S	UINT8
DCT_UNIT2_HK_DU2_RUN_ID	DU2 run id.	UUU0008N	UINT32
DCT_UNIT2_HK_DU2_OBT_SECONDS	DU2 obt seconds.	UUU2115H	UINT32
DCT_UNIT2_HK_DU2_OBT_MICROSECONDS	DU2 obt microseconds.	UUU2116H	UINT32
DCT_UNIT2_HK_DU2_OBT_ERROR	DU2 obt error.	UUU2117H	INT32
DCT_UNIT2_HK_DU2_CONFIG_REGA	DU2 config rega BEE register.	UUU2000S	UINT16
DCT_UNIT2_HK_DU2_CONFIG_REGB	DU2 config regb BEE register.	UUU2001S	UINT16
DCT_UNIT2_HK_DU2_HK_1_CONFIG	DU2 hk 1 config BEE register.	UUU2002S	UINT16
DCT_UNIT2_HK_DU2_HK_2_CONFIG	DU2 hk 2 config BEE register.	UUU2003S	UINT16
DCT_UNIT2_HK_DU2_HK_3_CONFIG	DU2 hk 3 config BEE register.	UUU2004S	UINT16
DCT_UNIT2_HK_DU2_SPARE_LVPS_1	DU2 spare lvps 1 BEE register.	UUU2011U	UINT16
DCT_UNIT2_HK_DU2_SPARE_DAQ_1	DU2 spare daq 1 BEE register.	UUU2017U	UINT16
DCT_UNIT2_HK_DU2_CURRENT_PWR_IN	DU2 current pwr in BEE register.	UUU2021I	UINT16
DCT_UNIT2_HK_DU2_SPARE_LPVS_2	DU2 spare lpvs 2 BEE register.	UUU2022U	UINT16
DCT_UNIT2_HK_DU2_SPARE_DAQ_2	DU2 spare daq 2 BEE register.	UUU2028U	UINT16

DCT_UNIT2_HK_DU2_READ_TEST	DU2 read test BEE register.	UUU2029S	UINT16
DCT_UNIT2_HK_DU2_DAC_VTH_CTRL	DU2 dac vth ctrl BEE register.	UUU2030S	UINT16
DCT_UNIT2_HK_DU2_DAC_VTEST_CTRL	DU2 dac vtest ctrl BEE register.	UUU2031S	UINT16
DCT_UNIT2_HK_DU2_ADC_XPOL_TI_DATA_IN	DU2 adc xpol ti data in BEE register.	UUU2032S	UINT16
DCT_UNIT2_HK_DU2_ADC_XPOL_TI_DATA_OUT	DU2 adc xpol ti data out BEE register.	UUU2033S	UINT16
DCT_UNIT2_HK_DU2_ADC_XPOL_TI_CTRL	DU2 adc xpol ti ctrl BEE register.	UUU2034S	UINT16
DCT_UNIT2_HK_DU2_ADC_XPOL_CLK_DIVIDER	DU2 adc xpol clk divider BEE register.	UUU2035S	UINT16
DCT_UNIT2_HK_DU2_XPOL_RO_CTRL	DU2 xpol ro ctrl BEE register.	UUU2036S	UINT16
DCT_UNIT2_HK_DU2_XPOL_RO_DISCH_WIDTH	DU2 xpol ro disch width BEE register.	UUU2038S	UINT16
DCT_UNIT2_HK_DU2_XPOL_RO_MH_CYCLES	DU2 xpol ro mh cycles BEE register.	UUU2039S	UINT16
DCT_UNIT2_HK_DU2_ALARM_OUT_CONFIG	DU2 alarm out config BEE register.	UUU2040S	UINT16
DCT_UNIT2_HK_DU2_XPOL_RO_PEDSUB_NSMP	DU2 xpol ro pedsub nsmp BEE register.	UUU2041S	UINT16
DCT_UNIT2_HK_DU2_XPOL_RO_PEDSUB_PXTH	DU2 xpol ro pedsub pxth BEE register.	UUU2042S	UINT16
DCT_UNIT2_HK_DU2_WIN_D_UPP_LIM_LSW	DU2 win d upp lim lsw BEE register.	UUU2043S	UINT16
DCT_UNIT2_HK_DU2_WIN_D_UPP_LIM_MSW	DU2 win d upp lim msw BEE register.	UUU2044S	UINT16
DCT_UNIT2_HK_DU2_WIN_D_LOW_LIM	DU2 win d low lim BEE register.	UUU2045S	UINT16
DCT_UNIT2_HK_DU2_CK_PER_CYCLES	DU2 ck per cycles BEE register.	UUU2052S	UINT16
DCT_UNIT2_HK_DU2_CK_SHIFT_CYCLES	DU2 ck shift cycles BEE register.	UUU2053S	UINT16
DCT_UNIT2_HK_DU2_XPOL_RO_INJ_WIDTH	DU2 xpol ro inj width BEE register.	UUU2054S	UINT16

DCT_UNIT2_HK_DU2_XPOL_RO_INJ_PERIOD	DU2 xpol ro inj period BEE register.	UUU2055S	UINT16
DCT_UNIT2_HK_DU2_COMPR_START_ADDR	DU2 compr start addr BEE register.	UUU2056S	UINT16
DCT_UNIT2_HK_DU2_SDI_START_ADDR	DU2 sdi start addr BEE register.	UUU2057S	UINT16
DCT_UNIT2_HK_DU2_XPOL_READ_OUT	DU2 xpol read out BEE register.	UUU2058S	UINT16
DCT_UNIT2_HK_DU2_XPOL_X_ADDR	DU2 xpol x addr BEE register.	UUU2059S	UINT16
DCT_UNIT2_HK_DU2_XPOL_Y_ADDR	DU2 xpol y addr BEE register.	UUU2060S	UINT16
DCT_UNIT2_HK_DU2_XPOL_SI_CONF_RB	DU2 xpol si conf rb BEE register.	UUU2061S	UINT16
DCT_UNIT2_HK_DU2_XPOL_SI_ADDR_RB_LSB	DU2 xpol si addr rb lsb BEE register.	UUU2062S	UINT16
DCT_UNIT2_HK_DU2_XPOL_SI_ADDR_RB_MSB	DU2 xpol si addr rb msb BEE register.	UUU2063S	UINT16
DCT_UNIT2_HK_DU2_XPOL_CONF	DU2 xpol conf BEE register.	UUU2069S	UINT16
DCT_UNIT2_HK_DU2_BR_RAM_A_DATA_IN	DU2 br ram a data in BEE register.	UUU2070S	UINT16
DCT_UNIT2_HK_DU2_BR_RAM_A_ADD	DU2 br ram a add BEE register.	UUU2071S	UINT16
DCT_UNIT2_HK_DU2_BR_RAM_A_CTRLS	DU2 br ram a ctrls BEE register.	UUU2072S	UINT16
DCT_UNIT2_HK_DU2_BR_RAM_B_DATA_IN	DU2 br ram b data in BEE register.	UUU2073S	UINT16
DCT_UNIT2_HK_DU2_BR_RAM_B_ADD	DU2 br ram b add BEE register.	UUU2074S	UINT16
DCT_UNIT2_HK_DU2_BR_RAM_B_CTRLS	DU2 br ram b ctrls BEE register.	UUU2075S	UINT16
DCT_UNIT2_HK_DU2_HV_CTRL	DU2 hv ctrl BEE register.	UUU2076S	UINT16
DCT_UNIT2_HK_DU2_DAC_VBOTTOM_CONFIG	DU2 dac vbottom config BEE register.	UUU2077S	UINT16
DCT_UNIT2_HK_DU2_DAC_VGEM_CONFIG	DU2 dac vgem config BEE register.	UUU2078S	UINT16
DCT_UNIT2_HK_DU2_DAC_VDRIFT_CONFIG	DU2 dac vdrift config BEE register.	UUU2079S	UINT16

DCT_UNIT2_HK_DU2_CURRENT_HV1_ALARM_TH	DU2 current hv1 alarm th BEE register.	UUU2081S	UINT16
DCT_UNIT2_HK_DU2_CURRENT_HV2_ALARM_TH	DU2 current hv2 alarm th BEE register.	UUU2082S	UINT16
DCT_UNIT2_HK_DU2_CURRENT_HV3_ALARM_TH	DU2 current hv3 alarm th BEE register.	UUU2083S	UINT16
DCT_UNIT2_HK_DU2_CURRENT_5_V_ALARM_TH	DU2 current 5 v alarm th BEE register.	UUU2084S	UINT16
DCT_UNIT2_HK_DU2_CURRENT_3_V3_ALARM_TH	DU2 current 3 v3 alarm th BEE register.	UUU2085S	UINT16
DCT_UNIT2_HK_DU2_CURRENT_1_V8_ALARM_TH	DU2 current 1 v8 alarm th BEE register.	UUU2086S	UINT16
DCT_UNIT2_HK_DU2_CURRENT_1_V5_ALARM_TH	DU2 current 1 v5 alarm th BEE register.	UUU2087S	UINT16
DCT_UNIT2_HK_DU2_SDI_PARAMS	DU2 sdi params BEE register.	UUU2088S	UINT16
DCT_UNIT2_HK_DU2_SDI_RTX_WAIT_TIME	DU2 sdi rtx wait time BEE register.	UUU2089S	UINT16
DCT_UNIT2_HK_DU2_VOLTAGE_HV_DRIFT_TH	DU2 voltage hv drift th BEE register.	UUU2090S	UINT16
DCT_UNIT2_HK_DU2_VOLTAGE_HV_TOP_TH	DU2 voltage hv top th BEE register.	UUU2091S	UINT16
DCT_UNIT2_HK_DU2_VOLTAGE_HV_BOT_TH	DU2 voltage hv bot th BEE register.	UUU2092S	UINT16
DCT_UNIT2_HK_DU2_TS_SECS_PRESET_LSB	DU2 ts secs preset lsb BEE register.	UUU2093S	UINT16
DCT_UNIT2_HK_DU2_TS_SECS_PRESET_MSB	DU2 ts secs preset msb BEE register.	UUU2094S	UINT16
DCT_UNIT2_HK_DU2_TEST	DU2 test BEE register.	UUU2097S	UINT16
DCT_UNIT2_HK_DU2_PHA_ULIM_COUNTER	DU2 pha ulim counter BEE register.	UUU2098S	UINT16
DCT_UNIT2_HK_DU2_PHA_LLIM_COUNTER	DU2 pha llim counter BEE register.	UUU2099S	UINT16
DCT_UNIT2_HK_DU2_PHA_ULIM_TH	DU2 pha ulim th BEE register.	UUU2100S	UINT16
DCT_UNIT2_HK_DU2_PHA_LLIM_TH	DU2 pha llim th BEE register.	UUU2101S	UINT16

DCT_UNIT2_HK_DU2_PEDS_MEMORY	DU2 peds memory BEE register.	UUU2102S	UINT16
DCT_UNIT2_HK_DU2_HV_RAMP_CTRL	DU2 hv ramp ctrl BEE register.	UUU2103S	UINT16
DCT_UNIT2_HK_DU2_PIXEL_SCAN_CTRL	DU2 pixel scan ctrl BEE register.	UUU2104S	UINT16
DCT_UNIT2_HK_DU2_SCAN_NUMBER_STEPS_X	DU2 scan number steps x BEE register.	UUU2105S	UINT16
DCT_UNIT2_HK_DU2_SCAN_NUMBER_STEPS_Y	DU2 scan number steps y BEE register.	UUU2106S	UINT16
DCT_UNIT2_HK_DU2_SCAN_DELTA_X	DU2 scan delta x BEE register.	UUU2107S	UINT16
DCT_UNIT2_HK_DU2_SCAN_DELTA_Y	DU2 scan delta y BEE register.	UUU2108S	UINT16
DCT_UNIT2_HK_DU2_DIAG_EVT_REFRESH	DU2 diag evt refresh BEE register.	UUU2109S	UINT16
DCT_UNIT2_HK_DU2_PARITY_ERR_COUNTER	DU2 parity err counter BEE register.	UUU2110S	UINT16
DCT_UNIT3_HK_DU3_DATA_VALIDITY	DU3 data validity.	UUU3113S	UINT8
DCT_UNIT3_HK_DU3_RUN_ID	DU3 run id.	UUU0009N	UINT32
DCT_UNIT3_HK_DU3_OBT_SECONDS	DU3 obt seconds.	UUU3115H	UINT32
DCT_UNIT3_HK_DU3_OBT_MICROSECONDS	DU3 obt microseconds.	UUU3116H	UINT32
DCT_UNIT3_HK_DU3_OBT_ERROR	DU3 obt error.	UUU3117H	INT32
DCT_UNIT3_HK_DU3_CONFIG_REGA	DU3 config rega BEE register.	UUU3000S	UINT16
DCT_UNIT3_HK_DU3_CONFIG_REGB	DU3 config regb BEE register.	UUU3001S	UINT16
DCT_UNIT3_HK_DU3_HK_1_CONFIG	DU3 hk 1 config BEE register.	UUU3002S	UINT16
DCT_UNIT3_HK_DU3_HK_2_CONFIG	DU3 hk 2 config BEE register.	UUU3003S	UINT16
DCT_UNIT3_HK_DU3_HK_3_CONFIG	DU3 hk 3 config BEE register.	UUU3004S	UINT16
DCT_UNIT3_HK_DU3_SPARE_LVPS_1	DU3 spare lvps 1 BEE register.	UUU3011U	UINT16
DCT_UNIT3_HK_DU3_SPARE_DAQ_1	DU3 spare daq 1 BEE register.	UUU3017U	UINT16

DCT_UNIT3_HK_DU3_CURRENT_PWR_IN	DU3 current pwr in BEE register.	UUU3021I	UINT16
DCT_UNIT3_HK_DU3_SPARE_LPVS_2	DU3 spare lpvs 2 BEE register.	UUU3022U	UINT16
DCT_UNIT3_HK_DU3_SPARE_DAQ_2	DU3 spare daq 2 BEE register.	UUU3028U	UINT16
DCT_UNIT3_HK_DU3_READ_TEST	DU3 read test BEE register.	UUU3029S	UINT16
DCT_UNIT3_HK_DU3_DAC_VTH_CTRL	DU3 dac vth ctrl BEE register.	UUU3030S	UINT16
DCT_UNIT3_HK_DU3_DAC_VTEST_CTRL	DU3 dac vtest ctrl BEE register.	UUU3031S	UINT16
DCT_UNIT3_HK_DU3_ADC_XPOL_TI_DATA_IN	DU3 adc xpol ti data in BEE register.	UUU3032S	UINT16
DCT_UNIT3_HK_DU3_ADC_XPOL_TI_DATA_OUT	DU3 adc xpol ti data out BEE register.	UUU3033S	UINT16
DCT_UNIT3_HK_DU3_ADC_XPOL_TI_CTRL	DU3 adc xpol ti ctrl BEE register.	UUU3034S	UINT16
DCT_UNIT3_HK_DU3_ADC_XPOL_CLK_DIVIDER	DU3 adc xpol clk divider BEE register.	UUU3035S	UINT16
DCT_UNIT3_HK_DU3_XPOL_RO_CTRL	DU3 xpol ro ctrl BEE register.	UUU3036S	UINT16
DCT_UNIT3_HK_DU3_XPOL_RO_DISCH_WIDTH	DU3 xpol ro disch width BEE register.	UUU3038S	UINT16
DCT_UNIT3_HK_DU3_XPOL_RO_MH_CYCLES	DU3 xpol ro mh cycles BEE register.	UUU3039S	UINT16
DCT_UNIT3_HK_DU3_ALARM_OUT_CONFIG	DU3 alarm out config BEE register.	UUU3040S	UINT16
DCT_UNIT3_HK_DU3_XPOL_RO_PEDSUB_NSMP	DU3 xpol ro pedsub nsmp BEE register.	UUU3041S	UINT16
DCT_UNIT3_HK_DU3_XPOL_RO_PEDSUB_PXTH	DU3 xpol ro pedsub pxth BEE register.	UUU3042S	UINT16
DCT_UNIT3_HK_DU3_WIN_D_UPP_LIM_LSW	DU3 win d upp lim lsw BEE register.	UUU3043S	UINT16
DCT_UNIT3_HK_DU3_WIN_D_UPP_LIM_MSW	DU3 win d upp lim msw BEE register.	UUU3044S	UINT16
DCT_UNIT3_HK_DU3_WIN_D_LOW_LIM	DU3 win d low lim BEE register.	UUU3045S	UINT16

DCT_UNIT3_HK_DU3_CK_PER_CYCLES	DU3 ck per cycles BEE register.	UUU3052S	UINT16
DCT_UNIT3_HK_DU3_CK_SHIFT_CYCLES	DU3 ck shift cycles BEE register.	UUU3053S	UINT16
DCT_UNIT3_HK_DU3_XPOL_RO_INJ_WIDTH	DU3 xpol ro inj width BEE register.	UUU3054S	UINT16
DCT_UNIT3_HK_DU3_XPOL_RO_INJ_PERIOD	DU3 xpol ro inj period BEE register.	UUU3055S	UINT16
DCT_UNIT3_HK_DU3_COMPR_START_ADDR	DU3 compr start addr BEE register.	UUU3056S	UINT16
DCT_UNIT3_HK_DU3_SDI_START_ADDR	DU3 sdi start addr BEE register.	UUU3057S	UINT16
DCT_UNIT3_HK_DU3_XPOL_READ_OUT	DU3 xpol read out BEE register.	UUU3058S	UINT16
DCT_UNIT3_HK_DU3_XPOL_X_ADDR	DU3 xpol x addr BEE register.	UUU3059S	UINT16
DCT_UNIT3_HK_DU3_XPOL_Y_ADDR	DU3 xpol y addr BEE register.	UUU3060S	UINT16
DCT_UNIT3_HK_DU3_XPOL_SI_CONF_RB	DU3 xpol si conf rb BEE register.	UUU3061S	UINT16
DCT_UNIT3_HK_DU3_XPOL_SI_ADDR_RB_LSB	DU3 xpol si addr rb lsb BEE register.	UUU3062S	UINT16
DCT_UNIT3_HK_DU3_XPOL_SI_ADDR_RB_MSB	DU3 xpol si addr rb msb BEE register.	UUU3063S	UINT16
DCT_UNIT3_HK_DU3_XPOL_CONF	DU3 xpol conf BEE register.	UUU3069S	UINT16
DCT_UNIT3_HK_DU3_BR_RAM_A_DATA_IN	DU3 br ram a data in BEE register.	UUU3070S	UINT16
DCT_UNIT3_HK_DU3_BR_RAM_A_ADD	DU3 br ram a add BEE register.	UUU3071S	UINT16
DCT_UNIT3_HK_DU3_BR_RAM_A_CTRLS	DU3 br ram a ctrls BEE register.	UUU3072S	UINT16
DCT_UNIT3_HK_DU3_BR_RAM_B_DATA_IN	DU3 br ram b data in BEE register.	UUU3073S	UINT16
DCT_UNIT3_HK_DU3_BR_RAM_B_ADD	DU3 br ram b add BEE register.	UUU3074S	UINT16
DCT_UNIT3_HK_DU3_BR_RAM_B_CTRLS	DU3 br ram b ctrls BEE register.	UUU3075S	UINT16
DCT_UNIT3_HK_DU3_HV_CTRL	DU3 hv ctrl BEE register.	UUU3076S	UINT16

DCT_UNIT3_HK_DU3_DAC_VBOTTOM_CONFIG	DU3 dac vbottom config BEE register.	UUU3077S	UINT16
DCT_UNIT3_HK_DU3_DAC_VGEM_CONFIG	DU3 dac vgem config BEE register.	UUU3078S	UINT16
DCT_UNIT3_HK_DU3_DAC_VDRIFT_CONFIG	DU3 dac vdrift config BEE register.	UUU3079S	UINT16
DCT_UNIT3_HK_DU3_CURRENT_HV1_ALARM_TH	DU3 current hv1 alarm th BEE register.	UUU3081S	UINT16
DCT_UNIT3_HK_DU3_CURRENT_HV2_ALARM_TH	DU3 current hv2 alarm th BEE register.	UUU3082S	UINT16
DCT_UNIT3_HK_DU3_CURRENT_HV3_ALARM_TH	DU3 current hv3 alarm th BEE register.	UUU3083S	UINT16
DCT_UNIT3_HK_DU3_CURRENT_5_V_ALARM_TH	DU3 current 5 v alarm th BEE register.	UUU3084S	UINT16
DCT_UNIT3_HK_DU3_CURRENT_3_V3_ALARM_TH	DU3 current 3 v3 alarm th BEE register.	UUU3085S	UINT16
DCT_UNIT3_HK_DU3_CURRENT_1_V8_ALARM_TH	DU3 current 1 v8 alarm th BEE register.	UUU3086S	UINT16
DCT_UNIT3_HK_DU3_CURRENT_1_V5_ALARM_TH	DU3 current 1 v5 alarm th BEE register.	UUU3087S	UINT16
DCT_UNIT3_HK_DU3_SDI_PARAMS	DU3 sdi params BEE register.	UUU3088S	UINT16
DCT_UNIT3_HK_DU3_SDI_RTX_WAIT_TIME	DU3 sdi rtx wait time BEE register.	UUU3089S	UINT16
DCT_UNIT3_HK_DU3_VOLTAGE_HV_DRIFT_TH	DU3 voltage hv drift th BEE register.	UUU3090S	UINT16
DCT_UNIT3_HK_DU3_VOLTAGE_HV_TOP_TH	DU3 voltage hv top th BEE register.	UUU3091S	UINT16
DCT_UNIT3_HK_DU3_VOLTAGE_HV_BOT_TH	DU3 voltage hv bot th BEE register.	UUU3092S	UINT16
DCT_UNIT3_HK_DU3_TS_SECS_PRESET_LSB	DU3 ts secs preset lsb BEE register.	UUU3093S	UINT16
DCT_UNIT3_HK_DU3_TS_SECS_PRESET_MSB	DU3 ts secs preset msb BEE register.	UUU3094S	UINT16
DCT_UNIT3_HK_DU3_TEST	DU3 test BEE register.	UUU3097S	UINT16
DCT_UNIT3_HK_DU3_PHA_ULIM_COUNTER	DU3 pha ulim counter BEE register.	UUU3098S	UINT16

DCT_UNIT3_HK_DU3_PHA_LLIM_COUNTER	DU3 pha llim counter BEE register.	UUU3099S	UINT16
DCT_UNIT3_HK_DU3_PHA_ULIM_TH	DU3 pha ulim th BEE register.	UUU3100S	UINT16
DCT_UNIT3_HK_DU3_PHA_LLIM_TH	DU3 pha llim th BEE register.	UUU3101S	UINT16
DCT_UNIT3_HK_DU3_PEDS_MEMORY	DU3 peds memory BEE register.	UUU3102S	UINT16
DCT_UNIT3_HK_DU3_HV_RAMP_CTRL	DU3 hv ramp ctrl BEE register.	UUU3103S	UINT16
DCT_UNIT3_HK_DU3_PIXEL_SCAN_CTRL	DU3 pixel scan ctrl BEE register.	UUU3104S	UINT16
DCT_UNIT3_HK_DU3_SCAN_NUMBER_STEPS_X	DU3 scan number steps x BEE register.	UUU3105S	UINT16
DCT_UNIT3_HK_DU3_SCAN_NUMBER_STEPS_Y	DU3 scan number steps y BEE register.	UUU3106S	UINT16
DCT_UNIT3_HK_DU3_SCAN_DELTA_X	DU3 scan delta x BEE register.	UUU3107S	UINT16
DCT_UNIT3_HK_DU3_SCAN_DELTA_Y	DU3 scan delta y BEE register.	UUU3108S	UINT16
DCT_UNIT3_HK_DU3_DIAG_EVT_REFRESH	DU3 diag evt refresh BEE register.	UUU3109S	UINT16
DCT_UNIT3_HK_DU3_PARITY_ERR_COUNTER	DU3 parity err counter BEE register.	UUU3110S	UINT16
OP_MODE_CMD_OP_MODE	Commanded DSU operative mode.	DDD0120S	UINT8
OP_MODE_CURRENT_OP_MODE	Current DSU operative mode.	DDD0121S	UINT8
OP_MODE_PREVIOUS_OP_MODE	Previous DSU operative mode.	DDD0122S	UINT8
OP_MODE_RUN_ID	Run identifier.	DDD0123N	UINT32
OP_MODE_MODE_TRANSITION_ERRORS	Operative mode transition errors.	DDD0124N	UINT32
TC_SRVC_TC_POOL_ERRORS	TC pool errors.	DDD0130N	UINT32
TC_SRVC_TC_READ_ERRORS	TC read errors.	DDD0131N	UINT32
TC_SRVC_TC_READ_NO_DATA_ERRORS	TC read no data errors.	DDD0132N	UINT32
TC_SRVC_TC_ERRORS	TC errors.	DDD0133N	UINT32

TC_SRVC_TC_PKT_LEN_ERRORS	TC packet length errors.	DDD0134N	UINT32
TC_SRVC_TC_UART_FRM_ERRORS	TC UART framing errors.	DDD0135N	UINT32
TC_SRVC_TC_UART_OFLW_ERRORS	TC UART overflow errors.	DDD0136N	UINT32
TC_SRVC_TC_UART_PARITY_ERRORS	TC UART parity errors.	DDD0137N	UINT32
TC_SRVC_TC_RCPT_TOUT_ERRORS	TC reception timeout.	DDD0138N	UINT32
TC_SRVC_TC_BUFFER_FULL_ERRORS	TC buffer full errors.	DDD0139N	UINT32
TC_SRVC_TC_MEM_POOL_USED	TC memory pool used.	DDD0140X	UINT32
TC_SRVC_TC_MEM_POOL_SIZE	TC memory pool size.	DDD0141X	UINT32
TC_SRVC_TC_RECV_COUNT	TC received counter.	DDD0142N	UINT32
TM_SRVC_TM_DEFER_QUEUE_ERRORS	TM deferred queue errors.	DDD0150N	UINT32
TM_SRVC_TM_POOL_ERRORS	TM pool errors.	DDD0151N	UINT32
TM_SRVC_TM_UNKNOWN_ERRORS	TM unknown errors.	DDD0152N	UINT32
TM_SRVC_TM_WRITE_BUSY_ERRORS	TM write busy errors.	DDD0153N	UINT32
TM_SRVC_TM_WRITE_ERRORS	TM write errors.	DDD0154N	UINT32
TM_SRVC_TM_WRITE_TIMEOUT_ERRORS	TM write timeout errors.	DDD0155N	UINT32
TM_SRVC_TM_PKT_LENGTH_ERRORS	TM packet length errors.	DDD0156N	UINT32
TM_SRVC_TM_PKT_ADDR_ERRORS	TM packet address errors.	DDD0157N	UINT32
TM_SRVC_TM_SENT_COUNT	TM sent count.	DDD0158N	UINT32
TM_SRVC_TM_MEM_POOL_SIZE	TM memory pool size.	DDD0159X	UINT32
TM_SRVC_TM_MEM_POOL_USED	TM memory pool used.	DDD0160X	UINT32
TM_SRVC_TM_CIRC_BUFF_SIZE	TM circular buffer size.	DDD0161X	UINT32
TM_SRVC_TM_CIRC_BUFF_USED	TM circular buffer used.	DDD0162X	UINT32
CMD_REP_TC_ACCEPT_ERRORS	TC acceptance errors.	DDD0170N	UINT32
CMD_REP_TC_EXEC_ERRORS	TC execution complete errors.	DDD0171N	UINT32
CMD_REP_TC_START_ERRORS	TC start of execution errors.	DDD0172N	UINT32
EVT_REP_EV_NORMAL_SEV_COUNTER	Normal severity events counter.	DDD0180N	UINT32
EVT_REP_EV_LOW_SEV_COUNTER	Low severity events counter.	DDD0181N	UINT32
EVT_REP_EV_MEDIUM_SEV_COUNTER	Medium severity events counter.	DDD0182N	UINT32
EVT_REP_EV_HIGH_SEV_COUNTER	High severity events counter.	DDD0183N	UINT32

OBT_CTRL_OBT_ERROR_REG	OnBoard time error register value.	DDD0190X	INT32
OBT_CTRL_OBT_MODE	Master OnBoard Time current mode.	DDD0191S	UINT32
OBT_CTRL_TOD_PROCESSING	Time of Day message processing inhibit flag.	DDD0192S	UINT8
OBT_CTRL_PPS_VALIDITY	Pulse per Second validity flag.	DDD0193S	UINT8
OBT_CTRL_TOD_READ_ERRORS	Time of day message read errors.	DDD0194N	UINT32
OBT_CTRL_TOD_TIMEOUT_ERRORS	Time of day message read time-out errors.	DDD0195N	UINT32
OBT_CTRL_FAILED_SET_TIME_COUNT	Failed set time counter.	DDD0196N	UINT32
OBT_CTRL_TOD_CDS_TIME	TOD CDS time.	DDD0197H	CDSTIME
OBT_CTRL_TOD_GPS_STATUS	TOD GPS status.	DDD0198S	UINT8
OBT_CTRL_TOD_GPS_SATS	TOD GPS satellites number.	DDD0199N	UINT8
OBT_CTRL_PPS_ACTIVE	Pulse per Second active flag.	DDD0200S	UINT8
THERM_CTRL1_DU1_THERMAL_DAC_ERRORS	DU1 thermal DAC set current errors.	DDD0210N	UINT32
THERM_CTRL1_DU1_THERMAL_OUTPUT	DU1 thermal output.	DDD0211S	UINT8
THERM_CTRL1_DU1_TEC_CURR_LIMIT	DU1 TEC current limit.	DDD0212I	UINT16
THERM_CTRL1_DU1_HOP_CURR_LIMIT	DU1 HOP current limit.	DDD0213I	UINT16
THERM_CTRL1_DU1_HOP_SET_POINT	DU1 HOP temperature set point.	DDD0214T	UINT16
THERM_CTRL1_DU1_TEC_SET_POINT	DU1 TEC temperature set point.	DDD0215T	UINT16
THERM_CTRL2_DU2_THERMAL_DAC_ERRORS	DU2 thermal DAC set current errors.	DDD0216N	UINT32
THERM_CTRL2_DU2_THERMAL_OUTPUT	DU2 thermal output.	DDD0217S	UINT8
THERM_CTRL2_DU2_TEC_CURR_LIMIT	DU2 TEC current limit.	DDD0218I	UINT16
THERM_CTRL2_DU2_HOP_CURR_LIMIT	DU2 HOP current limit.	DDD0219I	UINT16
THERM_CTRL2_DU2_HOP_SET_POINT	DU2 HOP temperature set point.	DDD0220T	UINT16
THERM_CTRL2_DU2_TEC_SET_POINT	DU2 TEC temperature set point.	DDD0221T	UINT16

THERM_CTRL3_DU3_THERMAL_DAC_ERRORS	DU3 thermal DAC set current errors.	DDD0222N	UINT32
THERM_CTRL3_DU3_THERMAL_OUTPUT	DU3 thermal output.	DDD0223S	UINT8
THERM_CTRL3_DU3_TEC_CURR_LIMIT	DU3 TEC current limit.	DDD0224I	UINT16
THERM_CTRL3_DU3_HOP_CURR_LIMIT	DU3 HOP current limit.	DDD0225I	UINT16
THERM_CTRL3_DU3_HOP_SET_POINT	DU3 HOP temperature set point.	DDD0226T	UINT16
THERM_CTRL3_DU3_TEC_SET_POINT	DU3 TEC temperature set point.	DDD0227T	UINT16
INST_CFG_MNGR_FCW1_HALL_POSITION	FCW1 hall position.	DDD0240S	UINT8
INST_CFG_MNGR_FCW2_HALL_POSITION	FCW2 hall position.	DDD0241S	UINT8
INST_CFG_MNGR_FCW3_HALL_POSITION	FCW3 hall position.	DDD0242S	UINT8
INST_CFG_MNGR_FCW_HIGH_POWER_STATUS	FCW high power status.	DDD0243S	UINT8
INST_CFG_MNGR_FCW_DEFER_QUEUE_ERRORS	FCW deferred TC queue errors.	DDD0244N	UINT32
INST_CFG_MNGR_FCW_TC_CIRC_BUFF_SIZE	FCW TC circular buffer size.	DDD0245X	UINT32
INST_CFG_MNGR_FCW_TC_CIRC_BUFF_USED	FCW TC circular buffer used.	DDD0246X	UINT32
INST_CFG_MNGR_DU1_5_V_STATUS	DU1 +5V status.	DDD0247S	UINT8
INST_CFG_MNGR_DU1_25_V_STATUS	DU1 +25V status.	DDD0248S	UINT8
INST_CFG_MNGR_DU2_5_V_STATUS	DU2 +5V status.	DDD0249S	UINT8
INST_CFG_MNGR_DU2_25_V_STATUS	DU2 +25V status.	DDD0250S	UINT8
INST_CFG_MNGR_DU3_5_V_STATUS	DU3 +5V status.	DDD0251S	UINT8
INST_CFG_MNGR_DU3_25_V_STATUS	DU3 +25V status.	DDD0252S	UINT8
FILTER_CAL1_FCW1_TIMEOUT_ERRORS	FCW1 positioning timeout errors.	DDD0260N	UINT32
FILTER_CAL2_FCW2_TIMEOUT_ERRORS	FCW2 positioning timeout errors.	DDD0261N	UINT32
FILTER_CAL3_FCW3_TIMEOUT_ERRORS	FCW3 positioning timeout errors.	DDD0262N	UINT32
MEM_MNGR_LEON_EDAC_MULTI_ERRORS	CPU EDAC uncorrected errors.	DDD0270N	UINT32
MEM_MNGR_LEON_EDAC_CORRECTIONS	CPU EDAC corrections.	DDD0271N	UINT32
MEM_MNGR_FPGA_EDAC_SINGLE_ERRORS	FPGA EDAC single-bit errors.	DDD0272N	UINT32

MEM_MNGR_FPGA_EDAC_MULTI_ERRORS	FPGA EDAC multiple-bits errors.	DDD0273N	UINT32
MEM_MNGR_MEM_DEFER_QUEUE_ERRORS	Memory deferred TC queue errors.	DDD0274N	UINT32
MEM_MNGR_MEM_TC_CIRC_BUFF_SIZE	Memory TC circular buffer size.	DDD0275N	UINT32
MEM_MNGR_MEM_TC_CIRC_BUFF_USED	Memory TC circular buffer used.	DDD0276N	UINT32
INST_CFG_MNGR_HI_RT_PH1_CURRENT	Peltier or heater 1 current.	DDD0280I	UINT16
INST_CFG_MNGR_HI_RT_PH2_CURRENT	Peltier or heater 2 current.	DDD0281I	UINT16
INST_CFG_MNGR_HI_RT_PH3_CURRENT	Peltier or heater 3 current.	DDD0282I	UINT16
INST_CFG_MNGR_HI_RT_PH1_VOLTAGE	Peltier or heater 1 voltage.	DDD0283U	UINT16
INST_CFG_MNGR_HI_RT_PH2_VOLTAGE	Peltier or heater 2 voltage.	DDD0284U	UINT16
INST_CFG_MNGR_HI_RT_PH3_VOLTAGE	Peltier or heater 3 voltage.	DDD0285U	UINT16
INST_CFG_MNGR_HI_RT_PSB_V_CLAMP	PSB clamp voltage.	DDD0286U	UINT16
INST_CFG_MNGR_HI_RT_GROUND	Ground reference.	DDD0287U	UINT16
INST_CFG_MNGR_HI_RT_FCW1_TEMPERATURE	FCW1 temperature.	DDD0288T	UINT16
INST_CFG_MNGR_HI_RT_FCW2_TEMPERATURE	FCW2 temperature.	DDD0289T	UINT16
INST_CFG_MNGR_HI_RT_FCW3_TEMPERATURE	FCW3 temperature.	DDD0290T	UINT16
INST_CFG_MNGR_HI_RT_GPD1_TEMPERATURE	GPD 1 temperature.	DDD0291T	UINT16
INST_CFG_MNGR_HI_RT_GPD2_TEMPERATURE	GPD 2 temperature.	DDD0292T	UINT16
INST_CFG_MNGR_HI_RT_GPD3_TEMPERATURE	GPD 3 temperature.	DDD0293T	UINT16
INST_CFG_MNGR_HI_RT_TEST_POINT_3_V3	3.3V test point.	DDD0294U	UINT16
INST_CFG_MNGR_HI_RT_TEST_POINT_2_V5	2.5V test point.	DDD0295U	UINT16
INST_CFG_MNGR_HI_RT_FCW1_POTENTIOMETER	FCW1 potentiometer.	DDD0296U	UINT16
INST_CFG_MNGR_HI_RT_FCW2_POTENTIOMETER	FCW2 potentiometer.	DDD0297U	UINT16
INST_CFG_MNGR_HI_RT_FCW3_POTENTIOMETER	FCW3 potentiometer.	DDD0298U	UINT16
INST_CFG_MNGR_HI_RT_SBC_CURRENT	SBC current.	DDD0299I	UINT16
INST_CFG_MNGR_HI_RT_SBC_VOLTAGE	SBC voltage.	DDD0300U	UINT16
INST_CFG_MNGR_HI_RT_PSB_TEMPERATURE	PSB temperature.	DDD0301T	UINT16
INST_CFG_MNGR_HI_RT_SBC_TEMPERATURE	PSB temperature.	DDD0301T	UINT16
INST_CFG_MNGR_HI_RT_TEST_POINT_15_V	15V test point.	DDD0303U	UINT16
RATE_MTR_RUN_ID	Run identifier.	DDD0400N	UINT32

RATE_MTR_OBT_SECONDS	Ratemeters seconds time-tag.	DDD0401H	UINT32
RATE_MTR_OBT_MICROSECONDS	Ratemeters microseconds time-tag.	DDD0402H	UINT32
RATE_MTR_OBT_ERROR	Ratemeters OBT error.	DDD0403H	INT32
RATE_MTR_DU1_TOTAL_CRC_ERRORS	DU1 total CRC errors.	DDD0404N	UINT32
RATE_MTR_DU1_TOTAL_EVT_COUNT	DU1 total events counter.	DDD0405N	UINT32
RATE_MTR_DU2_TOTAL_CRC_ERRORS	DU2 total CRC errors.	DDD0406N	UINT32
RATE_MTR_DU2_TOTAL_EVT_COUNT	DU2 total events counter.	DDD0407N	UINT32
RATE_MTR_DU3_TOTAL_CRC_ERRORS	DU3 total CRC errors.	DDD0408N	UINT32
RATE_MTR_DU3_TOTAL_EVT_COUNT	DU3 total events counter.	DDD0409N	UINT32
RATE_MTR_DU1_CRC_ERRORS	DU1 CRC errors.	DDD0410N	UINT16
RATE_MTR_DU1_EVT_COUNT	DU1 events counter.	DDD0411N	UINT16
RATE_MTR_DU1_PKT_LENGTH_SUM	DU1 packets length sum.	DDD0412N	UINT32
RATE_MTR_DU1_PKT_LENGTH_8K_COUNT	DU1 packets length > 8192 counter.	DDD0413N	UINT16
RATE_MTR_DU1_PKT_LENGTH_2K_COUNT	DU1 packets length > 2048 counter.	DDD0414N	UINT16
RATE_MTR_DU1_PKT_LEN_ERRORS	DU1 wrong length counter.	DDD0415N	UINT16
RATE_MTR_DU1_PKT_LENGHT_32_COUNT	DU1 packets length = 32 counter.	DDD0416N	UINT16
RATE_MTR_DU2_CRC_ERRORS	DU2 CRC errors.	DDD0430N	UINT16
RATE_MTR_DU2_EVT_COUNT	DU2 events counter.	DDD0431N	UINT16
RATE_MTR_DU2_PKT_LENGTH_SUM	DU2 packets length sum.	DDD0432N	UINT32
RATE_MTR_DU2_PKT_LENGTH_8K_COUNT	DU2 packets length > 8192 counter.	DDD0433N	UINT16
RATE_MTR_DU2_PKT_LENGTH_2K_COUNT	DU2 packets length > 2048 counter.	DDD0434N	UINT16
RATE_MTR_DU2_PKT_LEN_ERRORS	DU2 wrong length counter.	DDD0435N	UINT16
RATE_MTR_DU2_PKT_LENGHT_32_COUNT	DU2 packets length = 32 counter.	DDD0436N	UINT16
RATE_MTR_DU3_CRC_ERRORS	DU3 CRC errors.	DDD0450N	UINT16
RATE_MTR_DU3_EVT_COUNT	DU3 events counter.	DDD0451N	UINT16
RATE_MTR_DU3_PKT_LENGTH_SUM	DU3 packets length sum.	DDD0452N	UINT32

RATE_MTR_DU3_PKT_LENGTH_8K_COUNT	DU3 packets length > 8192 counter.	DDD0453N	UINT16
RATE_MTR_DU3_PKT_LENGTH_2K_COUNT	DU3 packets length > 2048 counter.	DDD0454N	UINT16
RATE_MTR_DU3_PKT_LEN_ERRORS	DU3 wrong length counter.	DDD0455N	UINT16
RATE_MTR_DU3_PKT_LENGHT_32_COUNT	DU3 packets length = 32 counter.	DDD0456N	UINT16
RATE_MTR_DU1_BO_PIXELS_SET1_COUNT	DU1 pixels = 1 counter before orphan removal.	DDD0470N	UINT32
RATE_MTR_DU1_BO_ENERGY_SUM	DU1 energy sum before orphan removal.	DDD0471N	UINT32
RATE_MTR_DU1_BO_PIXELS_COUNT	DU1 pixels counter before orphan removal.	DDD0472N	UINT32
RATE_MTR_DU1_AO_PIXELS_SET1_COUNT	DU1 pixels = 1 counter after orphan removal.	DDD0473N	UINT32
RATE_MTR_DU1_AO_ENERGY_SUM	DU1 energy sum after orphan removal.	DDD0474N	UINT32
RATE_MTR_DU1_AO_EVENTS_COUNT	DU1 events counter after orphan removal.	DDD0475N	UINT32
RATE_MTR_DU1_NP_EVENTS_COUNT	DU1 non-processed events counter.	DDD0476N	UINT32
RATE_MTR_DU2_BO_PIXELS_SET1_COUNT	DU2 pixels = 1 counter before orphan removal.	DDD0480N	UINT32
RATE_MTR_DU2_BO_ENERGY_SUM	DU2 energy sum before orphan removal.	DDD0481N	UINT32
RATE_MTR_DU2_BO_PIXELS_COUNT	DU2 pixels counter before orphan removal.	DDD0482N	UINT32
RATE_MTR_DU2_AO_PIXELS_SET1_COUNT	DU2 pixels = 1 counter after orphan removal.	DDD0483N	UINT32
RATE_MTR_DU2_AO_ENERGY_SUM	DU2 energy sum after orphan removal.	DDD0484N	UINT32
RATE_MTR_DU2_AO_EVENTS_COUNT	DU2 events counter after orphan removal.	DDD0485N	UINT32
RATE_MTR_DU2_NP_EVENTS_COUNT	DU2 non-processed events counter.	DDD0486N	UINT32
RATE_MTR_DU3_BO_PIXELS_SET1_COUNT	DU3 pixels = 1 counter before orphan removal.	DDD0490N	UINT32

RATE_MTR_DU3_BO_ENERGY_SUM	DU3 energy sum before orphan removal.	DDD0491N	UINT32
RATE_MTR_DU3_BO_PIXELS_COUNT	DU3 pixels counter before orphan removal.	DDD0492N	UINT32
RATE_MTR_DU3_AO_PIXELS_SET1_COUNT	DU3 pixels = 1 counter after orphan removal.	DDD0493N	UINT32
RATE_MTR_DU3_AO_ENERGY_SUM	DU3 energy sum after orphan removal.	DDD0494N	UINT32
RATE_MTR_DU3_AO_EVENTS_COUNT	DU3 events counter after orphan removal.	DDD0495N	UINT32
RATE_MTR_DU3_NP_EVENTS_COUNT	DU3 non-processed events counter.	DDD0496N	UINT32
DCT_UNIT1_CTRL_DU1_DEFER_QUEUE_ERRORS	DU1 deferred queue errors.	DDD0310N	UINT32
DCT_UNIT1_CTRL_DU1_CIRC_BUFF_SIZE	DU1 circular buffer size.	DDD0311N	UINT32
DCT_UNIT1_CTRL_DU1_CIRC_BUFF_USED	DU1 circular buffer used.	DDD0312N	UINT32
DCT_UNIT1_CTRL_DU1_CCI_READ_ERRORS	DU1 CCI read errors.	DDD0313N	UINT32
DCT_UNIT1_CTRL_DU1_CCI_WRITE_ERRORS	DU1 CCI write errors.	DDD0314N	UINT32
DCT_UNIT2_CTRL_DU2_DEFER_QUEUE_ERRORS	DU2 deferred queue errors.	DDD0315N	UINT32
DCT_UNIT2_CTRL_DU2_CIRC_BUFF_SIZE	DU2 circular buffer size.	DDD0316N	UINT32
DCT_UNIT2_CTRL_DU2_CIRC_BUFF_USED	DU2 circular buffer used.	DDD0317N	UINT32
DCT_UNIT2_CTRL_DU2_CCI_READ_ERRORS	DU2 CCI read errors.	DDD0318N	UINT32
DCT_UNIT2_CTRL_DU2_CCI_WRITE_ERRORS	DU2 CCI write errors.	DDD0319N	UINT32
DCT_UNIT3_CTRL_DU3_DEFER_QUEUE_ERRORS	DU3 deferred queue errors.	DDD0320N	UINT32
DCT_UNIT3_CTRL_DU3_CIRC_BUFF_SIZE	DU3 circular buffer size.	DDD0321N	UINT32
DCT_UNIT3_CTRL_DU3_CIRC_BUFF_USED	DU3 circular buffer used.	DDD0322N	UINT32
DCT_UNIT3_CTRL_DU3_CCI_READ_ERRORS	DU3 CCI read errors.	DDD0323N	UINT32
DCT_UNIT3_CTRL_DU3_CCI_WRITE_ERRORS	DU3 CCI write errors.	DDD0324N	UINT32
DCT_UNIT1_HK_HI_RT_DU1_HIRATE_DATA_VALIDITY	DU1 hirate data validity.	UUU1114S	UINT8
DCT_UNIT1_HK_HI_RT_DU1_HR_RUN_ID	DU1 hr run id.	UUU0004N	UINT32
DCT_UNIT1_HK_HI_RT_DU1_HR_OBT_SECONDS	DU1 hr obt seconds.	UUU1118H	UINT32
DCT_UNIT1_HK_HI_RT_DU1_HR_OBT_MICROSECONDS	DU1 hr obt microseconds.	UUU1119H	UINT32
DCT_UNIT1_HK_HI_RT_DU1_HR_OBT_ERROR	DU1 hr obt error.	UUU1120H	INT32

DCT_UNIT1_HK_HI_RT_DU1_VREF_XPOL	DU1 vref xpol BEE register.	UUU1005U	UINT16
DCT_UNIT1_HK_HI_RT_DU1_CURRENT_5_V	DU1 current 5v BEE register.	UUU1006I	UINT16
DCT_UNIT1_HK_HI_RT_DU1_CURRENT_3_V3	DU1 current 3v3 BEE register.	UUU1007I	UINT16
DCT_UNIT1_HK_HI_RT_DU1_CURRENT_1_V8	DU1 current 1v8 BEE register.	UUU1008I	UINT16
DCT_UNIT1_HK_HI_RT_DU1_TEMP_LVPS_1_V5	DU1 temp lvps 1v5 BEE register.	UUU1009T	UINT16
DCT_UNIT1_HK_HI_RT_DU1_TEMP_LVPS_1_V8	DU1 temp lvps 1v8 BEE register.	UUU1010T	UINT16
DCT_UNIT1_HK_HI_RT_DU1_TEMP_LVPS_3_V3	DU1 temp lvps 3v3 BEE register.	UUU1012T	UINT16
DCT_UNIT1_HK_HI_RT_DU1_TEMP_HV_1	DU1 temp hv 1 BEE register.	UUU1013T	UINT16
DCT_UNIT1_HK_HI_RT_DU1_TEMP_HV_2	DU1 temp hv 2 BEE register.	UUU1014T	UINT16
DCT_UNIT1_HK_HI_RT_DU1_CURRENT_HV_1	DU1 current hv 1 BEE register.	UUU1015I	UINT16
DCT_UNIT1_HK_HI_RT_DU1_CURRENT_HV_2	DU1 current hv 2 BEE register.	UUU1016I	UINT16
DCT_UNIT1_HK_HI_RT_DU1_TEMP_GPD	DU1 temp gpd BEE register.	UUU1018T	UINT16
DCT_UNIT1_HK_HI_RT_DU1_TEMP_DAQ_1	DU1 temp daq 1 BEE register.	UUU1019T	UINT16
DCT_UNIT1_HK_HI_RT_DU1_TEMP_DAQ_2	DU1 temp daq 2 BEE register.	UUU1020T	UINT16
DCT_UNIT1_HK_HI_RT_DU1_CURRENT_1_V5	DU1 current 1v5 BEE register.	UUU1023I	UINT16
DCT_UNIT1_HK_HI_RT_DU1_VOLTAGE_HV_DRIFT	DU1 voltage hv drift BEE register.	UUU1024U	UINT16
DCT_UNIT1_HK_HI_RT_DU1_VOLTAGE_HV_TOP	DU1 voltage hv top BEE register.	UUU1025U	UINT16
DCT_UNIT1_HK_HI_RT_DU1_VOLTAGE_HV_BOT	DU1 voltage hv bot BEE register.	UUU1026U	UINT16
DCT_UNIT1_HK_HI_RT_DU1_CURRENT_HV_3	DU1 current hv 3 BEE register.	UUU1027I	UINT16
DCT_UNIT1_HK_HI_RT_DU1_XPOL_RO_STATUS	DU1 xpol ro status BEE register.	UUU1037S	UINT16

DCT_UNIT1_HK_HI_RT_DU1_EVT_COUNTER_LSW	DU1 evt counter lsw BEE register.	UUU1046S	UINT16
DCT_UNIT1_HK_HI_RT_DU1_EVT_COUNTER_MSW	DU1 evt counter msw BEE register.	UUU1047S	UINT16
DCT_UNIT1_HK_HI_RT_DU1_WULIM_REJ_CNT_LS W	DU1 wulim rej cnt lsw BEE register.	UUU1048S	UINT16
DCT_UNIT1_HK_HI_RT_DU1_WLLIM_REJ_CNT_LS W	DU1 wllim rej cnt lsw BEE register.	UUU1050S	UINT16
DCT_UNIT1_HK_HI_RT_DU1_PPS_COUNTER_LSW	DU1 pps counter lsw BEE register.	UUU1064S	UINT16
DCT_UNIT1_HK_HI_RT_DU1_PPS_COUNTER_MSW	DU1 pps counter msw BEE register.	UUU1065S	UINT16
DCT_UNIT1_HK_HI_RT_DU1_USEC_COUNTER_LS W	DU1 usec counter lsw BEE register.	UUU1066S	UINT16
DCT_UNIT1_HK_HI_RT_DU1_USEC_COUNTER_MS W	DU1 usec counter msw BEE register.	UUU1067S	UINT16
DCT_UNIT1_HK_HI_RT_DU1_OBT_ERROR	DU1 obt error BEE register.	UUU1068S	INT16
DCT_UNIT1_HK_HI_RT_DU1_BEE_STATUS	DU1 bee status BEE register.	UUU1080S	UINT16
DCT_UNIT1_HK_HI_RT_DU1_HK_LIVE_TIME_LSB	DU1 hk live time lsb BEE register.	UUU1095S	UINT16
DCT_UNIT1_HK_HI_RT_DU1_HK_LIVE_TIME_MSB	DU1 hk live time msb BEE register.	UUU1096S	UINT16
DCT_UNIT1_HK_HI_RT_DU1_COUNTER_END_RO_ LSW	DU1 counter end ro lsw BEE register.	UUU1111S	UINT16
DCT_UNIT1_HK_HI_RT_DU1_COUNTER_END_RO_ MSW	DU1 counter end ro msw BEE register.	UUU1112S	UINT16
DCT_UNIT2_HK_HI_RT_DU2_HIRATE_DATA_VALID ITY	DU2 hirate data validity.	UUU2114S	UINT8
DCT_UNIT2_HK_HI_RT_DU2_HR_RUN_ID	DU2 hr run id.	UUU0005N	UINT32
DCT_UNIT2_HK_HI_RT_DU2_HR_OBT_SECONDS	DU2 hr obt seconds.	UUU2118H	UINT32
DCT_UNIT2_HK_HI_RT_DU2_HR_OBT_MICROSEC ONDS	DU2 hr obt microseconds.	UUU2119H	UINT32
DCT_UNIT2_HK_HI_RT_DU2_HR_OBT_ERROR	DU2 hr obt error.	UUU2120H	INT32
DCT_UNIT2_HK_HI_RT_DU2_VREF_XPOL	DU2 vref xpol BEE register.	UUU2005U	UINT16
DCT_UNIT2_HK_HI_RT_DU2_CURRENT_5_V	DU2 current 5v BEE register.	UUU2006I	UINT16

DCT_UNIT2_HK_HI_RT_DU2_CURRENT_3_V3	DU2 current 3v3 BEE register.	UUU2007I	UINT16
DCT_UNIT2_HK_HI_RT_DU2_CURRENT_1_V8	DU2 current 1v8 BEE register.	UUU2008I	UINT16
DCT_UNIT2_HK_HI_RT_DU2_TEMP_LVPS_1_V5	DU2 temp lvps 1v5 BEE register.	UUU2009T	UINT16
DCT_UNIT2_HK_HI_RT_DU2_TEMP_LVPS_1_V8	DU2 temp lvps 1v8 BEE register.	UUU2010T	UINT16
DCT_UNIT2_HK_HI_RT_DU2_TEMP_LVPS_3_V3	DU2 temp lvps 3v3 BEE register.	UUU2012T	UINT16
DCT_UNIT2_HK_HI_RT_DU2_TEMP_HV_1	DU2 temp hv 1 BEE register.	UUU2013T	UINT16
DCT_UNIT2_HK_HI_RT_DU2_TEMP_HV_2	DU2 temp hv 2 BEE register.	UUU2014T	UINT16
DCT_UNIT2_HK_HI_RT_DU2_CURRENT_HV_1	DU2 current hv 1 BEE register.	UUU2015I	UINT16
DCT_UNIT2_HK_HI_RT_DU2_CURRENT_HV_2	DU2 current hv 2 BEE register.	UUU2016I	UINT16
DCT_UNIT2_HK_HI_RT_DU2_TEMP_GPD	DU2 temp gpd BEE register.	UUU2018T	UINT16
DCT_UNIT2_HK_HI_RT_DU2_TEMP_DAQ_1	DU2 temp daq 1 BEE register.	UUU2019T	UINT16
DCT_UNIT2_HK_HI_RT_DU2_TEMP_DAQ_2	DU2 temp daq 2 BEE register.	UUU2020T	UINT16
DCT_UNIT2_HK_HI_RT_DU2_CURRENT_1_V5	DU2 current 1v5 BEE register.	UUU2023I	UINT16
DCT_UNIT2_HK_HI_RT_DU2_VOLTAGE_HV_DRIFT	DU2 voltage hv drift BEE register.	UUU2024U	UINT16
DCT_UNIT2_HK_HI_RT_DU2_VOLTAGE_HV_TOP	DU2 voltage hv top BEE register.	UUU2025U	UINT16
DCT_UNIT2_HK_HI_RT_DU2_VOLTAGE_HV_BOT	DU2 voltage hv bot BEE register.	UUU2026U	UINT16
DCT_UNIT2_HK_HI_RT_DU2_CURRENT_HV_3	DU2 current hv 3 BEE register.	UUU2027I	UINT16
DCT_UNIT2_HK_HI_RT_DU2_XPOL_RO_STATUS	DU2 xpol ro status BEE register.	UUU2037S	UINT16
DCT_UNIT2_HK_HI_RT_DU2_EVT_COUNTER_LSW	DU2 evt counter lsw BEE register.	UUU2046S	UINT16

DCT_UNIT2_HK_HI_RT_DU2_EVT_COUNTER_MSW	DU2 evt counter msw BEE register.	UUU2047S	UINT16
DCT_UNIT2_HK_HI_RT_DU2_WULIM_REJ_CNT_LS W	DU2 wulim rej cnt lsw BEE register.	UUU2048S	UINT16
DCT_UNIT2_HK_HI_RT_DU2_WLLIM_REJ_CNT_LS W	DU2 wllim rej cnt lsw BEE register.	UUU2050S	UINT16
DCT_UNIT2_HK_HI_RT_DU2_PPS_COUNTER_LSW	DU2 pps counter lsw BEE register.	UUU2064S	UINT16
DCT_UNIT2_HK_HI_RT_DU2_PPS_COUNTER_MSW	DU2 pps counter msw BEE register.	UUU2065S	UINT16
DCT_UNIT2_HK_HI_RT_DU2_USEC_COUNTER_LS W	DU2 usec counter lsw BEE register.	UUU2066S	UINT16
DCT_UNIT2_HK_HI_RT_DU2_USEC_COUNTER_MS W	DU2 usec counter msw BEE register.	UUU2067S	UINT16
DCT_UNIT2_HK_HI_RT_DU2_OBT_ERROR	DU2 obt error BEE register.	UUU2068S	INT16
DCT_UNIT2_HK_HI_RT_DU2_BEE_STATUS	DU2 bee status BEE register.	UUU2080S	UINT16
DCT_UNIT2_HK_HI_RT_DU2_HK_LIVE_TIME_LSB	DU2 hk live time lsb BEE register.	UUU2095S	UINT16
DCT_UNIT2_HK_HI_RT_DU2_HK_LIVE_TIME_MSB	DU2 hk live time msb BEE register.	UUU2096S	UINT16
DCT_UNIT2_HK_HI_RT_DU2_COUNTER_END_RO_ LSW	DU2 counter end ro lsw BEE register.	UUU2111S	UINT16
DCT_UNIT2_HK_HI_RT_DU2_COUNTER_END_RO_ MSW	DU2 counter end ro msw BEE register.	UUU2112S	UINT16
DCT_UNIT3_HK_HI_RT_DU3_HIRATE_DATA_VALID ITY	DU3 hirate data validity.	UUU3114S	UINT8
DCT_UNIT3_HK_HI_RT_DU3_HR_RUN_ID	DU3 run id.	UUU0006N	UINT32
DCT_UNIT3_HK_HI_RT_DU3_HR_OBT_SECONDS	DU3 hr obt seconds.	UUU3118H	UINT32
DCT_UNIT3_HK_HI_RT_DU3_HR_OBT_MICROSEC ONDS	DU3 hr obt microseconds.	UUU3119H	UINT32
DCT_UNIT3_HK_HI_RT_DU3_HR_OBT_ERROR	DU3 hr obt error.	UUU3120H	INT32
DCT_UNIT3_HK_HI_RT_DU3_VREF_XPOL	DU3 vref xpol BEE register.	UUU3005U	UINT16
DCT_UNIT3_HK_HI_RT_DU3_CURRENT_5_V	DU3 current 5v BEE register.	UUU3006I	UINT16
DCT_UNIT3_HK_HI_RT_DU3_CURRENT_3_V3	DU3 current 3v3 BEE register.	UUU3007I	UINT16

DCT_UNIT3_HK_HI_RT_DU3_CURRENT_1_V8	DU3 current 1v8 BEE register.	UUU3008I	UINT16
DCT_UNIT3_HK_HI_RT_DU3_TEMP_LVPS_1_V5	DU3 temp lvps 1v5 BEE register.	UUU3009T	UINT16
DCT_UNIT3_HK_HI_RT_DU3_TEMP_LVPS_1_V8	DU3 temp lvps 1v8 BEE register.	UUU3010T	UINT16
DCT_UNIT3_HK_HI_RT_DU3_TEMP_LVPS_3_V3	DU3 temp lvps 3v3 BEE register.	UUU3012T	UINT16
DCT_UNIT3_HK_HI_RT_DU3_TEMP_HV_1	DU3 temp hv 1 BEE register.	UUU3013T	UINT16
DCT_UNIT3_HK_HI_RT_DU3_TEMP_HV_2	DU3 temp hv 2 BEE register.	UUU3014T	UINT16
DCT_UNIT3_HK_HI_RT_DU3_CURRENT_HV_1	DU3 current hv 1 BEE register.	UUU3015I	UINT16
DCT_UNIT3_HK_HI_RT_DU3_CURRENT_HV_2	DU3 current hv 2 BEE register.	UUU3016I	UINT16
DCT_UNIT3_HK_HI_RT_DU3_TEMP_GPD	DU3 temp gpd BEE register.	UUU3018T	UINT16
DCT_UNIT3_HK_HI_RT_DU3_TEMP_DAQ_1	DU3 temp daq 1 BEE register.	UUU3019T	UINT16
DCT_UNIT3_HK_HI_RT_DU3_TEMP_DAQ_2	DU3 temp daq 2 BEE register.	UUU3020T	UINT16
DCT_UNIT3_HK_HI_RT_DU3_CURRENT_1_V5	DU3 current 1v5 BEE register.	UUU3023I	UINT16
DCT_UNIT3_HK_HI_RT_DU3_VOLTAGE_HV_DRIFT	DU3 voltage hv drift BEE register.	UUU3024U	UINT16
DCT_UNIT3_HK_HI_RT_DU3_VOLTAGE_HV_TOP	DU3 voltage hv top BEE register.	UUU3025U	UINT16
DCT_UNIT3_HK_HI_RT_DU3_VOLTAGE_HV_BOT	DU3 voltage hv bot BEE register.	UUU3026U	UINT16
DCT_UNIT3_HK_HI_RT_DU3_CURRENT_HV_3	DU3 current hv 3 BEE register.	UUU3027I	UINT16
DCT_UNIT3_HK_HI_RT_DU3_XPOL_RO_STATUS	DU3 xpol ro status BEE register.	UUU3037S	UINT16
DCT_UNIT3_HK_HI_RT_DU3_EVT_COUNTER_LSW	DU3 evt counter lsw BEE register.	UUU3046S	UINT16
DCT_UNIT3_HK_HI_RT_DU3_EVT_COUNTER_MSW	DU3 evt counter msw BEE register.	UUU3047S	UINT16

DCT_UNIT3_HK_HI_RT_DU3_WULIM_REJ_CNT_LS W	DU3 wulim rej cnt lsw BEE register.	UUU3048S	UINT16
DCT_UNIT3_HK_HI_RT_DU3_WLLIM_REJ_CNT_LS W	DU3 wllim rej cnt lsw BEE register.	UUU3050S	UINT16
DCT_UNIT3_HK_HI_RT_DU3_PPS_COUNTER_LSW	DU3 pps counter lsw BEE register.	UUU3064S	UINT16
DCT_UNIT3_HK_HI_RT_DU3_PPS_COUNTER_MSW	DU3 pps counter msw BEE register.	UUU3065S	UINT16
DCT_UNIT3_HK_HI_RT_DU3_USEC_COUNTER_LS W	DU3 usec counter lsw BEE register.	UUU3066S	UINT16
DCT_UNIT3_HK_HI_RT_DU3_USEC_COUNTER_MS W	DU3 usec counter msw BEE register.	UUU3067S	UINT16
DCT_UNIT3_HK_HI_RT_DU3_OBT_ERROR	DU3 obt error BEE register.	UUU3068S	INT16
DCT_UNIT3_HK_HI_RT_DU3_BEE_STATUS	DU3 bee status BEE register.	UUU3080S	UINT16
DCT_UNIT3_HK_HI_RT_DU3_HK_LIVE_TIME_LSB	DU3 hk live time lsb BEE register.	UUU3095S	UINT16
DCT_UNIT3_HK_HI_RT_DU3_HK_LIVE_TIME_MSB	DU3 hk live time msb BEE register.	UUU3096S	UINT16
DCT_UNIT3_HK_HI_RT_DU3_COUNTER_END_RO_ LSW	DU3 counter end ro lsw BEE register.	UUU3111S	UINT16
DCT_UNIT3_HK_HI_RT_DU3_COUNTER_END_RO_ MSW	DU3 counter end ro msw BEE register.	UUU3112S	UINT16
FDIR_MNGR_FDIR_0_RESULT	FDIR 0 RESULT result.	DDD1400X	UINT8
FDIR_MNGR_FDIR_1_RESULT	FDIR 1 RESULT result.	DDD1401X	UINT8
FDIR_MNGR_FDIR_2_RESULT	FDIR 2 RESULT result.	DDD1402X	UINT8
FDIR_MNGR_FDIR_3_RESULT	FDIR 3 RESULT result.	DDD1403X	UINT8
FDIR_MNGR_FDIR_4_RESULT	FDIR 4 RESULT result.	DDD1404X	UINT8
FDIR_MNGR_FDIR_5_RESULT	FDIR 5 RESULT result.	DDD1405X	UINT8
FDIR_MNGR_FDIR_6_RESULT	FDIR 6 RESULT result.	DDD1406X	UINT8
FDIR_MNGR_FDIR_7_RESULT	FDIR 7 RESULT result.	DDD1407X	UINT8
FDIR_MNGR_FDIR_8_RESULT	FDIR 8 RESULT result.	DDD1408X	UINT8
FDIR_MNGR_FDIR_9_RESULT	FDIR 9 RESULT result.	DDD1409X	UINT8
FDIR_MNGR_FDIR_10_RESULT	FDIR 10 RESULT result.	DDD1410X	UINT8
FDIR_MNGR_FDIR_11_RESULT	FDIR 11 RESULT result.	DDD1411X	UINT8
FDIR_MNGR_FDIR_12_RESULT	FDIR 12 RESULT result.	DDD1412X	UINT8

FDIR_MNGR_FDIR_13_RESULT	FDIR 13 RESULT result.	DDD1413X	UINT8
FDIR_MNGR_FDIR_14_RESULT	FDIR 14 RESULT result.	DDD1414X	UINT8
FDIR_MNGR_FDIR_15_RESULT	FDIR 15 RESULT result.	DDD1415X	UINT8
FDIR_MNGR_FDIR_16_RESULT	FDIR 16 RESULT result.	DDD1416X	UINT8
FDIR_MNGR_FDIR_17_RESULT	FDIR 17 RESULT result.	DDD1417X	UINT8
FDIR_MNGR_FDIR_18_RESULT	FDIR 18 RESULT result.	DDD1418X	UINT8
FDIR_MNGR_FDIR_19_RESULT	FDIR 19 RESULT result.	DDD1419X	UINT8
FDIR_MNGR_FDIR_20_RESULT	FDIR 20 RESULT result.	DDD1420X	UINT8
FDIR_MNGR_FDIR_21_RESULT	FDIR 21 RESULT result.	DDD1421X	UINT8
FDIR_MNGR_FDIR_22_RESULT	FDIR 22 RESULT result.	DDD1422X	UINT8
FDIR_MNGR_FDIR_23_RESULT	FDIR 23 RESULT result.	DDD1423X	UINT8
FDIR_MNGR_FDIR_24_RESULT	FDIR 24 RESULT result.	DDD1424X	UINT8
FDIR_MNGR_FDIR_25_RESULT	FDIR 25 RESULT result.	DDD1425X	UINT8
FDIR_MNGR_FDIR_26_RESULT	FDIR 26 RESULT result.	DDD1426X	UINT8
FDIR_MNGR_FDIR_27_RESULT	FDIR 27 RESULT result.	DDD1427X	UINT8
FDIR_MNGR_FDIR_28_RESULT	FDIR 28 RESULT result.	DDD1428X	UINT8
FDIR_MNGR_FDIR_29_RESULT	FDIR 29 RESULT result.	DDD1429X	UINT8
FDIR_MNGR_FDIR_30_RESULT	FDIR 30 RESULT result.	DDD1430X	UINT8
FDIR_MNGR_FDIR_31_RESULT	FDIR 31 RESULT result.	DDD1431X	UINT8
FDIR_MNGR_FDIR_32_RESULT	FDIR 32 RESULT result.	DDD1432X	UINT8
FDIR_MNGR_FDIR_33_RESULT	FDIR 33 RESULT result.	DDD1433X	UINT8
FDIR_MNGR_FDIR_34_RESULT	FDIR 34 RESULT result.	DDD1434X	UINT8
FDIR_MNGR_FDIR_35_RESULT	FDIR 35 RESULT result.	DDD1435X	UINT8
FDIR_MNGR_FDIR_36_RESULT	FDIR 36 RESULT result.	DDD1436X	UINT8
FDIR_MNGR_FDIR_37_RESULT	FDIR 37 RESULT result.	DDD1437X	UINT8
FDIR_MNGR_FDIR_38_RESULT	FDIR 38 RESULT result.	DDD1438X	UINT8
FDIR_MNGR_FDIR_39_RESULT	FDIR 39 RESULT result.	DDD1439X	UINT8
FDIR_MNGR_FDIR_40_RESULT	FDIR 40 RESULT result.	DDD1440X	UINT8
FDIR_MNGR_FDIR_41_RESULT	FDIR 41 RESULT result.	DDD1441X	UINT8
FDIR_MNGR_FDIR_42_RESULT	FDIR 42 RESULT result.	DDD1442X	UINT8
FDIR_MNGR_FDIR_43_RESULT	FDIR 43 RESULT result.	DDD1443X	UINT8
FDIR_MNGR_FDIR_44_RESULT	FDIR 44 RESULT result.	DDD1444X	UINT8

FDIR_MNGR_FDIR_45_RESULT	FDIR 45 RESULT result.	DDD1445X	UINT8
FDIR_MNGR_FDIR_46_RESULT	FDIR 46 RESULT result.	DDD1446X	UINT8
FDIR_MNGR_FDIR_47_RESULT	FDIR 47 RESULT result.	DDD1447X	UINT8
FDIR_MNGR_FDIR_48_RESULT	FDIR 48 RESULT result.	DDD1448X	UINT8
FDIR_MNGR_FDIR_49_RESULT	FDIR 49 RESULT result.	DDD1449X	UINT8
FDIR_MNGR_FDIR_50_RESULT	FDIR 50 RESULT result.	DDD1450X	UINT8
FDIR_MNGR_FDIR_51_RESULT	FDIR 51 RESULT result.	DDD1451X	UINT8
FDIR_MNGR_FDIR_52_RESULT	FDIR 52 RESULT result.	DDD1452X	UINT8
FDIR_MNGR_FDIR_53_RESULT	FDIR 53 RESULT result.	DDD1453X	UINT8
FDIR_MNGR_FDIR_54_RESULT	FDIR 54 RESULT result.	DDD1454X	UINT8
FDIR_MNGR_FDIR_55_RESULT	FDIR 55 RESULT result.	DDD1455X	UINT8
FDIR_MNGR_FDIR_56_RESULT	FDIR 56 RESULT result.	DDD1456X	UINT8
FDIR_MNGR_FDIR_57_RESULT	FDIR 57 RESULT result.	DDD1457X	UINT8
FDIR_MNGR_FDIR_58_RESULT	FDIR 58 RESULT result.	DDD1458X	UINT8
FDIR_MNGR_FDIR_59_RESULT	FDIR 59 RESULT result.	DDD1459X	UINT8
FDIR_MNGR_FDIR_60_RESULT	FDIR 60 RESULT result.	DDD1460X	UINT8
FDIR_MNGR_FDIR_61_RESULT	FDIR 61 RESULT result.	DDD1461X	UINT8
FDIR_MNGR_FDIR_62_RESULT	FDIR 62 RESULT result.	DDD1462X	UINT8
FDIR_MNGR_FDIR_63_RESULT	FDIR 63 RESULT result.	DDD1463X	UINT8
FDIR_MNGR_FDIR_64_RESULT	FDIR 64 RESULT result.	DDD1464X	UINT8
FDIR_MNGR_FDIR_65_RESULT	FDIR 65 RESULT result.	DDD1465X	UINT8
FDIR_MNGR_FDIR_66_RESULT	FDIR 66 RESULT result.	DDD1466X	UINT8
FDIR_MNGR_FDIR_67_RESULT	FDIR 67 RESULT result.	DDD1467X	UINT8
FDIR_MNGR_FDIR_68_RESULT	FDIR 68 RESULT result.	DDD1468X	UINT8
FDIR_MNGR_FDIR_69_RESULT	FDIR 69 RESULT result.	DDD1469X	UINT8
FDIR_MNGR_FDIR_70_RESULT	FDIR 70 RESULT result.	DDD1470X	UINT8
FDIR_MNGR_FDIR_71_RESULT	FDIR 71 RESULT result.	DDD1471X	UINT8
FDIR_MNGR_FDIR_72_RESULT	FDIR 72 RESULT result.	DDD1472X	UINT8
FDIR_MNGR_FDIR_73_RESULT	FDIR 73 RESULT result.	DDD1473X	UINT8
FDIR_MNGR_FDIR_74_RESULT	FDIR 74 RESULT result.	DDD1474X	UINT8
FDIR_MNGR_FDIR_75_RESULT	FDIR 75 RESULT result.	DDD1475X	UINT8
FDIR_MNGR_FDIR_76_RESULT	FDIR 76 RESULT result.	DDD1476X	UINT8

FDIR_MNGR_FDIR_77_RESULT	FDIR 77 RESULT result.	DDD1477X	UINT8
FDIR_MNGR_FDIR_78_RESULT	FDIR 78 RESULT result.	DDD1478X	UINT8
FDIR_MNGR_FDIR_79_RESULT	FDIR 79 RESULT result.	DDD1479X	UINT8
FDIR_MNGR_FDIR_80_RESULT	FDIR 80 RESULT result.	DDD1480X	UINT8
FDIR_MNGR_FDIR_81_RESULT	FDIR 81 RESULT result.	DDD1481X	UINT8
FDIR_MNGR_FDIR_82_RESULT	FDIR 82 RESULT result.	DDD1482X	UINT8
FDIR_MNGR_FDIR_83_RESULT	FDIR 83 RESULT result.	DDD1483X	UINT8
FDIR_MNGR_FDIR_84_RESULT	FDIR 84 RESULT result.	DDD1484X	UINT8
FDIR_MNGR_FDIR_85_RESULT	FDIR 85 RESULT result.	DDD1485X	UINT8
FDIR_MNGR_FDIR_86_RESULT	FDIR 86 RESULT result.	DDD1486X	UINT8
FDIR_MNGR_FDIR_87_RESULT	FDIR 87 RESULT result.	DDD1487X	UINT8
FDIR_MNGR_FDIR_88_RESULT	FDIR 88 RESULT result.	DDD1488X	UINT8
FDIR_MNGR_FDIR_89_RESULT	FDIR 89 RESULT result.	DDD1489X	UINT8
FDIR_MNGR_FDIR_90_RESULT	FDIR 90 RESULT result.	DDD1490X	UINT8
FDIR_MNGR_FDIR_91_RESULT	FDIR 91 RESULT result.	DDD1491X	UINT8
FDIR_MNGR_FDIR_92_RESULT	FDIR 92 RESULT result.	DDD1492X	UINT8
FDIR_MNGR_FDIR_93_RESULT	FDIR 93 RESULT result.	DDD1493X	UINT8
FDIR_MNGR_FDIR_94_RESULT	FDIR 94 RESULT result.	DDD1494X	UINT8
FDIR_MNGR_FDIR_95_RESULT	FDIR 95 RESULT result.	DDD1495X	UINT8
FDIR_MNGR_FDIR_96_RESULT	FDIR 96 RESULT result.	DDD1496X	UINT8
FDIR_MNGR_FDIR_97_RESULT	FDIR 97 RESULT result.	DDD1497X	UINT8
FDIR_MNGR_FDIR_98_RESULT	FDIR 98 RESULT result.	DDD1498X	UINT8
FDIR_MNGR_FDIR_99_RESULT	FDIR 99 RESULT result.	DDD1499X	UINT8
FDIR_MNGR_FDIR_100_RESULT	FDIR 100 RESULT result.	DDD1500X	UINT8
FDIR_MNGR_FDIR_101_RESULT	FDIR 101 RESULT result.	DDD1501X	UINT8
FDIR_MNGR_FDIR_102_RESULT	FDIR 102 RESULT result.	DDD1502X	UINT8
FDIR_MNGR_FDIR_103_RESULT	FDIR 103 RESULT result.	DDD1503X	UINT8
FDIR_MNGR_FDIR_104_RESULT	FDIR 104 RESULT result.	DDD1504X	UINT8
FDIR_MNGR_FDIR_105_RESULT	FDIR 105 RESULT result.	DDD1505X	UINT8
FDIR_MNGR_FDIR_106_RESULT	FDIR 106 RESULT result.	DDD1506X	UINT8
FDIR_MNGR_FDIR_107_RESULT	FDIR 107 RESULT result.	DDD1507X	UINT8
FDIR_MNGR_FDIR_108_RESULT	FDIR 108 RESULT result.	DDD1508X	UINT8

FDIR_MNGR_FDIR_109_RESULT	FDIR 109 RESULT result.	DDD1509X	UINT8
FDIR_MNGR_FDIR_110_RESULT	FDIR 110 RESULT result.	DDD1510X	UINT8
FDIR_MNGR_FDIR_111_RESULT	FDIR 111 RESULT result.	DDD1511X	UINT8
FDIR_MNGR_FDIR_112_RESULT	FDIR 112 RESULT result.	DDD1512X	UINT8
FDIR_MNGR_FDIR_113_RESULT	FDIR 113 RESULT result.	DDD1513X	UINT8
FDIR_MNGR_FDIR_114_RESULT	FDIR 114 RESULT result.	DDD1514X	UINT8
FDIR_MNGR_FDIR_115_RESULT	FDIR 115 RESULT result.	DDD1515X	UINT8
FDIR_MNGR_FDIR_116_RESULT	FDIR 116 RESULT result.	DDD1516X	UINT8
FDIR_MNGR_FDIR_117_RESULT	FDIR 117 RESULT result.	DDD1517X	UINT8
FDIR_MNGR_FDIR_118_RESULT	FDIR 118 RESULT result.	DDD1518X	UINT8
FDIR_MNGR_FDIR_119_RESULT	FDIR 119 RESULT result.	DDD1519X	UINT8
FDIR_MNGR_FDIR_120_RESULT	FDIR 120 RESULT result.	DDD1520X	UINT8
FDIR_MNGR_FDIR_121_RESULT	FDIR 121 RESULT result.	DDD1521X	UINT8
FDIR_MNGR_FDIR_122_RESULT	FDIR 122 RESULT result.	DDD1522X	UINT8
FDIR_MNGR_FDIR_123_RESULT	FDIR 123 RESULT result.	DDD1523X	UINT8
FDIR_MNGR_FDIR_124_RESULT	FDIR 124 RESULT result.	DDD1524X	UINT8
FDIR_MNGR_FDIR_125_RESULT	FDIR 125 RESULT result.	DDD1525X	UINT8
FDIR_MNGR_FDIR_126_RESULT	FDIR 126 RESULT result.	DDD1526X	UINT8
FDIR_MNGR_FDIR_127_RESULT	**FDIR 127 RESULT result.**	**DDD1527X**	UINT8

C.2 SW Software Patch Procedure

The following procedure applies both to a complete SW image upload and to a SW patch: the difference is that in the first case the provided image will be complete, while in the latter only the part of the image to be updated is provided.

In both cases, together with the image or the patch, all parameters depending on the patch and all the required CRCs will be provided.

ASW Patch Procedure				
STEP	**N°**	**TC**	**TLM RESPONSE**	**Remarks**
	100			Verify that the DUs are OFF, HVBs are OFF and FCWs are in CLOSE position.
Enter Maintenance Mode	110	tcsend DDD11041	Successful Command Acceptance Report generated (TM APID 1210) Successful Command Execution Report generated (TM APID 1214) Opmode Successful Change Report (TM APID 1230) Verify in the telemetry APID 1200 (DSU HK): DDD0121S [CURRENT OP MODE] = MAINTENANCE	
Patch Memory to Activate SafePD Mode After Reboot	120	tcsend DDD11020 {DDD0043S UT699FT_MRAM} {DDD0002X 0x107FFFB0} {DDD0003X 16} {DDD0004X 0x4040000000000100000000100000DCB5}	Successful Command Acceptance Report generated (TM APID 1210)	Nominal Boot Information Table address: 0x107FFFB0

			Successful Command Execution Report generated (TM APID 1214)	Redundant Boot Information Table address: 0x107FFFD8
	125	tcsend DDD11020 {DDD0043S UT699FT_MRAM} {DDD0002X 0x107FFFD8} {DDD0003X 16} {DDD0004X 0x4040000000000100000000100000DCB5}	Successful Command Acceptance Report generated (TM APID 1210) Successful Command Execution Report generated (TM APID 1214)	SW image to load = SafePD (0x00000010) See I2C-OHBI-IOP-TEC-003 – IXPE Software User manual for details
Enter Safe Mode	130	tcsend DDD11044	Successful Command Acceptance Report generated (TM APID 1210) Successful Command Execution Report generated (TM APID 1214) Opmode Successful Change Report (TM APID 1230) Verify in the telemetry APID 1200 (DSU HK): DDD0121S [CURRENT OP MODE] = SAFE	
Reboot	140	tcsend DDD11045	Verify the telemetry APID 1220 (Boot SW Report) is generated The periodic telemetry TM(3,25) APID 1202 is generated every 10 seconds	
Upload New ASW Boot Segment Image	150	Send a list of TCs APID 1020 until the complete image is uploaded. The maximum length of the data to be uploaded (parameter DDD0004X) with a single TC is 988 bytes. tcsend DDD11020 {DDD0043S UT699FT_MRAM} {DDD0002X <mem_address>} {DDD0003X <data_length>} {DDD0004X <asw_data>}	Successful Command Acceptance Report generated (TM APID 1210)	ASW Boot Segment Image A starts at address 0x10000000 ASW Boot Segment Image B starts at address 0x10180000

		[…] […]	Successful Command Execution Report generated (TM APID 1214) […] […] […] […]	<mem_address> from ASW Boot Segment Image SREC file content (incremented by <data_length> of previous TC at each TC sending <data_length> depending on <asw_data>, maximum value per TC 988 <asw_data> from ASW Boot Segment Image SREC file content
Check ASW Boot Segment Image Memory	160	tcsend DDD11022 {DDD0001S UT699FT_MRAM} {DDD0002X <mem_address>} {DDD0003X <asw_length>}	Check DSU Memory Report (APID 1261) Verify the CRC result with the value provided at ASW Boot Segment Image delivery	<mem_address> from ASW Boot Segment Image SREC file content (start address of ASW Boot Segment Image, see remarks of previous step) <asw_length> total length of uploaded ASW Boot Segment Image
Update Boot Application Descriptor Tables	170	tcsend DDD11020 {DDD0043S UT699FT_MRAM} {DDD0002X 0x107FFFC0} {DDD0003X 12} {DDD0004X 0x40000000100000000000089A7} tcsend DDD11020 {DDD0043S UT699FT_MRAM} {DDD0002X 0x107FFFE8} {DDD0003X 12} {DDD0004X 0x40000000100000000000089A7}	Successful Command Acceptance Report generated (TM APID 1210) Successful Command Execution Report generated (TM APID 1214) Successful Command Acceptance Report generated (TM APID 1210)	**NOTE:** This step can safely be skipped if Boot Application Descriptor Tables are not affected by the uploaded ASW Boot Segment Image. This information will be provided with the ASW

			Successful Command Execution Report generated (TM APID 1214)	Boot Segment Image with correct TC parameters if required. Nominal Boot Application Descriptor Table address image A: 0x107FFFC0 Redundant Boot Application Descriptor Table address image A: 0x107FFFE8 Nominal Boot Application Descriptor Table address image B: 0x107FFFCC Redundant Boot Application Descriptor Table address image B: 0x107FFFF4 See I2C-OHBI-IOP-TEC-003 – IXPE Software User manual for details
	175	tcsend DDD11020 {DDD0043S UT699FT_MRAM} {DDD0002X 0x107FFFCC} {DDD0003X 12} {DDD0004X 0x0x40000000101800000008FD0} tcsend DDD11020 {DDD0043S UT699FT_MRAM} {DDD0002X 0x107FFFF4} {DDD0003X 12} {DDD0004X 0x0x40000000101800000008FD0}	Successful Command Acceptance Report generated (TM APID 1210) Successful Command Execution Report generated (TM APID 1214) Successful Command Acceptance Report generated (TM APID 1210) Successful Command Execution Report generated (TM APID 1214)	
Copy New ASW Image to SRAM	180	tcsend DDD11080 {DDD1001S <image_id>}	Successful Command Acceptance Report generated (TM APID 1210) Successful Command Execution Report generated (TM APID 1214)	<image_id> = ASW_IMAGE_A or ASW_IMAGE_B, depending on the uploaded ASW Boot Segment Image
Check Loaded ASW Image Memory	190	tcsend DDD11022 {DDD0001S UT699FT_SRAM} {DDD0002X 0x40000000} {DDD0003X <length>}	Check DSU Memory Report (APID 1261)	<length> = size of ASW Image, provided at image delivery

			Verify the CRC result with the value provided at ASW Image delivery	
Start ASW	200	tcsend DDD11081 {DDD1002X 0x40000000}	Verify the telemetry APID 1220 (Boot SW Report) is generated Verify in the telemetry APID 1220 (Boot SW Report): • DDD1063S [ASW_B_TEST_R] = 0 • DDD1064S [ASW_A_TEST_R] = 0 • DDD1065S [INTERRUPT_TEST_R] = 0 • DDD1066S [EDAC_TEST_R] = 0 • DDD1067S [SRAM_TEST_R] = 0 • DDD1068S [INFO_TBL_TEST_R] = 0 • DDD1069S [PROM_TEST_R] = 0 • DDD1070S [CACHE_TEST_R] = 0 • DDD1071S [IU_PARITY_TEST_R] = 0 Verify the telemetry APID 1221 (ASW Start Report) is generated Verify in the telemetry APID 1221 (ASW Start Report) • DDD0660S [INIT OP MODE] = STAND_BY or RECOVERY • DDD0661S [DSU BOARD] =NOMINAL or REDUNDANT	
Enter Maintenance Mode	210	tcsend DDD11041	Successful Command Acceptance Report generated (TM APID 1210)	

			Successful Command Execution Report generated (TM APID 1214) Opmode Successful Change Report (TM APID 1230) Verify in the telemetry APID 1200 (DSU HK): DDD0121S [CURRENT OP MODE] = MAINTENANCE	
Patch Memory to Activate Image A or Image B After Reboot	220	Image A tcsend DDD11020 {DDD0043S UT699FT_MRAM} {DDD0002X 0x107FFFB0} {DDD0003X 16} {DDD0004X 0x4040000000000100000000010000A8E6} tcsend DDD11020 {DDD0043S UT699FT_MRAM} {DDD0002X 0x107FFFD8} {DDD0003X 16} {DDD0004X 0x4040000000000100000000010000A8E6}	Successful Command Acceptance Report generated (TM APID 1210) Successful Command Execution Report generated (TM APID 1214) Successful Command Acceptance Report generated (TM APID 1210) Successful Command Execution Report generated (TM APID 1214)	Nominal Boot Information Table address: 0x107FFFB0 Redundant Boot Information Table address: 0x107FFFD8 SW image to load = Image A (0x00000001) or Image B (0x00000002) See I2C-OHBI-IOP-TEC-003 – IXPE Software User manual for details
	225	Image B tcsend DDD11020 {DDD0043S UT699FT_MRAM} {DDD0002X 0x107FFFB0} {DDD0003X 16} {DDD0004X 0x4040000000000100000000020000F1B6} tcsend DDD11020 {DDD0043S UT699FT_MRAM} {DDD0002X 0x107FFFD8} {DDD0003X 16} {DDD0004X 0x4040000000000100000000020000F1B6}	Successful Command Acceptance Report generated (TM APID 1210) Successful Command Execution Report generated (TM APID 1214) Successful Command Acceptance Report generated (TM APID 1210)	

			Successful Command Execution Report generated (TM APID 1214)	
Enter Safe Mode	230	tcsend DDD11044	Successful Command Acceptance Report generated (TM APID 1210) Successful Command Execution Report generated (TM APID 1214) Opmode Successful Change Report (TM APID 1230) Verify in the telemetry APID 1200 (DSU HK): DDD0121S [CURRENT OP MODE] = SAFE	
Reboot	240	tcsend DDD11045	Verify in the telemetry APID 1220 (Boot SW Report): • DDD1063S [ASW_B_TEST_R] = 0 • DDD1064S [ASW_A_TEST_R] = 0 • DDD1065S [INTERRUPT_TEST_R] = 0 • DDD1066S [EDAC_TEST_R] = 0 • DDD1067S [SRAM_TEST_R] = 0 • DDD1068S [INFO_TBL_TEST_R] = 0 • DDD1069S [PROM_TEST_R] = 0 • DDD1070S [CACHE_TEST_R] = 0 • DDD1071S [IU_PARITY_TEST_R] = 0 Verify the telemetry APID 1221 (ASW Start Report) is generated Verify in the telemetry APID 1221 (ASW Start Report)	

			• DDD0660S [INIT OP MODE] = STAND_BY or RECOVERY • DDD0661S [DSU BOARD] =NOMINAL or REDUNDANT	

8. LIST OF ACRONYMS

ADC	Analog to Digital Converter
AIT	Assembly, Integration and Test
BB	Breadboard
CPU	Central Processing Unit
ECSS	European Cooperation for Space Standardization
EGSE	Electrical Ground Support Equipment
EM	Engineering Model
ELM	Electrical Model Model
ESA	European Space Agency
FDIR	Fault Detection, Isolation and Recovery
FFT	Full Functional Test
FM	Flight Model
GSE	Ground Support Equipment
H/W	Hardware
HK	Housekeeping
IF	Interface
MGSE	Mechanical Ground Support Equipment
MoI	Moment of Inertia
N/A	Not Applicable
OCOE	Overall Checkout Equipment

PA	Product Assurance
PFM	Proto Flight Model
RD-n	Reference Document n
RTDB	Run Time Database
FR	Flight Representative
S/C	Spacecraft
SFT	Short Functional Test
S/W	Software
SMM	Structural Mathematical Model
STM	Structural Thermal Model
TBC	To Be Confirmed
TBD	To Be Defined
TBW	To Be Written
TC	Tele Command
TLM	Telemetry

END OF DOCUMENT