Design and prototyping of the Italian Tile Processor Module 1.5 (ITPM) for the Low-Frequency Aperture Array deployment

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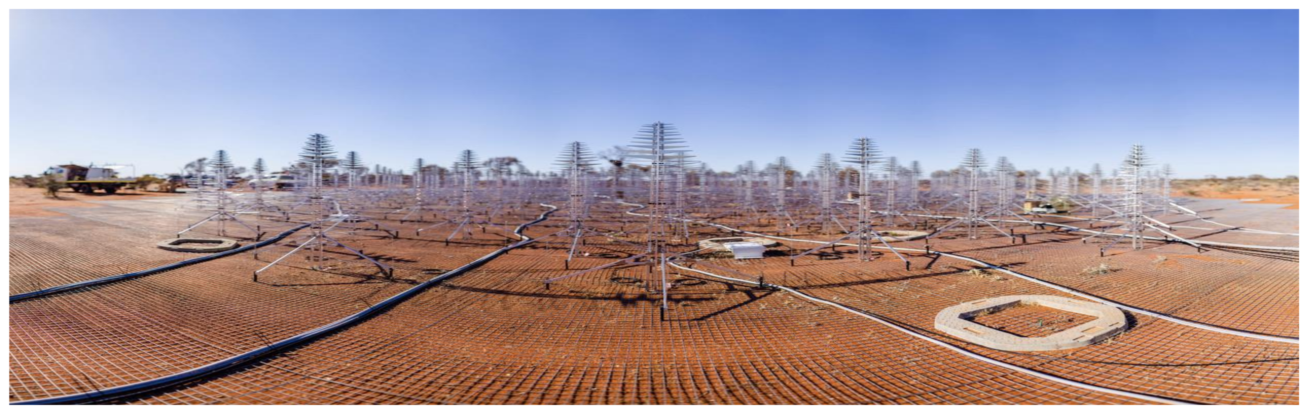
INTRODUCTION

The Square Kilometre Array (SKA) will be the largest and most sensitive radio telescope ever built[1] (Dewdney *et al.*, 2009). It will be constructed in two phases (SKA1 and SKA2)[2], over two sites, South Africa and Western Australia, and at the end of the second phase, it will provide about a million square meters of collecting area through many thousands of connected radio telescopes.
The Low Frequency Aperture Array (LFAA)[3] is the low frequency section of the SKA, it's currently designed to produce 512 of these logical stations to be installed in Australia, which can be flexibly configured by programming the signal processing platform to send its traffic across a highly configurable network.
A single LFAA station is composed of 16 tiles, in each of which 16 antennas are grouped to run their functionalities, first of all the digital beamforming that allows the electrical pointing of the telescope . Each 16 antennas tile is processed in a Tile Processing Module (TPM)[4,5] that is the data processor of each group of antennas, and the core of the digital equipment of the overall LFAA section.
The purpose of this work is to mainly describe the Italian TPM prototype, developed since 2013 together with its digital and mechanical platform within the context of the activities of the Aperture Array Design and Construction Consortium (AADC) of the SKA LFAA and the next SKA Bridging Phase active at the moment, before the phase of construction o radio telescopes.. The project was led by the Italian Istituto Nazionale di Astrofisica (INAF) in collaboration with University of Oxford, Malta University and Science, Technology Facility Council (STFC). and Sanitas EG, an Italian company skilled in digital technologies. After various prototypes realized and successfully tested , the first release of the complete design of ITPM, the ITPM 1.2 version obtained by the assembly two subsystems such an Analog to Digital Unit (ADU) and Pre-ADU boards, was used in 2017 for the Aperture Array Verification System 1 (AAVS1)[6] demonstrator, which include the deployment of 200 antennas at the Murchison Radio-astronomy Observatory, and now deployed for AAVS" and EDA2 demonstrators[30,31].

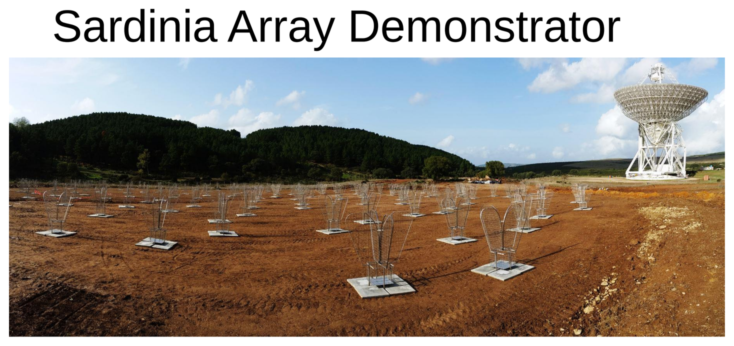
ITPM 1.6 version was adopted as reference design for the Tile Processor Module in 2019 by AADC consortium within the LFAA Critical Design Review process[7].

INAF is getting ready for mass production for the incoming SKA low frequency radio telescope deployment.

AAVS1 (2017) and SKA LFAA



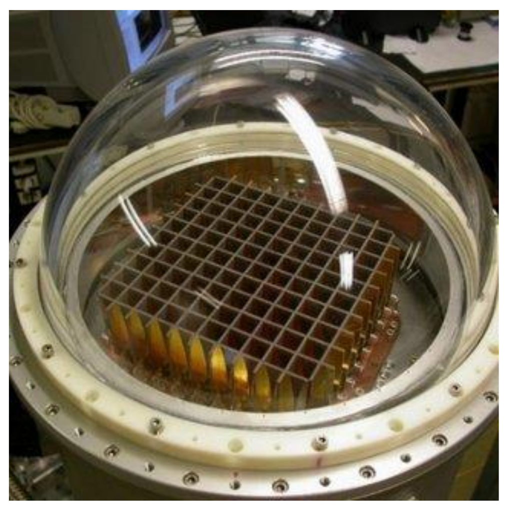
Sardinia Array Demonstrator



Space Debris Application

FRB with Northern Cross - INAF

PHAROS II Back-end



ITPM is engineered as General Purpose Back-end

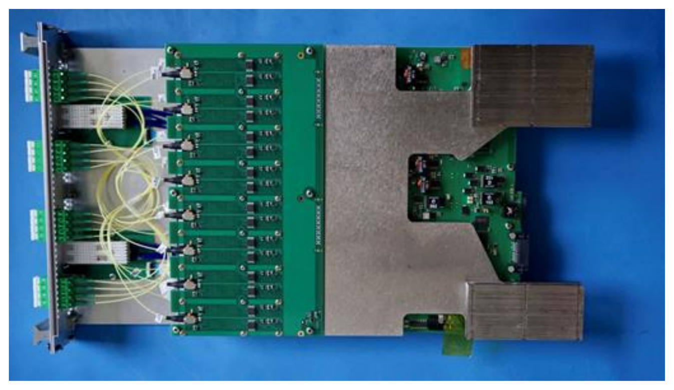
ITPM 1. 6: Upgrades versus previous ITPM 1.2 version

- **New generation FPGAs Xilinx 16 nm Kintex Ultrascale+ devices (**40nm ITPM1.2;
- **ADCs AD9695 ADCs (28 nm)** (AD9680 ITPM 1.2);
- **DDR4 family to improve RAW data buffering** (DDR3L ITPM 1.2);
- **New heat dissipation system;**
- **About 20% of reduction of the absorbed power;**
- **Engineered Subrack including local management functions, power supply, clocks and Ethernet,**

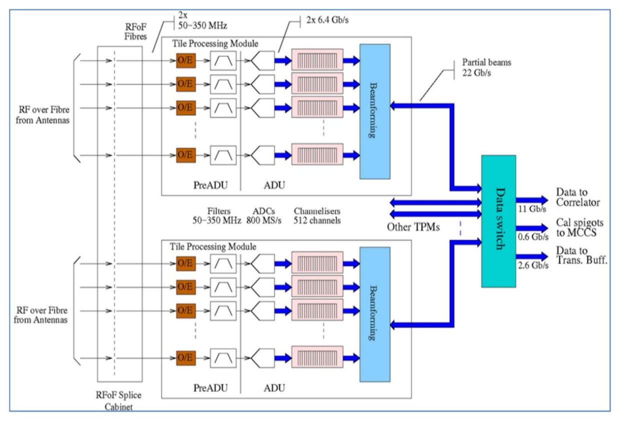
ITPM Architecture

The Italian TPM presented here is mainly composed of two boards: the ADU (Analogue to Digital Unit) board and pre-ADU boards. Pre-ADU boards are devoted to optical-electrical conversion, filtering, amplification and equalization of 32 analogue signals.
The ADU board has the task of: analogue to digital conversion, polyphase filtering, application of calibration and beamforming coefficients, sum of all 32 signals to form the tile beam (local), sum the tile beam with the incoming partial station beam and transmission of the data to the network (switch).

Pre-ADU board corresponds to the analogue receiver in front of the ADU. The current design pre-ADU 2.5 hosts 8 double channel analogue receivers (i.e. 16 analogue chains). The two chains in each double channel receiver correspond to the two antenna polarizations.
The first stage of any pre-ADU channel is an optical receiver (ORX) which converts back to the RF domain the signal transmitted through an optical fibre from the remote antenna. The current pre- ADU version adopts WDM (Wavelength Division Multiplex) optical receivers, which paired with WDM optical RFoF transmitters at the antennas, allows use of one single fibre for both antenna polarizations.
Architecture of the pre-ADU board[16] has simplified the mechanics and interconnection to ADU, but also the RF electronics.



ITPM 1.6 assembly: PRE-ADU (left), ADU (right)



ITPM 1.6 functional view: PRE-ADU (left), ADU (right)

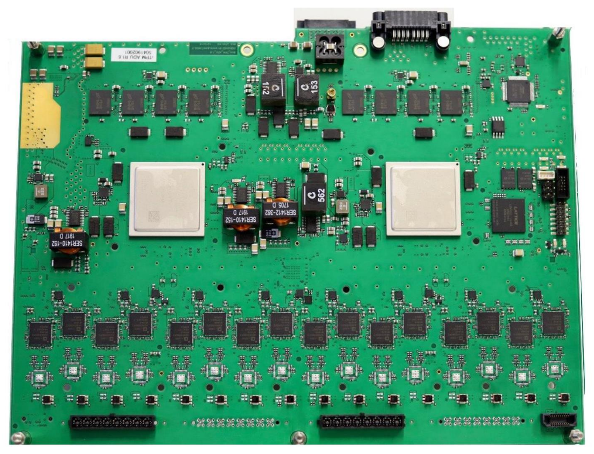
The ITPM ADU processor board is organized in three areas, from left to right as reported in Figure 4: management and power supply, FPGA and memories, analog signal interface. The organization of physical components layout into three separate areas has been adopted to obtain performance and noise isolation between DC-DC converter, digital elements and analog interface.

The **Management Interface** includes the 10/100/1000 data link, the FLASH based CPLD (U1), the Micro Controller Unit & System Monitor (U4), the SPI FLASH memories (U6, U7) and the CPLD external configuration flash, U19.

ITPM ADU **Acquisition Data Path** is organized in four sections: the analog to digital conversion, the data elaboration inside FPGAs, the data buffering in the memory banks, the data communication between FPGAs and the external interface optical link..

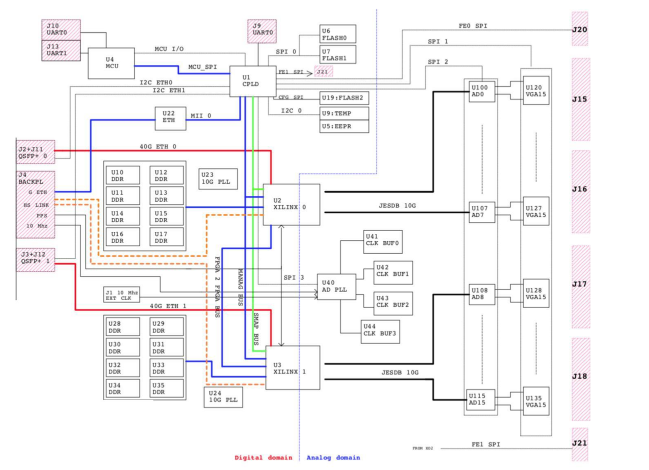
Sixteen lines from the AD can generate up to 16 GByte/s of raw data at maximum sampling frequencies. JESD I/F IP core manages the physical interface and is connected with an internal bus to the data analysis core.

The DDR 64 bit memory interface can perform up to 16GByte read or write operations (800 MHz clock) and can be connected to JESD interface to implement a 128M sample raw buffer. The ITPM FPGA**s** are two identical devices (U2, U3) Xilinx Ultrascale XCKU9P 16 nm, that provide suitable and efficient resources to implement all the main board data management and elaboration. Each FPGA contributes to the System Monitor function.



ITPM 1.6 ADU Board top view

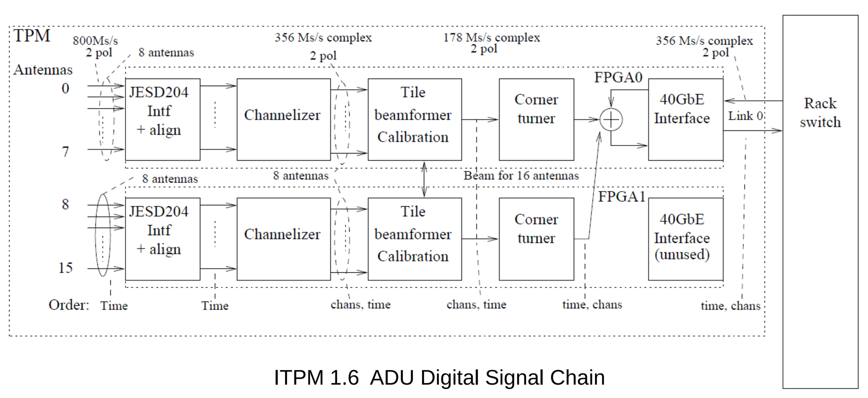
Finally, the **Analog Section** includes the acquisition clock generation and distribution network (U40, U41 – U44), the sixteen dual channel ADCs (U100-U115)AD9695 14 bit 1Ghz, , the sixteen dual channel analog buffers (U120-U135) and the four RF high isolation x8 input connectors (J15-J18). Two connectors (J20 and J21) provide supply and digital SPI control for a pluggable analog board for signal over-fiber connection and physical connection.



ITPM 1.6 ADU Board Schematic

ITPM Firmware

The LFAA station beamformer structure is based on a frequency domain beamforming architecture. Data streams from the individual antennas are channelized with a channel spacing of 781.25 KHz, and delayed in the frequency domain by applying a dynamic phase correction to each individual channel. Each signal is also corrected using a static instrumental gain, phase and polarization calibrations, updated on a timescale of a few minutes. It is possible to select multiple regions in the processed band, and/or to generate multiple beams of the same or different spectral regions. The channelization process is used both to allow for frequency dependent calibration, for frequency domain beamforming, and to provide the first stage of a two-stage channelizer.



ITPM 1.6 ADU Digital Signal Chain

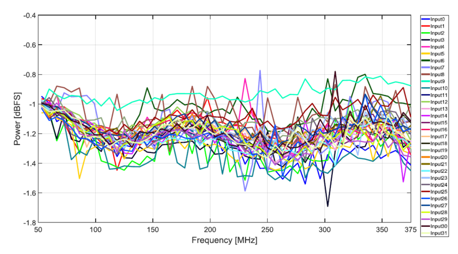
Processing is performed in groups (tiles) of 16 antennas in a TPM. TPMs are connected together in a flexible way using the 40 Gb high speed network, with non-blocking network switches. Stations can then be configured dynamically as arbitrary groups of tiles.

The firmware structure is adapted to a time multiplexed data stream, with 4 samples processed in parallel at each FPGA clock cycle. After channelization and beamforming, odd and even frequency channels for the whole tile beam are processed separately in the two FPGAs. Channelized data is stored in an external local memory, that is used for the corner turner function.

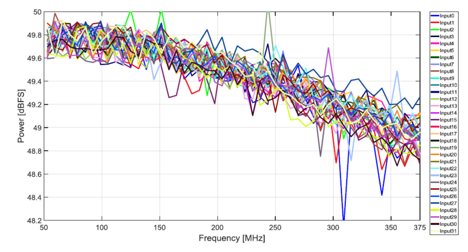
ITPM 1.6 is a digital back-end complete of digital boards, station ITPM housings and Firmware designed for LFAA .

PERFORMANCES

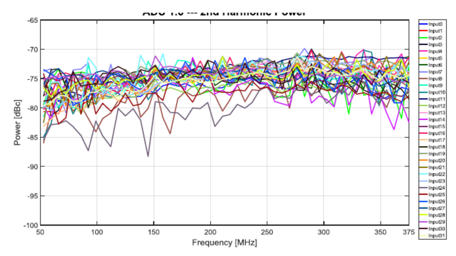
RF tests have been accomplished by using a previously developed method comprising the following steps: to inject a very pure and stable tone into each ADC RF input and acquire it (acquisition sample rate at 800 MSPS) into the buffer memory of the FPGA that captures a block of digital data. Data are then transferred on the server that performs FFT computation and returns a few performance parameters, including among others SNR, SFDR, SINAD, and ENOB for all the 32 input channels. The procedure is repeated for a predefined number of frequencies (typically 50) evenly covering the SKA LFAA bandwidth (50-375MHz).



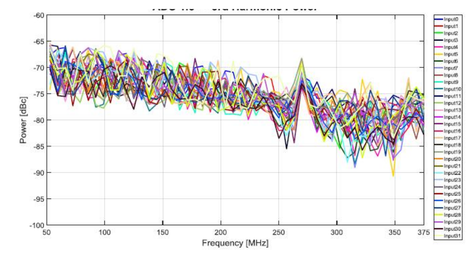
Measured Fundamental Tone Power



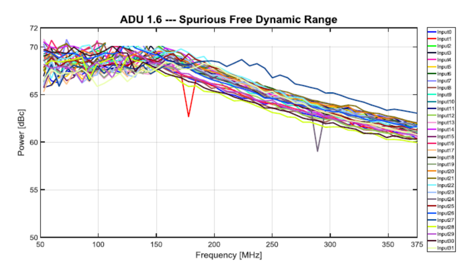
Measured Signal to Noise Ratio



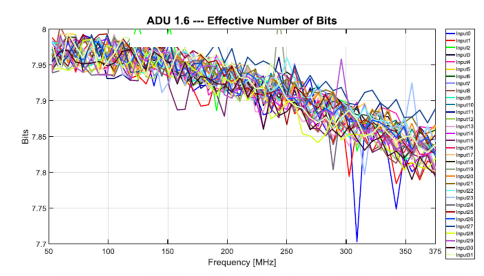
Measured 2nd Harmonic Power



Measured 3rd Harmonic Power



Measured Spurious Free Dynamic Range (SFDR)

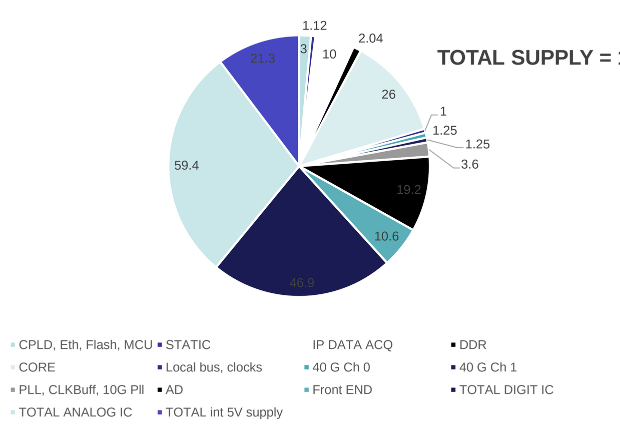


Measured Effective Number of Bits (ENOB)

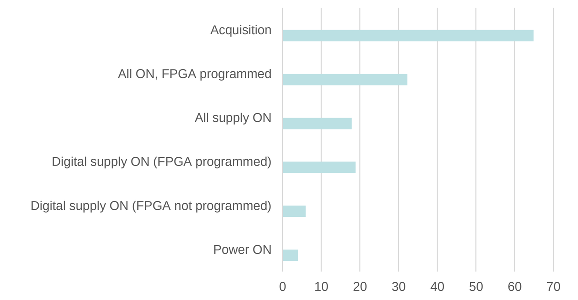
Table 1. ITPM RF measured Performances : worst values.

Fs: 800 MSPS --- BW: 50 ÷ 375 MHz	
ADC Performance Parameters	**ADU Board ver. 1.6**
Signal to Noise Ratio referenced to Full Scale [dBFS]	≥ 48.14
Gain Flatness [dBFS]	≤ ±0.81
2nd-order Harmonic Distortion [dBc]	≤ -69.86
3rd-order Harmonic Distortion [dBc]	≤ -65.28
Worst Other Spur [dBc]	≤ -59.02
Spurious Free Dynamic Range [dBc]	≥ 59.02
ENOB [bits]	≥ 7.70
Cross-Talk [dBc]	≤ -44.30

ITPM Power Budget for Components (W)



Power Supply for Operational Mode (W)



CONCLUSIONS

The Italian Tile Processor Module (ITPM) is the digital processor adopted by LFAA SKA consortium as reference design for future production and deployment of the Low Frequency SKA telescope. After seven years of design, different phases of board definition process and a number of prototyped boards, a final version ITPM 1.6 was released.
The overall ITPM system was schematically presented, together with the operational parameters, as RF and power consumption performance, that proved their compliance to the requirements fixed for the aperture array instrumentation.
ITPM board and its components, together with its sub-rack system, are undergoing a design for manufacturing phase for optimized production chain at SKA volumes.

Italian Tile Processor Module 1.6 is compliant with SKA_LFAA Technical Requirements.

ITPM is now engineering for SKA mass production.

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