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# An ASIC front-end for fluorescence and Cherenkov light detection with SiPM for space and ground applications

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## ABSTRACT

Astroparticle and High Energy Astrophysics space missions measuring extensive air showers produced by cosmic rays and neutrinos in atmosphere require detection of very faint and intense ultraviolet and visible light. Characteristics of the new generation of SiPM (Silicon PhotoMultiplier) are potentially right for this purpose. The capability to operate SiPM contemporarily in photon counting and in charge integration is strictly dependent indeed by the design of the front-end electronics (FEE). In this context, the challenge is to find the right balance and a feasible solution for managing SiPM with a FEE to be able to work, contemporarily and efficiently, in photon counting and charge integration. In this manuscript we present a new ASIC, named RADIOROC, that is an improvement of the CITIROC and that is at the end of its design phase: this chip will be able to work contemporarily in both the named modes. The RADIOROC characteristics and the first simulations carried out on the chip design will be presented.

## 1. Introduction

In the last years there were many experiments devoted to the study of energetic messengers from the Universe, first of all the Cosmic Rays and the Gamma Rays.

For the Cosmic Rays, especially the ones which have an energy greater than  $10^{19}$  eV, the flux of events is very low ( $\sim 1$  particle/ $100$  km<sup>2</sup>/year for Cosmic Rays with an energy greater than  $10^{20}$  eV) and so the only way to have a reasonable statistic is to have a very large collecting area; for this reason, the next step after the biggest existing Cosmic Rays' observatory (Auger Observatory with its 3000 km<sup>2</sup>) is to look downward at the dark earth atmosphere from an observatory placed in orbit. The two big projects that will be devoted to this goal will be: EUSO (Extreme Universe Space Observatory) and POEMMA (Probe of Extreme Multi-Messenger Astrophysics). These projects will not search only energetic cosmic rays, but other rare events like neutrinos.

For energies up to a few hundred TeV it is possible to use ground-based telescopes such as Cherenkov telescopes, which are dedicated to the detection of gamma rays. The next years will be led by the

CTA (Cherenkov Telescope Array) observatory, that will be made by different types of telescopes to search the gamma universe from 20 GeV to 300 TeV.

This manuscript is intended to present the design of a new ASIC (and the electronics related to it) that will be able to manage all of these instrument detectors. In the following sections we will briefly talk about the physics of cosmic rays, neutrinos and gamma rays and a reminder about the Cherenkov and fluorescence phenomena. Then we will talk about the electronics needed to detect these ones; the design of the new ASIC starts from the modification of an existing front-end, so we will introduce the CITIROC and its use in the ASTRI-Horn telescope. Then we move on to the description of the changes to be made to the chip to obtain the RADIOROC and we will conclude with the first tests made on the ASIC design.

## 2. Physics

The experiments mentioned in ¶ 1 will be devoted to the search of Ultra High Energy Cosmic Rays (UHECRs), neutrinos and gamma rays. Some of them are indicated in Fig. 1 and here we summarize them.

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Detector Read-Out	SiPM, SiPM array
Number of Channel	32
Signal Polarity	Positive
Sensitivity	Trigger on 1/3 photo-electron
Timing Resolution	better than 100ps RMS on single photo-electron
Dynamic Range	0-400 pC i.e 2500 photo-electrons @ 10 <sup>4</sup> SiPM gain
Packaging & Dimension	<ul style="list-style-type: none"> <li>TQFP 160 28x28mm</li> <li>TFBGA 353 12x12mm</li> </ul>
Power Consumption	225 mW when all stages on - supply voltage 3.3V
Inputs	32 voltage inputs with independent SiPM HV adjustments
Outputs	<ul style="list-style-type: none"> <li>32 trigger outputs</li> <li>2 multiplexed charge output</li> <li>2 ASIC trigger output (Trigger OR)</li> </ul>
Internal Programmable Features	<ul style="list-style-type: none"> <li>32 HV adjustment for SiPM (32*8bits)</li> <li>Trigger Threshold Adjustment (10bits)</li> <li>Channel by channel gain tuning</li> <li>32 Trigger Masks</li> <li>Trigger Latch</li> <li>Internal temperature sensor</li> </ul>

Fig. 3. CITIROC ASIC main characteristics.

is possible using a channel-by-channel 8-bit DAC (Digital-to-Analog Converter) connected to the ASIC inputs. This allows a fine SiPM gain adjustment at the system level to correct for the gain non-uniformity of SiPM pixels. Timing measurement better than 100 ps RMS jitter is possible along with 1% linearity energy measurement up to 2500 pe. The power consumption is about 7 mW/channel with all features ON.

Going into detail, as explained in Catalano et al. 2018 [7] and shown in Fig. 2, each CITIROC is characterized by separate chains for high gain (HG), low gain (LG) and trigger outputs. The pulse generated by the SiPM is processed by the AC-coupled CITIROC electronic channel: it is amplified by means of two programmable preamplifiers and then shaped (shaping time = 25 ns) with two shaper circuits (LG and HG respectively). A bipolar fast shaper (FSH in Fig. 2) connected to the high gain preamplifier produces a fast signal (~15 ns shaping time) that is connected to a discriminator with a 10 bits-DAC programmable threshold. The output of the discriminator gives a digital signal (trigger) if the input signal exceeds the threshold level. The peak detector or single channel analyzer (track&hold mode) are selectable via slow-control configuration bits. The base-line operational mode is peak detector. Peak detector captures the most positive point of the input signal so that the maximum of the shapers signals represents the pulse height conversion of the SiPM output signal. The ASTRI-Horn telescope is equipped with 64 pixels SiPMs, so the FEE needs two chips; the digital triggers (64 trigger channels) are available on the 32 + 32 output pads of the two ASICs constituting the unit module based on 64 pixels. The analog outputs of the peak detectors are stored into 64 analog memories and read, at the occurrence of a trigger condition, by multiplexing the three-state output registers (LG and HG respectively) and then converted to digital counts by external ADC devices. An FPGA (Field Programmable Gate Array) manage all the input/output operations from/to CITIROCs and SiPMs.

#### 4. RADIOROC requirements

Although the great results obtained by CITIROC (in the ASTRI-Horn system), it is not suitable for the detection of fluorescence light, where single photon counting with a double pulse resolution of few ns is needed. To do this, we need the new ASIC: as already said, the RADIOROC is an improvement of the CITIROC, with the possibility to have up to 100 MHz single photon counting, 64 channels and other features required to the Weeroc company, that now has just reached the final stage of the design phase.

To detect both fluorescence and Cherenkov light, single-photon counting as well as charge integration should coexist within the same

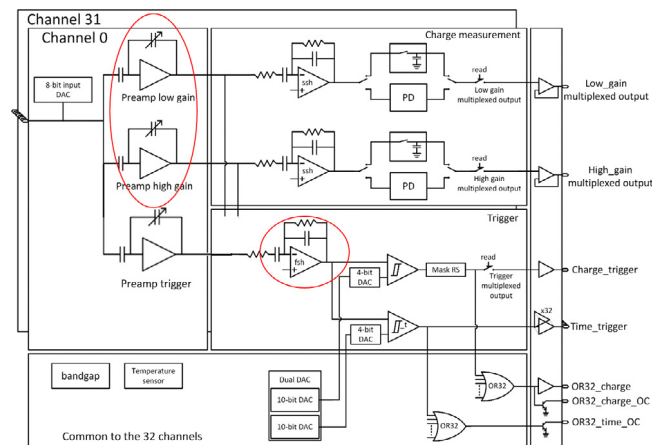


Fig. 4. General block scheme of the CITIROC with the changes to be made for RADIOROC highlighted by red ovals.

ASIC and these modes must be selectable by the user by means of a set of programmable functions, implemented through a string of configuration bits, which instruct the front-end on the desired operating mode. In single-photon-counting mode, a double pulse resolution of a few ns ( $\approx 10$  ns) is necessary to avoid pulses pile-up. For the input stage, a programmable pole-zero cancellation technique is required to cope with long tail SiPM signals; the CITIROC has a fast-shaper that works like a normal shaper, where each pulse has a positive and negative part. To avoid the long tail (under the baseline) that can cause pile-up problems it is preferred a pole cancellation circuit that assure a stable single photon counting. Analog chains based on fast pulse sampling or pulse height measurement technique using peak detector should be implemented including pulse-shaping time and pre-amplifier gain programmability in order to cover the desired energy dynamic range (energy measurement from 1 pe up to several thousand pe within 1% linearity should be acceptable). Digital triggers should be managed and selectable. Fast discriminators with user adjustable threshold by means of DAC provide the digital trigger signals that are routed to a majority/topological trigger logic in the FPGA. Timing measurement should also be better than 100 ps RMS jitter. Masking of the digital triggers is also required to switch off potential noisy pixels. An adjustment of the SiPM high-voltage should be allowed using channel-by-channel DAC connected to the ASIC inputs. This allows for a fine SiPM gain adjustment at the system level to correct for the gain non-uniformity of SiPMs.

For all the things explained in this section and in the previous one, we could say that the CITIROC 1A was a good starting point in order to create the new RADIOROC, applying some important modifications:

- the preamplifiers shall be redesigned to let them work with a bigger bandwidth;
- a preamplifier shall be added in the trigger chain;
- and a pole zero cancellation circuit shall replace the trigger fast shaper to have a trigger pulse at  $\sim 3$  ns (unlike the previous configuration with  $\sim 18$  ns).

#### 5. RADIOROC simulation results

Meeting the requirements, the Weeroc company implemented all the changes in the RADIOROC; a block scheme of the CITIROC, with all the modifications aforesaid, is shown in Fig. 4, remembering that the RADIOROC will manage 64 channels instead of 32.

In addition to the block scheme, here we present some simulations carried out on the ASIC design, using the “Spectre” simulator of Cadence [8].

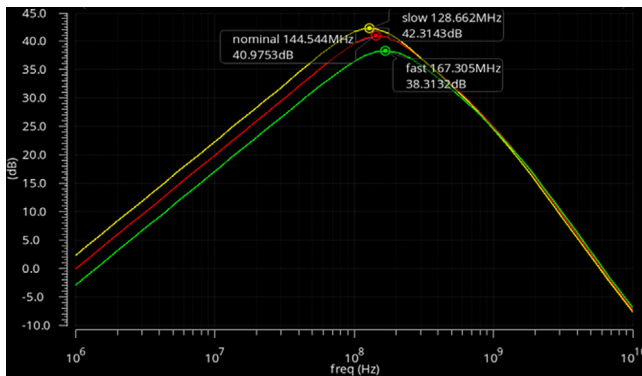


Fig. 5. Trigger preamplifier Bode diagram for 3 corner simulations.

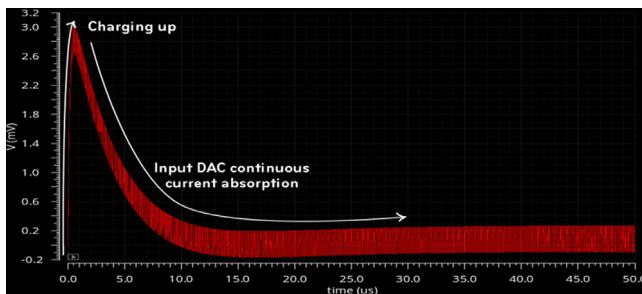


Fig. 6. Input signal by triggering a photoelectron every 10 ns (100 MHz signal).

The Bode diagram of the trigger chain preamplifier looks like a bandpass filter with the high-cut frequency being the actual bandwidth of the amplifier. The transfer function of 3 different simulations is shown in Fig. 5. The low-cut frequency is crucial to the recovery time of the preamplifier to handle high pe rates for photon counting application.

To validate the design of the RADIOROC, simulations have been carried out with different input signals. A simulated SiPM signal is shown in Fig. 6 and is related to one pixel of  $6 \times 6 \text{ mm}^2$ .

One of the most important parameter is the response of the preamplifier to a signal; the output when the input signal is set at 100 MHz is shown in Fig. 7. We chose 100 MHz because it corresponds to 10 ns, that is the average time we need for our purposes, as explained in ¶ 4.

The discriminator output, for the same 100 MHz input signal, is shown in Fig. 8.

## 6. Conclusions

In case of space missions, as well as for ground experiments, measurement of fluorescence, Cherenkov light or atmospheric phenomena require detection, with different time scale, of very faint and very intense light. Therefore, single photon counting and charge integration must coexist in the same front-end to obtain optimum performance; the CITIROC 1A chip lent itself to the changes suggested in short time. We believe that RADIOROC will be very important for any space mission and particularly for the proposed UHECR space missions as EUSO, POEMMA and similar ones. The progress in SiPM manufacturing, front-end ASIC and system integration associated with System on Chip design made it possible for this outcome to be achieved; an example of this kind of integration has been used successfully in the ASTRI-Horn Cherenkov telescope.

Summarizing, the main specifications of the RADIOROC are:

- SiPM high-voltage adjustment (with DACs connected to the ASIC inputs);

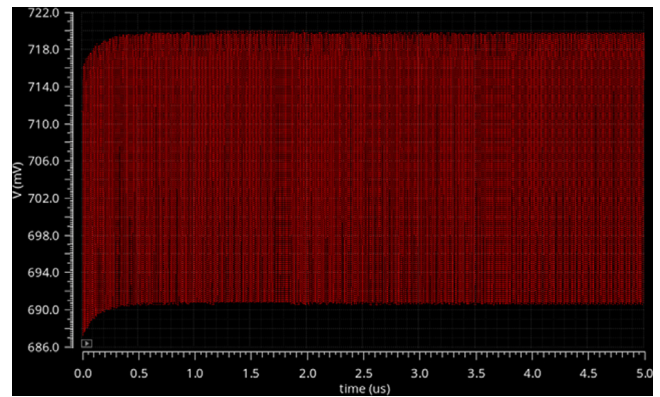


Fig. 7. Preamplifier output with a 100 MHz input signal.

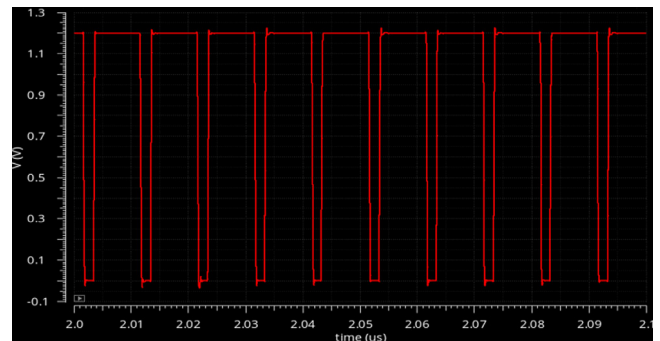


Fig. 8. 10 ns discriminator output.

- double pulse resolution of a few ns ( $< 10 \text{ ns}$ ) (to reduce pulses pile-up);
- programmable pole-zero cancellation trigger shaper (to cope with long tail SiPM signals);
- analog pulse height measurement using fast peak detector;
- wide energy dynamic range (energy measurement from 1 pe up to several thousand pe);
- 64 digital triggers;
- timing measurement better than 100 ps RMS;
- masking of the digital triggers (switch off potential noisy pixels);
- each parameter of the chip individually modifiable through slow control.

As can be seen from the simulations carried out on the ASIC design, shown in Figs. 5–8, the targets were achieved with regard to the resulting double-pulse resolution of 10 ns (100 MHz).

At the end we must remember that the new ASIC is still at the end of its design phase, so we are waiting to have it in our hands to do intensive laboratory tests to better understand its real potential.

## Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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