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INAF Technical Report

Son Of X-Shooter

SOXS

UV-VIS Detector System Design

Technical report version 1.5
SOXS-TRE-0005
Date: 26/01/2022

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CHANGE RECORD

ISSUE	DATE	SECTION/PARAGRAPH AFFECTED	REASON/INITIATION DOCUMENTS/REMARK
1.0	22.12.2017	all	Issue for FDR
1.1	29.01.2018	all	corrections
1.2	27.06.2018	all	Upgrade
1.3	20.09.2018	all	After the RIX
1.4	01.10.2018	all	Upgrade if the mechanical design
1.41	5/10/2018	3.4.3	Figure and text added
1.5	26/01/2022	3.2; 3.3; 3.5; 3.6; 5	Upgrade

TABLE OF CONTENTS

1 Purpose and Scope of the Document

We present a general overview about the UV-VIS detector system, the detector selection vs detector performances and the electronics adopted to control and manage the CCD readout.

2 List of Applicable and Reference Documents

2.1 Applicable Documents

Ref.	Document title	Document ID
AD1	Memorandum of Understanding for Preliminary Design Phase of the SOXS project	N°11206/LET/CP/AMA
AD2	Interface specification for visiting Instruments in La Silla Observatory	LSO-SPE-ESO-00000-0003
AD3	CALL FOR PROPOSALS	Ref. 10828/LET/CP/AMA Annex 1
AD4	Requirements for Scientific Instruments on the VLT Unit Telescopes	VLT-SPE-ESO-10000-2723 Issue 1 dd. 18.03.05
AD5	SOXS Verification Plan	SOXS-PLA-0004
AD6	SOXS Optical Design	SOXS-TRE-0001
AD7	SOXS Mechanical Design	SOXS-TRE-0002
AD8	SOXS Cryogenic Design	SOXS-TRE-0003
AD9	SOXS Software Design	SOXS-SPE-0002
AD10	SOXS AIT Plan	SOXS-PLA-0003

2.2 Reference Documents

Ref.	Document title	Document ID
RD1	SOXS: Technical, Management Plan and Schedule Proposal	
RD2	New General Detector Controller (NGC) USER MANUAL	VLT-MAN-ESO-13660-4510
RD3	Interface Control Document for the New General detector Controller (NGC)	VLT-ICD-ESO-13660-4009
RD4	New General Detector Controller (NGC) Technical Report	VLT-TRE-ESO-13660-3900

3 UV-VIS Detector System

The UV-VIS CCD Detector Systems for SOXS is designed to reach a wavelength response from 350 to 850 nm and consist of the following sub-systems:

1 e2v CCD44-82 2K x 4K CCD
2 CFC cooling system
3 detector head
4 CCD controller unit and power supply to operate the CCD detector head, with cable set to connect them
5 shutter
6 Commercial shutter control unit with cable set.
7 temperature controller with cable set

The visible camera will be developed under the responsibility of SOXS team; INAF will buy the hardware from ESO in order to have an ESO compliant system at the NTT ESO observatory.
INAF plans to have a period in Garching to get know-how on NGC and to learn how assemble of the CCD into the UV-VIS camera following the ESO standardization (we decided to use the same arrangement used for the CCD e2v 4482 at ESO).
The CCD will be integrated by the INAF team (we have the facilities to do this operation).

3.1 VIS Detector

The detector chosen for the SOXS UV-VIS arm is an e2v CCD44-82. This detector is a high performance, back illuminated CCD with a 15.0 µm square pixel and an image area of 30.7x61.4 mm and is characterised by a high Quantum Efficiency (QE). In Figure 1 is shown the QE of this detector for different coatings.
This detector technology was chosen for the following reasons:

1. devices manufactured with this technology meets or exceeds the requirements
2. INAF has extensive experience with devices with this technology and it is considered to be of low risk.

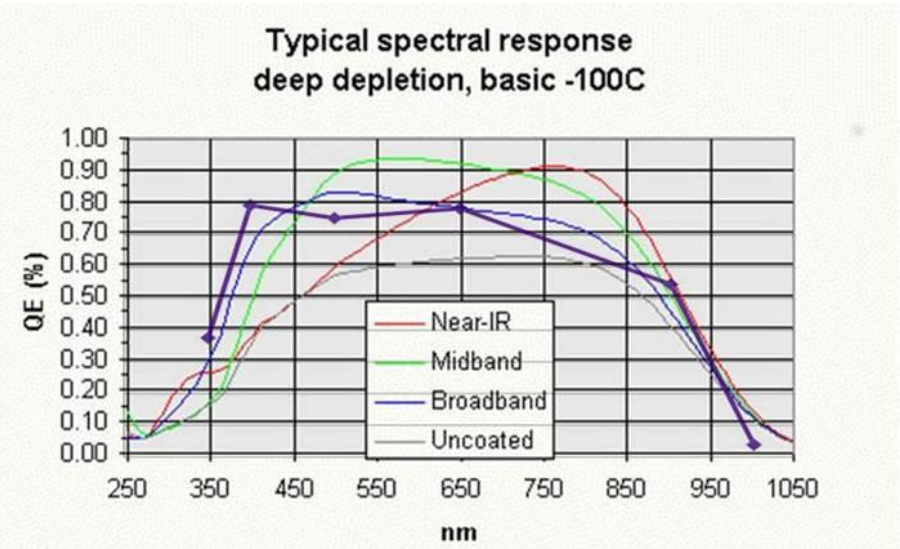

Figure 1 - QE vs. wavelength for different coatings as provided by the manufacturer. The selected CCD is the midband, the purple points are our specific CCD QE data, taken from the e2v technical note.

In Error! Reference source not found. the test-sheet of the SOXS detector show more details of the CCD characteristics.

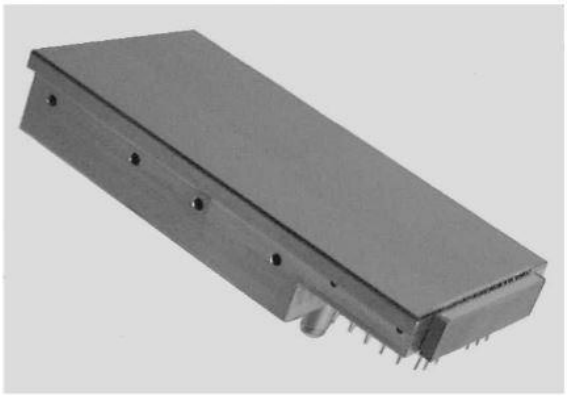

Figure 2 - CCD44-82 back-illuminated CCD sensor

Table 1 - CCD main characteristics

Detector	CCD44-82
Chip type	Thinned back illuminated
Pixel size	15 µm
Area (pixels)	2048 x 4096
Area (mm)	30.7 x 61.4
QE at 500 nm	90%
Coating	yes
Flatness	Better than 20 µm peak to valley
Peak signal	200 ke^-/pixel
CTE Serial OSL	99.9993%
CTE Serial OSR	99.9999%
CTE Parallel	99.9998%

3.2 The camera housing

The detector head and the wiring are based on the heritage of existing instruments at ESO. The head is coupled with a Continuous Flow Cryostat (CFC) cooling system, successfully adopted in several ESO projects. The UV-VIS camera is made up by the ESO CFC cooling system coupled with the custom detector head (Figure 3 and Figure 4) that allows its placement into the UV-VIS arm of the spectrograph. Due to the reduced space available in the spectrograph, the front part of the camera, where the light will be incoming, has a special rectangular design called 'nose'.

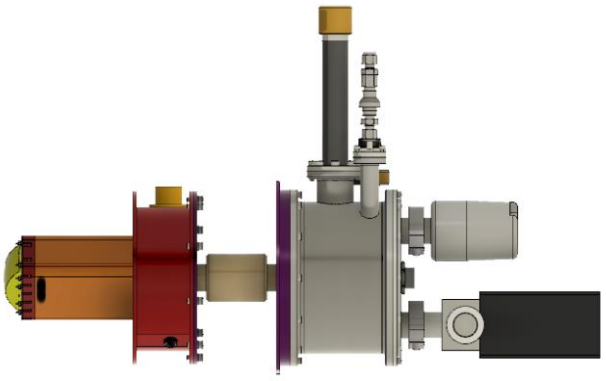

Figure 3 - Drawing of the VIS detector system

Figure 4 - Camera housing and CFC mounted in the test bench

3.3 Detector head and wiring

The detector wiring, i.e. the baseplate and flex circuits (Figure 5 and Figure 6), will provide the components to safely mount the CCD and to conduct signals from the CCDs to the external wall of the cryostat. It also provides the mounting and wiring for the temperature sensors and heater that stabilize the detector temperature and monitor cryostat performance. The detector wiring will place minimal heat load on the cooling system. It should not introduce noticeable crosstalk or readout noise, and it should also be flexible enough to accommodate shrinkage during cooling down. It should not add appreciably to the outgassing and should use as much as possible previously tested cryogenic compatible materials and components. In the design and choice of fabrication materials and techniques for the detector head wiring, the following rules have been followed:

- the preamplifiers are placed attached to the cryostat or very close to it
- the clocks-filters and wave-shaping (passive components) are placed in a box attached to the cryostat or inside the cryostat .
- clock, bias, output, and temperature signal groups are kept separated, with ground shields in between
- the thermal load of wiring on cryogenic cooling is kept as low as possible.

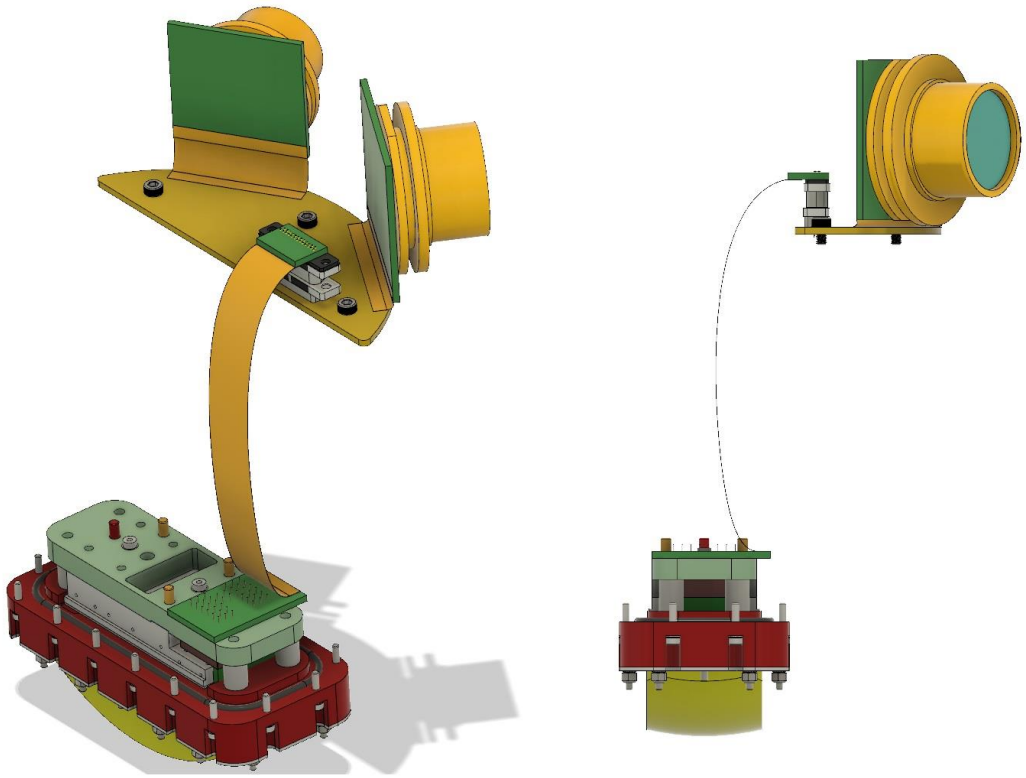

Figure 5 - CCD wiring

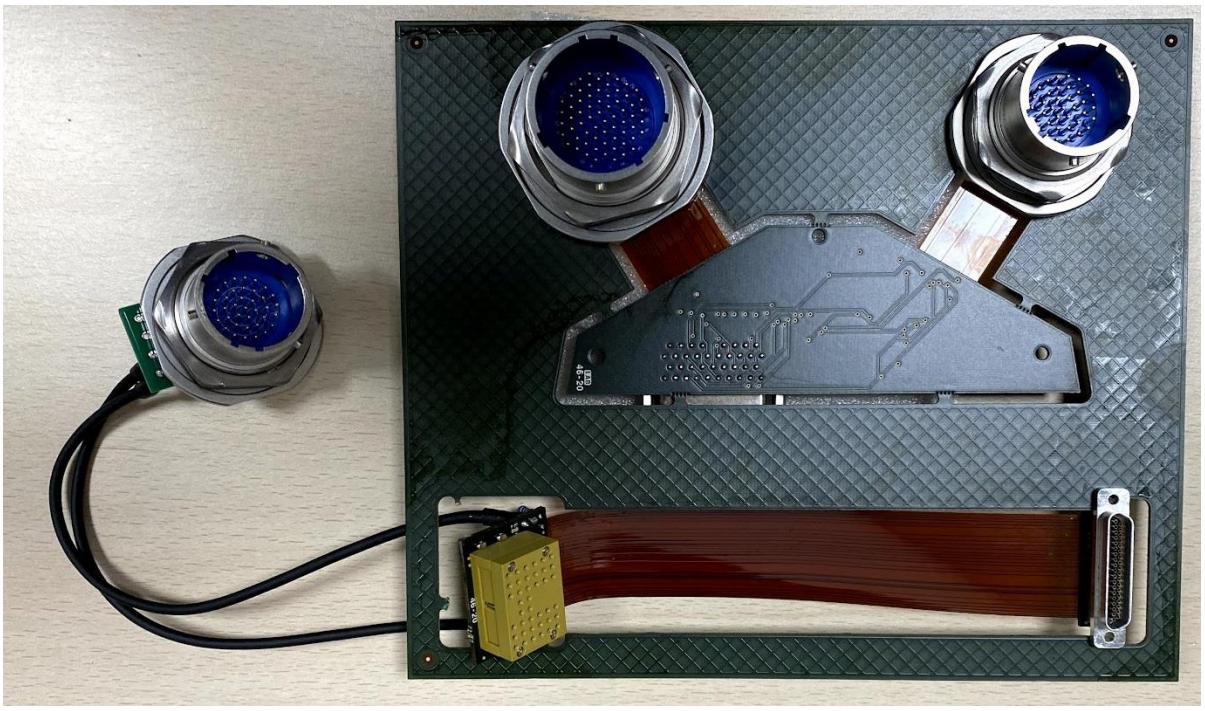

Figure 6 - CCD wiring boards

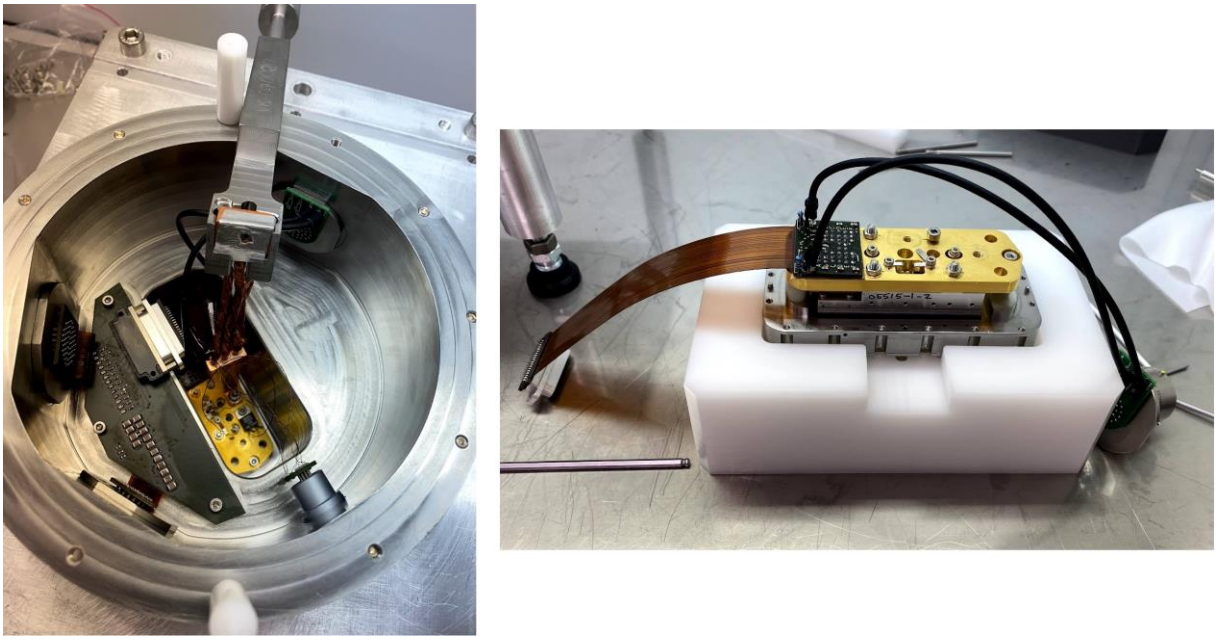

Figure 7 - camera wiring

3.4 CCD controller unit

The detector controller provides the biases and the correct sequences of clocks and analog video processing to drive and acquire the images of the CCDs. The dead time is defined as the interval between the end of one exposure (closed shutter) to the start of the next one (open shutter) and it obviously includes the read time and also other software overheads, e.g. for data storage and shutter control. The CCD controller will be the NGC (New General detector Controller) system. This controller, designed by ESO to replace the former FIERA and IRACE devices, is a single multipurpose controller able to manage both CCDs and IR arrays. The NGC is the current controller for ESO instrumentation and it will be adopted in SOXS project as well to comply with ESO standards and to reduce any compatibility failure with ESO hardware and software systems. The NGC is based on newest hardware standard (FPGA), it has the same hardware core for both optical and IR controllers and, in addition, is fully compatible with ESO software and it includes all the good features of previous systems.

NGC consists of five major components:

- Data Acquisition Computer with integrated PCIe interface (DAQC)
- Detector Front-end (DFE)
- Detector Cryostat Cables (DCC)
- Detector Front-end Power Supply (DFPS)
- Detector Preamplifier (DPA)

The main NGC features are:

- high speed link
- the core element on each board is a Xilinx FPGA
- digital parts and the sequencer are implemented in the FPGA
- compact system
- full compatibility with ESO SW standard

The controller has to be located near the detector, because the maximum cable length must be 2 m.

The control system, for VIS detector, is composed by:

1. LLCU, which is a Linux machine (DELL or an industrial PC)
2. PCI-Express card
3. front-end box (preamplifier)
4. power supply, including the cable to the NGC
5. two NGC modules
6. fiber interfaces, including fiber cable
7. CCD temperature control
8. Shutter driver

The NGC has three different housing: compact, fan-less and water-cooling. The housing is selected according to the setup where the controller is located. In SOXS situation we need to locate the controller close to the instrument because the cable between the dewar and the device must be shorter than 2 m. Therefore, we have to select the water-cooling housing to prevent any thermal dissipation into the telescope Nasmyth room.

Figure 8 - The NGC water-cooling housing

Figure 9 - The NGC Two-Slot system housing

The power supply for the NGC device is a 19-inch 3HE rack-mountable unit, which may be at a distance from the DFE of up to 12 meters (see. Figure 15, Figure 16, Figure 17).

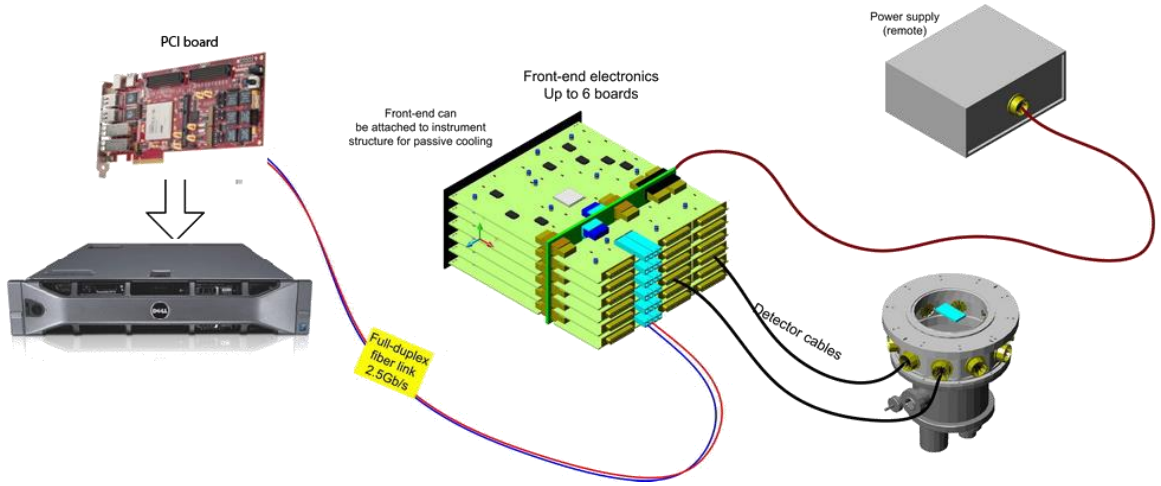

Figure 10 - The New General detector Controller (NGC)

3.4.1 PCI interface Board (DAQC)

An ESO-made PCI64 board (Figure 11) with a fiber-optic connection to the Front End is installed in the Data Acquisition Computer. The maximum theoretical bandwidth per interface is 256MB/s, which matches the 2.5 GBit/s fiber transmission rate. The bandwidth for actual data transmission is about 20% lower.

Figure 11 - The PCIe interface board (DAQC)

3.4.2 Detector front-end (DFE)

The DFE has to be located close to or on the instrument (maximum detector cable length 2m depending on the application, an extension up to 3m may be possible).
The module, from which the VIS NGC DFE can be built, is one Basic Board that contains four video channels and clock/bias generation.
In order to prevent damage from overheating, all housings shall have equipped with a thermal sensor that can shut off the power to the NGC box.

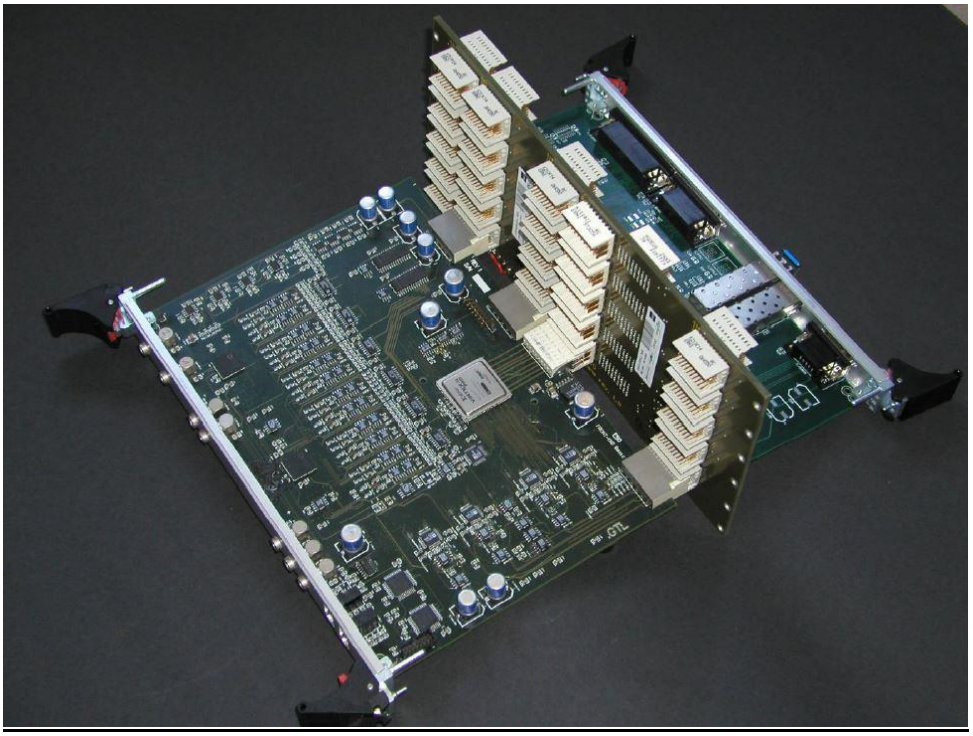

Figure 12 - NGC system with Basic Board, Backplane and Transition Board (VIS arm)

3.4.3 Detector Cryostat Cables (DCC)

The Detector Cryostat Cable is the connection between the DFE and the VIS camera (Figure 13). It contains clock and bias lines and the video signals. The maximum length depends on application (2-3 m). The cable shown in Figure 13 is the detector-cryostat cable that we shall use for SOXS (bias and clock separated).

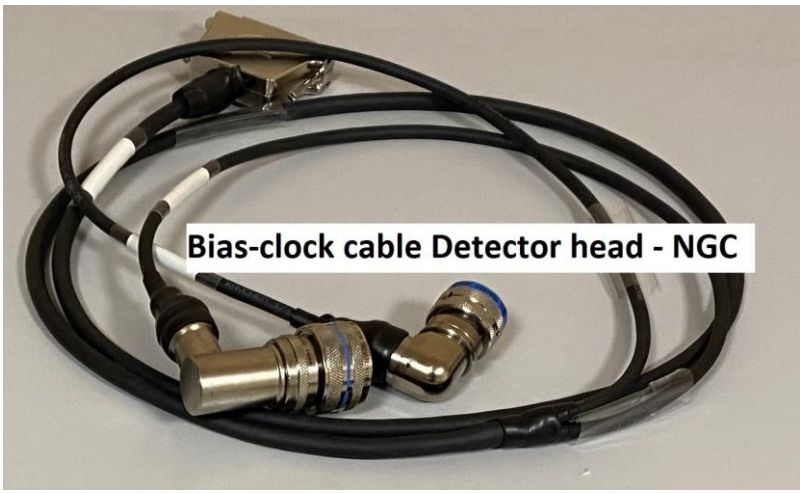

Figure 13 – Detector Cryostat Cables (DCC)

The SOXS interfaces between the NGC and the cryostat will be done following the same philosophy used by ESO for the implementation of the e2v 44-82 with the NGC. The ESO architecture implements the CCD wiring very similar to the shown in Figure 5 and two vacuum connectors; one for the clock signal and the other for the Video and Bias. In Figure 14 the VIS-UV interfaces between the NGC and the cryostat are shown.

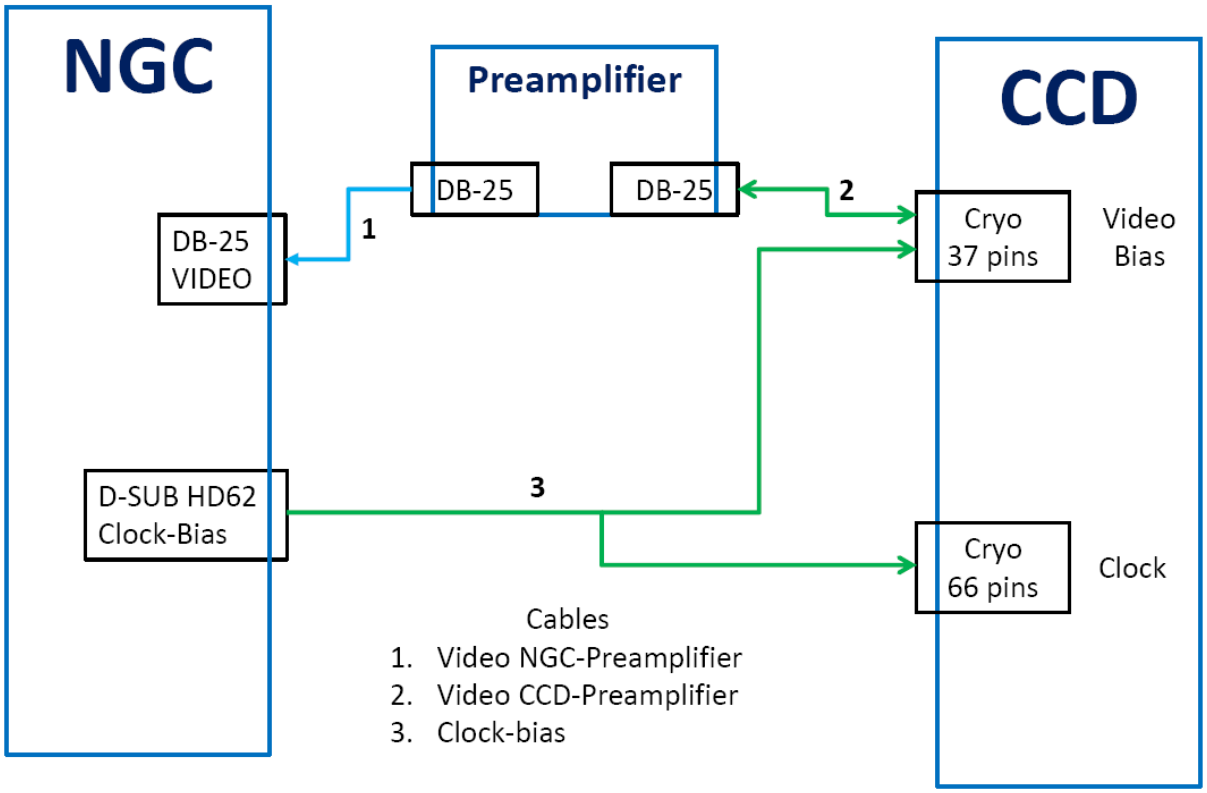

Figure 14 - Interfaces between NGC and the cryostat

3.4.4 Detector Front-end Power Supply (DFPS)

The power supply for the DFE is a 19-inch 3HE rack-mountable unit which may be at a distance from the DFE of up to 12 meters.

Figure 15 - Power supply (front view)

Figure 16 - Power supply (back view)

Figure 17 - Power supply cable

3.4.5 Detector Preamplifier (DPA)

The CCD preamplifier is placed between the cryostat and the DFE. The location of the Detector Preamplifier is application dependent; in the SOXS case of an optical detector the preamplifier is located outside the cryostat. It features 4 video channels with 16 software-selectable gains and 8 software-selectable bandwidths per channel. Its outer dimensions are 100 x 120 x 40 mm^3. The preamp is show in Figure 18.

Figure 18 - Detector Preamplifier (DPA)

For optical detectors the preamp is located outside the cryostat by a 10 to 15cm cable connecting the cryostat to the preamp. This is cable and its layout are shown in Figure 19

Figure 19 - CCD cryostat video cable

Figure 20 - NGC-Preamplifier cable

3.5 Shutter control

The shutter control shall be driven by the CCD controller and will be managed by a commercial shutter control. The shutter selected is a Uniblitz DSS10B1T1 with the controller model VED24 (Figure 21).

Features:

- 10mm aperture
- Bi-stable operation
- extremely slim, low-profile form-factor
- RoHS Compliant
- transfer time on opening: 5.0 milliseconds
- total opening time: 8.6 milliseconds
- configured for the VED24 shutter driver
- It is guaranteed to operate for 2,000,000 operations

Figure 21 - Shutter Uniblitz DSS10B1T1 and controller VED24

Figure 22 - Shutter cable

3.6 Temperature controller

For the CCD temperature control two options can be taking into account:

- The CCD controller integrated control
- A commercial temperature control (i.e. Lakeshore 336)

The characteristics of the Lakeshore 336 are summarized in the following list:

- operates down to 300 mK with appropriate NTC RTD sensors
- four sensor inputs
- two PID control loops: 100 W and 50 W into a 50 Ω or 25 Ω load
- auto-tuning automatically collects PID parameters
- automatically switch sensor inputs using zones to allow continuous measurement and control from 300 mK to 1505 K
- ccustom display set-up allows you to label each sensor input
- Ethernet, USB and IEEE-488 interfaces
- Supports diode, RTD, and thermocouple temperature sensors
- Sensor excitation current reversal eliminates thermal EMF errors for resistance sensors
- ±10 V analog voltage output, alarms, and relays

Figure 23 - Temperature controller Lakeshore 336

Figure 24 – Temperature cable (monitoring and control)

4 AIV Plan

This paragraph presents the Manufacturing, Assembly, Integration and Verification logic of the VIS-UV detector system (**AD10**).

- NGC installation and test
- Assembly of the engineering CCD in the detector head and test
- Mounting of the scientific CCD in the detector head and test
- CCD optimization
- Test of the camera after the integration in the spectrograph

Table 2 - NGC Installation and test

Step ID	Sub-Sys VIS detector 01
Title	NGC installation and test
Tools needed	PC+ NGC + cables + oscilloscope
Prerequisites	
Description	This test consists in the verification of the NGC functionality and the generation of the correct bias and clock for the CCD readout.
Responsible	Rosario Cosentino
Estimated Time	Two weeks
Number of People	2
Success criteria	Verification of the bias voltages and clock sequence and readout of a dummy image
Notes	Before the integration of the CCD

Table 3 - Assembly of the engineering CCD in the detector head and test

Step ID	Sub-Sys VIS detector 02
Title	Assembly of the engineering CCD in the detector head and test
Tools needed	PC+ NGC + detector head + engineering CCD + clean room + CCD mounting hardware + vacuum pump + cryogenic control system + LN_2
Prerequisites	Detector head previously tested (vacuum and cryogenics)
Description	This test consists in the verification of the correct CCD readout.
Responsible	Rosario Cosentino
Estimated Time	Two weeks
Number of People	2
Success criteria	Readout of the CCD (bias, dark and sample image) with image quality as expected
Notes	Before the integration in the spectrograph

Table 4 - Mounting of the scientific CCD in the detector head and test

Step ID	Sub-Sys VIS detector 03
Title	Mounting of the scientific CCD in the detector head and test
Tools needed	PC+ NGC + detector head + scientific CCD + clean room + CCD mounting hardware + vacuum pump + cryogenic control system + LN_2
Prerequisites	Step 2 completed
Description	This test consists in the verification of the correct CCD readout.
Responsible	Rosario Cosentino
Estimated Time	7 days
Number of People	2
Success criteria	Readout of the CCD (bias, dark and sample image) with image quality as expected
Notes	Before the integration in the spectrograph

Table 5 - CCD optimization

Step ID	Sub-Sys VIS detector 04
Title	CCD optimization
Tools needed	PC+ NGC + detector head + scientific CCD + vacuum pump + cryogenic control system + LN_2
Prerequisites	VIS camera (step 3 completed)
Description	This test consists in the optimization of the CCD readout parameters.
Responsible	Rosario Cosentino
Estimated Time	7 days
Number of People	2
Success criteria	Optimization of the readout parameters (clock and biases) to reach the optimum performances of the CCD
Notes	Before the integration in the spectrograph

Table 6 - Test of the camera after the integration in the spectrograph

Step ID	Sub-Sys VIS detector 05
Title	Test of the camera after the integration in the spectrograph
Tools needed	VIS camera complete with NGC + SOXS vacuum system + SOXS cryogenic control system + LN_2
Prerequisites	VIS camera optimized (step 4 completed) and integration in the VIS arm completed
Description	This test consists in the verification of the correct functioning of the VIS acquisition system in the VIS arm of the spectrograph
Responsible	Rosario Cosentino
Estimated Time	7 days
Number of People	2
Success criteria	No degradation in the performance previously measured and acquisition of spectra images
Notes	After the integration in the VIS arm

5 System costs

In Table 7 are summarized the estimated cost of the detector system of the UV-VIS arm.

Table 7 - Estimated budget

UV-VIS Detector System Budget	
VIS Detector	84 K€
CCD socket	1.2 K€
Detector controller (NGC)	42 K€
Vacuum connectors	2409 USD
Optical fiber PC-Controller	Included in detector controller
Power cable	Included in detector controller
clock-bias cable	2103,95 €
CTRL-Pre cable	Included in detector controller
Pre-dewar cable	705,70€ (estimated)
Preamplifier	Included in detector controller
Temperature controller	3,500 €
Shutter Driver VED24	1025 $
Shutter DSS10B1T0L	450 $ (no feedback model)
PCB, flat cables, etc	3 K€
CCD Head	Not included in this WP
CFC control electronic	Not included in this WP

Abbreviations and Acronyms

AD	Applicable Document
ADC	Analog-to-Digital Converter
AI	Action Item
AIT	Assembly, Integration and test
AIV	Assembly, Integration, Test & Verification
CCD	Coupled Charged Device
CFC	Continuous Flow Cryostat
CRE	Change Request
CTE	Charge Transfer Efficiency
DAQC	Data Acquisition Computer
DCC	Detector Cryostat Cables
DFE	Detector Front-end
DFPS	Detector Front-end Power Supply
DNO	Discrepancy Note
DPA	Detector Preamplifier
DRD	Document Requirement Description
DRS	Data Reduction Software
ESO	European Southern Observatory
FDR	Final Design Review
FITS	Flexible Image Transport System
FOV	Field Of View
FPGA	Field Programmable Gate Array
HW	HardWare
ICD	Interface Control Document
ICS	Instrument Control Software
INAF	Istituto Nazionale di Astrofisica
KoM	Kick off Meeting
LAN	Local Area Network
LPO	La Silla Paranal Observatory
LRU	Line Replaceable Unit
MAIT	Manufacture, Assembly, Integration and Test
MoU	Memorandum of Understanding
NGC	New Generation Controller
NTT	New Technology Telescope
PAC	Provisional Acceptance Chile
PAE	Preliminary Acceptance Europe
PCI	Peripheral Component Interconnect
PDP	Preliminary Design Phase
PDR	Preliminary Design Review
PID	Proportional, Integral, Derivative
QE	Quantum Efficiency
RAMS	Reliability, Availability, Maintenance and Safety (analysis)
RD	Reference Document
SoW	Statement of Work
SOXS	Son Of X-Shooter

SW	Software
TBC	To be Confirmed
TBD	To Be Defined
TCS	Telescope Control System
TLR	Top Level Requirements
TRS	Technical Requirements Specifications
USB	Universal Serial Bus
UT	Unit Telescope (of the VLT)
VLT	Very Large Telescope
WP	Work Package
ZIF	Zero Insertion Force

Appendix A CCD44-82 Testsheet

e2v

Waterhouse Lane, Chelmsford, Essex CM1 2QU United Kingdom
Telephone: +44 (0) 1245 493493 Facsimile: +44 (0) 1245 492492
Internet: www.e2v.com

CCD44-82 SLOWSCAN TEST SHEET — Form No. 10683N

TITLE: **Back Illuminated, Non-AIMO, Deep Depleted silicon** — Version 6 — Sheet 1 of 1

Associated Document: A1A764199

Device serial number	09491-08-01	Tester (Initials & Clock No.)	SW 30318
Grade	0	Date	20-Jan-11
		Device type number	CCD44-82-0-E93

TEST RESULTS

TEST		RESULT	LIMITS Grade 0	LIMITS Grade 1	LIMITS Grade 2	UNITS
GAIN (AMPLIFIER RESPONSIVITY)	OSL	6.29	4.5 min.			µV/e⁻
	OSR	6.01	4.5 min.			µV/e⁻
NOISE	OSL	2.3	4.0 max.			rms e⁻
	OSR	2.3	4.0 max.			rms e⁻
NON Linearity (to 150k electrons)	OSL	0.3	5.0 max.			%
	OSR	0.3	5.0 max.			%
CTE (serial)	OSL	99.9993	99.999 min.			%
	OSR	99.9999	99.999 min.			%
CTE (parallel)		99.9998	99.999 min.			%
DEFERRED CHARGE		0.0	3.0 max.			e⁻
SATURATION LEVEL FOR IMAGE AREA		313	150 min.			ke⁻
DEFECTS IN DARKNESS	POINT DEFECTS (a)	184	500	1000	1500	max.
PHOTO-RESPONSE DEFECTS	DARK POINT DEFECTS (b)	20	For information only			n/a
	TRAPS	2	20	30	50	max.
TOTAL PIXEL DEFECTS (a+b)		204	1250	2000	3000	max.
TOTAL COLUMN DEFECTS		0	2	6	12	max.
MEAN DARK SIGNAL		0.0	2.0 max. at -120°C			e⁻/pix/h
AREA DARK SIGNAL (32 x 32 block)		0.1	For information only			e⁻/pix/h

TEST		RESULT	LIMITS for device variant: Astro Midband -D26	Astro Broadband -D03, -B43	Astro ER1 -D23, -D48	Basic ER1 -A72	Astro 2layer -D42 -E93	Astro graded -E97	UNITS
QUANTUM EFFICIENCY	at 350 nm	37.4	20	40	20	10	30	FIO	min. %
	at 400 nm	79.3	50	70	35	25	70	35	min. %
	at 500 nm	75.3	80	75	65	60	75	65	min. %
	at 650 nm	78.4	80	70	80	85	75	85	min. %
	at 900 nm	54.4	40	40	45	45	50	50	min. %
	at 1000 nm	4.0	FIO	FIO	FIO	FIO	FIO	10	min. %
PHOTO-RESPONSE NON-UNIFORMITY	at 400 nm	1.6	3.0 max.					FIO	max. %
	at 650 nm	1.6	3.0 max.					FIO	max. %
	at 900 nm	1.6	5.0 max.					FIO	max. %

CUSTOM TESTS (if applicable)

TEST	RESULTS	LIMITS			UNITS

OPERATING CONDITIONS

VOLTAGE	VALUE	MIN	MAX	UNITS	VOLTAGE	VALUE	MIN	MAX			UNITS
VOD	31	27	32	V	VSS	3	0	10			V
VOG1	3	1	4	V	VRϕ (high)	11	8	15			V
VRD	19	15	19	V	VϕR (high)	11	9	15			V
VOG2	4	1+VOG1		V	Vlϕ (high)	10	8	15			V
VDD	24	22	26	V							

TEST TEMPERATURES

MEASUREMENT	TYPICAL VALUE	ACTUAL VALUE	UNITS
Dark Signal and White Defects	-100	-100	°C
Others	-100	-100	°C

NOTES

C/R 109713

24 Nov 2010

Appendix B (CCD E2V 44-82, Dummy and ZIF Socket)

The SOXS CCD is storage and packaged as shown in Figure 25.

Figure 25 - CCD E2V 44-82

Figure 26 - CCD E2V 44-82 Package (Dummy)

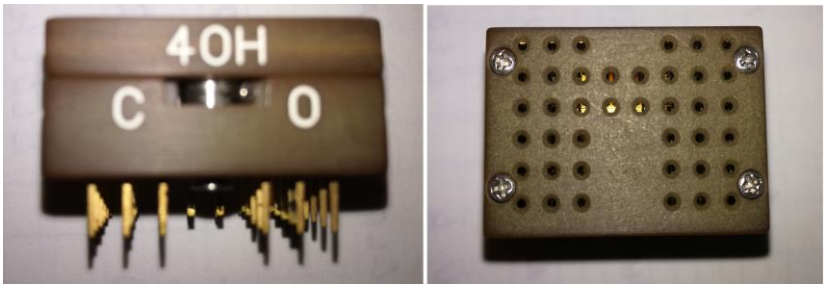

Figure 27 - CCD-ZIF-Socket