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Possible application of FPGA to the MAORY Real Time Computer

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Abstract. MAORY is the post-focal Adaptive Optics module for the European Extremely Large Telescope first light. The baseline of MAORY is to rely upon the use of multiple Laser Guide Stars (6), multiple Natural Guide Stars (3) for wavefront sensing and multiple Deformable Mirrors (DM) for correction (M4/M5, that are part of the telescope, and 2 post focal DMs). The Real-Time Computer is a key sub-system of MAORY. It must collect the measurements from various sensing devices and drive several thousands actuators within high demanding latency requirements dictated by the system performance needs. The FPGA technology has been widely diffused in Real Time Systems due to its low latency and high determinism. Performance evaluation of this technology for the wavefront sensors images calibration and processing is in progress.

Key words. Field Programmable Gate Array, Adaptive Optics, Real Time Computer, European Extremely Large Telescope

1. Introduction

Adaptive Optics (AO) is a technique that allows us to obtain diffraction limited astronomical images using ground based telescopes, despite the presence of the turbulent earth atmosphere. Its functioning is based on the use of sensors, to measure the atmospheric turbulence, and actuators, usually deformable mirrors, to correct the aberrations introduced by it. Typically the AO loop frequency is an range of 100 - 1000 Hz. MAORY (Multi Adaptive Optics RelaY, Diolaiti et al. 2014) is one of the approved first light instruments for the European Extremely Large Telescope (E-ELT, Tamai and Spyromilio 2014). It offers two adaptive optics modes to support the MICADO near-infrared camera(Davies et al. 2010): Multi-Conjugate Adaptive Optics (MCAO) and Single-Conjugate Adaptive Optics (SCAO, Clénet et al. 2016). While SCAO technique is used to optimize the performance on axis and across a Field of View (FoV) of few arcseconds by using only one reference star for the wavefront sensing and one DM for the wavefront correction, MCAO performs a 3D reconstruction of the turbulence through multiple reference stars and apply the correction at different altitudes by the means of multiple DMs. The MAORY SCAO mode development is made jointly by the MAORY and MICADO consortia. In the MCAO mode, that is the most complex configuration, MAORY uses the adaptive mirror M4 and tip-tilt mirror M5 in the telescope and up to two post-focal adaptive mirrors (DM1 and DM2) to achieve high performance with excellent stability of the point spread function across the ∼1 arcmin scientific FoV; in order to ensure high sky coverage, wavefront sensing is based on three Natural Guide Stars (NGS), positioned over a 3 arcmin technical FoV, and on a constellation of up to six artificial reference sources based on the excitation of the atmospheric Sodium Layer, located at an altitude of about 90 km, by the means of a laser. The Sodium Laser Guide Stars (LGS) are projected from the telescope side in a constellation of 2 arcmin angular diameter. The NGS are necessary for the low-order (LO) wavefront sensing to measure the modes which cannot be accurately sensed by the LGSs (like tip-tilt, focus and astigmatism) and the latter are used for high-order (HO) wavefront sensing. Furthermore, the NGS light is also used to monitor the spurious LGS aberrations due to the Sodium layer temporal variation (Schreiber et al. 2014) as well as to monitor the quasi-static aberrations of the optical system. The wavefront sensing is performed in closed-loop with optical feedback from the sensors to the deformable mirrors. Considering the complexity of MAORY, the Real Time Computer (RTC) plays an extremely important role in the overall system optimization design. To combine the signals received from the various wavefront sensors (WFS) at different rates and to compute the commands for the actuators in Real-Time, MAORY needs a very powerful and deterministic computer, characterized by a very low latency. From the knowledge of the incoming wavefront shape, measured by the sensors, it is possible to build a tomographic model of the turbulence and to distribute the correction among the different mirrors, translating the information in commands for the single actuators. A possible technology used to process the pixel data of the WFSs are FPGAs (Munch et al. 2014-Munch et al. 2015-Yang et al. 2015). This technology provides high speed of computation using its massively parallel nature (Rodriguez et al. 2006), that allows a reduction of latency and an increase of the closed-loop bandwidth. For this reason, many telescopes (Valles et al. 2012-Hovey et al. 2010) implement FPGAs in their RTC. This paper is specifically addressed to the first step of the wavefront reconstruction process, in particular the slope measurements, as in Rodriguez et al. (2008). In this regard, a conceptual design for the slope computer using a massive parallel processing with FPGA is presented. Section 2 provides an overview of the RTC preliminary architecture. Section 3 presents the conceptual design of the system embedded in the FPGA, providing also the description of a possible algorithm to calculate the slopes. Section 4 describes the estimation of computational requirements and latency. Finally, conclusions are drawn. We want to stress that the MAORY RTC will be developed in close collaboration with ESO in order to ensure a common approach. Even if throughout this paper we refer to certain technologies or interfaces, ESO will deliver the Common Specifications (architecture, interfaces, technology standards, and verification requirements). This should be therefore considered as a preliminary study, to be shared with ESO, that does not imply the final chose of this technology in the future MAORY RTC.

2. Real Time Computer architecture

The preliminary conceptual architecture of the MAORY RTC is represented in Fig. 1. Different loops, characterized by different frequencies, can be identified: two main loops, running at a maximum frequency of 1 kHz, are devoted to HO (by the means of LGSs) and LO (by the means of NGSs) correction. While the HO correction is distributed between the post-focal MAORY DMs and M4, the telescope actuators will take care of the LO correction (mainly through M4 and M5). The light of the NGSs feeds also the so called 'Reference' WFSs, that run at a slower frame rate (~0.1-1 fps) in order to properly monitor the Sodium layer variations. The slopes computed by the Reference WFS loop are used as slope offsets for the LGS WFSs. Other auxiliary loops are devoted to the correction of the LGS launching facility jitter (fast) and to differential focus variation compensation of the LGS WFS units (slow). The wavefront sensing will rely mainly on the Shack-Hartmann WFS concept, based on the wavefront local slope measurement derived by the x and y shifts of the reference star imaged through a lenset array in a telescope pupil plane. The WFS Processing Units (WPU) receive the WFS pixels, take care of image reconstruction, pixels pre-processing (see below), centroid calculation and gain calibration (to mitigate for WFS non-linearities), and finally provide slopes measurements. Each WFS is associated to a single Unit to optimize parallelization. In Fig. 1, all the WPU relative to a certain loop (LGS, LO NGS or Reference NGS) are grouped in a single box for simplicity. A global tomographic reconstructor receives the slopes from the WPUs and computes the HO and the LO correction to be applied to the various actuators after the proper filtering.

3. Wavefront Process Unit embedded in FPGA

The main objective of this conceptual design is to analyze the viability of WPU based exclusively on FPGAs, considering their parallel processing capability. The major tasks are planned using a modular design in order to allow the simultaneous development of the modules and to add further improvements. In Fig. 2, the modules to implement in the FPGA are described. In this conceptual design, a WFS with Gigabit interface has been considered, but it is possible to use other kinds of communication interface between WFS and WPU, depending on the camera interface (Camera Link, USB3.0 . . .). The data stream, sent by the WFS with Gigabit Interface, is received by Ethernet Interface module which could be either embedded in the same FPGA of WPU or realized with a dedicated hardware (another FPGA or a router). The Ethernet data packets are filtered in this module, in order to extract the pixel data information, which are stored in a FIFO buffer. The Image Reconstruction module reads the data inside the FIFO and builds the pixel data pattern according to the internal clock of the FPGA in such a way to have a synchronization with the next modules. Once the image has been reconstructed, it could be sent to a VGA display, in order to have a real time image without any processing. This is an optional module and it might be removed in order to reduce the amount of chip area occupied. The Centroid Computation module calculates the centroid position of the reference star image in each sub-aperture recovered from the WFS. The pixel calibration module consists in standard pixel processing operations through additions and multiplications, including dark, flat field and background subtraction. Slope computation module is based on the Weighted Centre of Gravity (WCoG) algorithm (Fusco et al. 2004). This algorithm identifies the major probability estimation of the spot position in presence of Gaussian noise. To calculate the x shift of the spot in the (x, y) plane, the following equation can be used:

$$C_{\mathrm{x}} = \gamma * \frac{\sum_{i,j} x_{\mathrm{i,j}} W_{\mathrm{i,j}} I_{\mathrm{i,j}}}{\sum_{i,j} W_{\mathrm{i,j}} I_{\mathrm{i,j}}} \tag{1}$$

where $x_{\mathrm{i,j}}$ is the x coordinate of the pixel (i, j), $I_{\mathrm{i,j}}$ is the intensity of the pixel (i, j) and W is a suitable weighting function. γ is a necessary correction factor in order to compensate for non-linearity effects (Schreiber et al. 2009). The weighting function can be an average image of the reference star image. A similar equation can derived for y component. Therefore, the WCoG complexity, for a $n \times n$ pixles sub-aperture, is about $2 \times n \times n + 1$ multiplications, $2 \times n \times n$ additions and 1 division per axis.

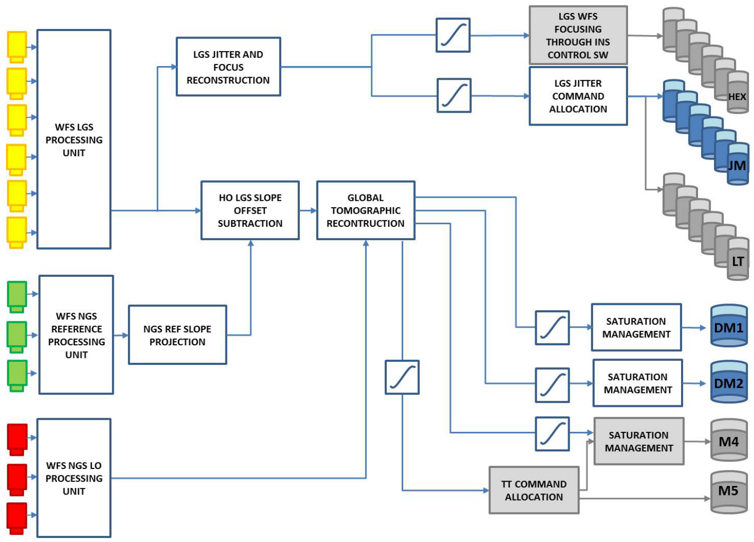

Fig. 1. Conceptual overall control loop diagram for MCAO mode configuration. The actuators depicted in grey belongs to the Telescope Control System. Functional blocks depicted in grey may not be commanded directly by the RTC.

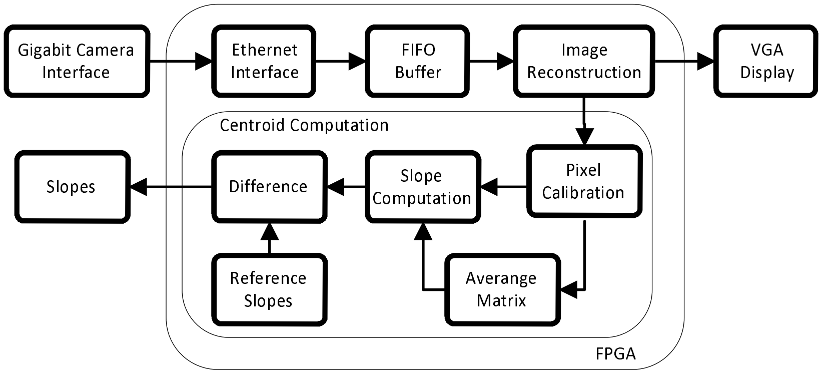

Fig. 2. Diagram of the WPU embedded in the FPGA.

Reference slopes module takes in account the aberrations related to the Sodium profile temporal variability and the open loop compensation of quasi-static aberrations due to the post-focal relay optics and additional closed loop correction by long term filtering of the LGS WFS slopes. Reference slopes should be updated on a regular time basis that depends on the Sodium layer density profile variation rate; a typical frequency range might be 0.1-1 Hz. The algorithm described in this section will be implemented in an WPU experimental prototype, based exclusively on FPGAs, exploiting the MAORY LGS WFS prototype (Patti et al. 2015) that generates the pixel data information.

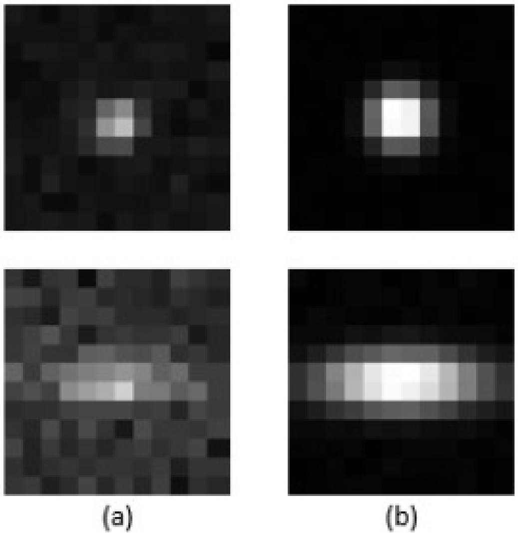

Fig. 3. Instantaneous (2ms) spots (a) and average spot (b) over 500 realizations (nph=500 and RON=3)

4. Wavefront Process Unit Complexity

In this section the complexity of WFS data processing is discussed. The aim is to provide an estimation of computational burden associated to each WFS data processing which will drive the architecture of WPU module and participate to the overall latency.

4.1. Computation requirements

In Table 1 are defined the matrix dimension and the frame rate of the LGS and NGS WFS as in the MAORY current design, in order to calculate the computing requirements for slopes computation. Either for LGS and NGS, the baseline parameters and the goals are reported.

Considering the most demanding case (goal), when a detector of 1760 × 1680 pixels of 10 bits is used for the LGS WFS, the required memory in the WPU is 29.6 Mbits. As total system operation, in order to compute the slopes, 27.8 MFlop are needed, considering also the pixel calibration. In this case, the computing requirements with a frame rate of 1000 fps are: 29.6 Gbps and 27.8 MFlop/s memory bandwidth. To calculate this requirements an LGS WFS of $80 \times 80 \times (\pi/4)$ useful sub-apertures and 20×20 pixels per sub-aperture has been considered. The calculation could be done by using many processing engines in parallel as FPGAs.

4.2. Latency estimation

The time available for the RTC to compute the AO is a critical specification directly impacting the required computational power. In Fig. 4, the time model for the open loop AO chain is depicted. In this work only the RTC latency, defined as the maximum time allotted for RTC computation, is analyzed. RTC Latency is defined as the time elapsed between the reception of the first WFS readout data by the RTC and the moment at which the last actuator command is sent to DM. The computation time T_{RTC} is calculated as follows:

$$T_{RTC} = T_{read} + \tau \qquad (2)$$

where T_{read} is the WFS readout time that accounts a potential time slot to be used by the RTC for computation, while τ is the maximum acceptable RTC computation delay after WFS

Table 1. Dimension matrix and frame rate for LGS and NGS WFS

WFS	Matrix size	Maximum Frame Rate (fps)
LGS(baseline)	(880*840)10bits	700
LGS(goal)	(1760*1680)10bits	1000
NGS(baseline)	(320*256)32bits	1000
NGS(goal)	(500*500)32bits	2000

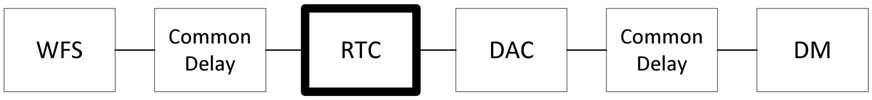

Fig. 4. Time model for the open loop AO chain.

readout is complete. τ is a summation of latencies related also to the tasks that follows the WPU represented in Fig. 1. In particular, the tomographic reconstruction will be probably the most demanding task in terms of computational power and latency.

$$\tau = \tau_{WPU} + \tau_{rec} + \ldots \quad (3)$$

τ_{WPU} considers only the module involved directly with the slopes computation. The latency evaluation in table 2 for the WPU has been made considering one cycle minimum for adding and multiplying operations. In addition, a 200 MHz clock has been used, in order to evaluate the latency in absolute time. The latency has been evaluated for a single sub aperture. In MAORY phase A, the requirement regarding total latency had a goal of one frame delay (1-2 ms, depending on the loop frequency). In this study, the estimated WPU latency is negligible in comparison with the overall MAORY requirement.

5. Conclusion

The conceptual approach of a FPGA based wavefront process unit for MAORY instrument has been presented. The main complexity features have been evaluated, clearly showing the feasibility to embed WPU in the FPGA. The main concept is the use of the sub apertures as a grid for the parallel processing.

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Table 2. Estimated latency for the WPU

Module	Latency(clock cycle)	Latency (ns)
Pixel Calibration	4	20
Slope Computation	10	50
Other	4	20
TOTAL(τ)	18	90