Forming-free and self-rectifying resistive switching effect in Anodic Titanium Dioxide-based Memristors

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Abstract - The paper presents the resistive switching of electroforming-free Ti/anodic-TiO_2/Cu memristors. Anodic TiO_2 thin films were prepared by anodizing Ti layers. Microscale devices were fabricated by direct laser-assisted photolithography. Experimental results showed a bipolar and self-rectifying behavior of the devices, which could be useful for crossbar array configurations. Moreover, a gradual resistive switching of the devices in both directions was observed, indicating the presence of multi-level resistance states.

Keywords—Memristor; RRAM; Anodizing; Titanium Dioxide; Multistate resistance; Crossbar array.

I. INTRODUCTION

Electronics industry has tremendously improved the computational power of its products, because of the development of increasingly sophisticated miniaturization techniques. However, this process has almost reached its physical limit, and alternative techniques, such as quantum computing, that could potentially boost computer and information storage performances are still far from being applied to everyday life [1]. For this reason, many research groups have focused their attention on novel devices that although still employing current technologies, may improve performances in terms of density, speed, and power consumption. One of the devices promisingly capable to maintain the development rate of the last decades and that could replace current flash and CMOS-based memories is the memristor. This device is constituted, in its basic form, by a simple metal/insulator/metal structure which, if proper excited by electric fields, shows a reversible and repeatable resistive switching. This means that such a device can be used as non-volatile memory cell [2]. The switching effect takes place inside the insulator and consists in the formation and rupture of conductive filaments [2], [3] between the top and the bottom contacts. As a result, the I-V characteristic is a non-linear curve known as pinched hysteresis. Initially, the device is normally in the so called OFF state or high resistance state (HRS), characterized by the native oxide resistance ROFF, usually very high.

If a proper SET voltage V_{SET} is applied to the metal contacts, an abrupt change in the resistance occurs. The device is then switched to the ON state, or low resistance state (LRS), where it shows a lower resistance R_{ON}. Decreasing the applied voltage does not immediately restore the OFF state. In fact, a RESET voltage V_{RESET} has to be reached to ensure the transition from the LRS to the HRS.

The physical mechanisms behind the memristor operation are different [3]. One of the most studied switching mechanism, related to the filament-type memristor, is ascribed to the migration of ionic species through the insulator layer, under the influence of an electrical stimulus. In a metal/insulator/metal structure, the ionic species are randomly spread within the insulator layer. If a proper electric field is applied, the ionic species start to migrate eventually resulting in the formation of conductive filaments between the metal contacts. The nature of the species that form the conductive path depends mainly on the employed materials. In particular, by using metal oxides as insulator and inert metals as contacts (e.g. Pt), the resistive switching was found to be due to the migration of the oxygen vacancies within the oxide layer [4]. On the other hand, if the metal contacts are not inert (e.g. Cu, Ag), also metal ions can migrate through the insulator to form metallic conductive filaments, also called metallic bridges [5].

Normally, an electroforming cycle is necessary to activate the switching properties of resistive memories. Such process consists in the introduction or rearrangement of ionic species inside the insulator from the nearby environment, usually stimulated by the application of an external electric field. This process, however, requires often a much higher bias voltage, which may lead to unpredictable resistance states [6]. Nevertheless, not all the materials require the forming process, especially when enough imperfections or impurities for filaments formation are already present [3]. This simplify the practical utilization of the devices because an additional technological process step is avoided.

One of the most interesting property of memristors is the ability to retain the induced resistance value (R_{ON}, R_{OFF} or intermediate resistance values) indefinitely in time. Thus, memristors may be employed as non-volatile, single or multi-level memory element characterized by a very simple structure, scalable down to nanometer range, and characterized by low power and high-speed operation, as well as good compatibility with CMOS technology. The most common and simplest method to obtain addressable nanoscale memory elements is the so-called crossbar array structure [3]. As it can be seen in Fig. 1, it consists of two perpendicular sets of nanometric electrodes separated by an insulating material, resulting in the formation of a memristor for each cross-point [7]. The fabrication of such a structure is possible with several technologies, such as nanoimprint lithography [8] and electron beam lithography [9], and allows scaling memristors down to the nanometer scale, keeping at the same time external access to each nano-device. Moreover, memristor crossbar arrays are able to integrate computation and memory operations as in the brain [10]. A further improvement in terms of memory density can be obtained, in addition, by implementing a 3D version of the crossbar structure, which can potentially lead to terabit-scale memory devices [11], [12]. Moreover, the multi-level operation, doable with memristors, could allow storing more data in one single memory element, and the crossbar configuration could then be employed to further improve the scalability of such simple devices, still exploiting the already well-established industry fabrication methods [13].

Among all the oxide materials potentially employable for memristor fabrication, titanium dioxide is one of the most promising because of its abundance in nature and the very good already reported performances [2]. However, the fabrication methods of TiO_2-based memristors rely usually on expensive and high power consuming techniques, such as atomic layer deposition (ALD) and RF sputtering [2], [14]. A much simpler and cheaper technique for obtaining titanium dioxide films for memristor applications is anodizing [15], [16]. It is in fact carried out at room temperature and it is a very versatile technique for preparing oxides of different thickness and composition by properly selecting the metallic substrate and the electrochemical conditions. Indeed, anodizing has already been used for the fabrication of resistive switching devices based on HfO_2, Nb_2O_5 [17] and TiO_2 [18], [19].

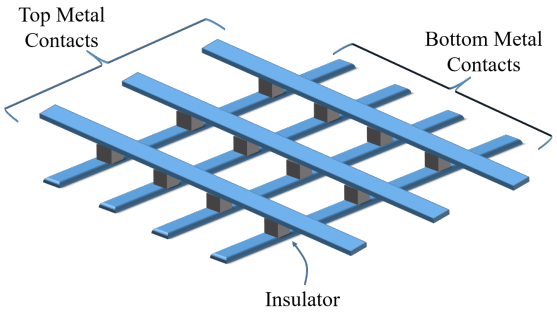

Fig. 1. Sketch of a crossbar array configuration employed for the fabrication of nanoscale memory elements. Parallel nanometer electrodes acting as bottom and top metal contacts (blue) are fabricated perpendicularly to each other. The insulator layer (dark grey) sandwiched between the two set of parallel electrodes constitutes the active layer of the memristors. Each cell can be generally addressed independently by an appropriate selection of a word and bit line. The current, however, can flow through different cells, causing the so-called sneak path problem.

In this work we present forming-free anodic TiO_2-based memristors showing a strong self-rectifying behavior suitable for the implementation in a crossbar-array configuration. Moreover, a discrete change in the conductivity of the devices when a constant voltage is applied is also observed and discussed.

II. Experiments

Ti (80 nm)/anodic-TiO_2 (8 nm)/Cu (300 nm) 10 × 10 μm^2 memristors were fabricated by direct laser maskless photolithography. A schematic of the fabricated devices is reported in Fig. 2. The 8 nm-thick TiO_2 was prepared by anodizing in potentiostatic mode (5 V, 100 s) a 80-nm-thick titanium thin film previously deposited by e-beam evaporation onto a glass substrate. The anodizing process, performed by using a Pt net as counter-electrode in 1 M H_3PO_4 aqueous solution, was characterized by a current density decreasing with the increase of the polarization time. More details on the fabrication process can be found in [18].

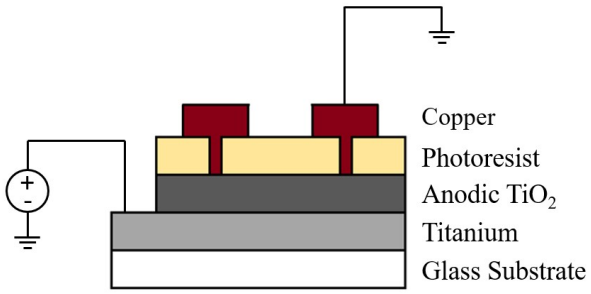

Fig. 2. Schematic representation of the fabricated memristors. The voltage source is connected to the bare titanium film that acts as the common contact for all the devices. On top of the anodic TiO_2 layer a photoresist film is patterned and hard baked to form the microscale (10 × 10 µm²) vias afterwards filled with copper. Large copper pads are grounded to perform the electrical characterization.

All devices have been electrically characterized at room temperature by means of a Versastat 3 (Princeton Applied Research) connected to a Karl Süss probe station. The voltage was applied to the Ti common contact while the top copper contact was grounded, as depicted in Fig. 2. The voltage sweep was set between − 2 V and + 2 V with a scan speed of 0.5 V/s. A further electrical characterization has been carried out by applying a steps-like voltage to the devices by means of another setup made of a Philips PM5133 signal generator as a voltage source, a Tektronix TDS 1012 oscilloscope for data acquisition and a 1.2 MΩ resistor, connected in series with the device under test, for calculating the current values.

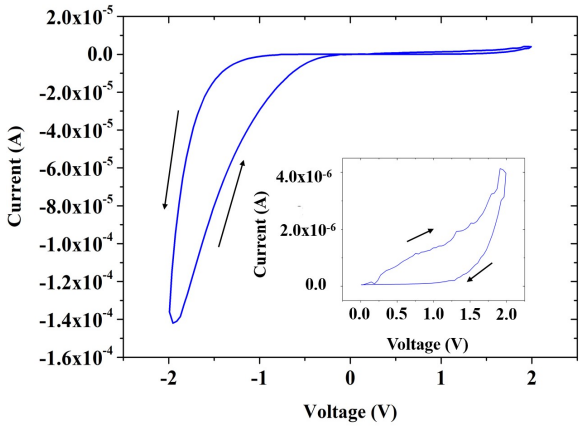

Fig. 3. Typical current-voltage characteristic of a 10 × 10 µm² Ti/anodic-TiO_2/Cu memristor with 8 nm-thick oxide. The arrows show the voltage sweep directions. The inset zooms in the curve for positive voltages.

III. RESULTS AND DISCUSSION

A typical I-V characteristic obtained from a 10 × 10 µm² memristor is reported in Fig. 3. The arrows indicate the switching directions. As it can be seen, the device presents an asymmetric, bipolar hysteresis, with a pronounced rectifying behavior. The V_{SET} necessary to the transition from the HRS to the LRS is found to be negative and equal to ~ − 1 V. The V_{RESET} is positive and equal to ~ 1.75 V. Due to the large difference in current scale between negative and positive voltage sweeps, an inset has been introduced in Fig. 3 to clearly display the current evolution during the positive voltage sweep.

The main conduction mechanism in this device may be

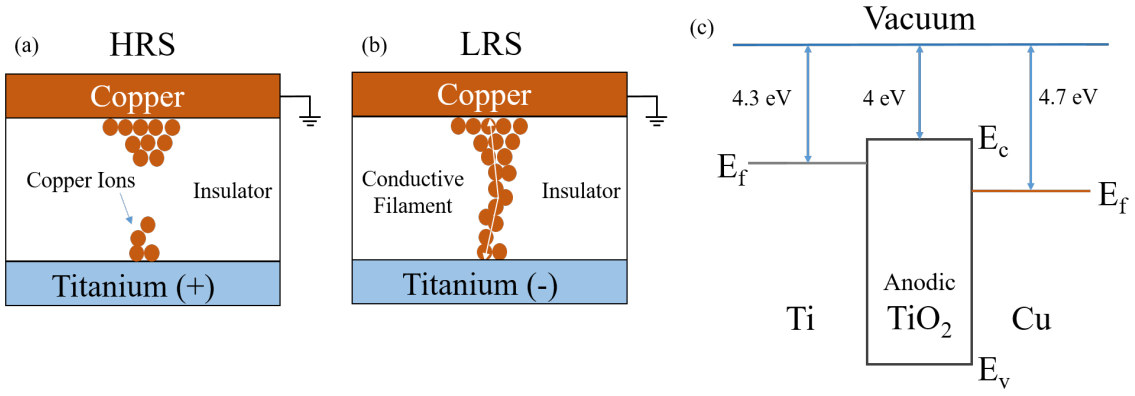

Fig. 4. Schematic illustration of the conductive filament formation in the Ti/anodic-TiO_2/Cu structure. In a) is depicted the HRS or OFF State: the filament constituted by copper ions is not formed yet or broken during a previous switch from the LRS to the HRS, thus the conduction inside the insulator layer is not allowed. In b) is depicted the LRS or ON state: the filament formation occurs after the application of a negative potential to the titanium bottom electrode, forming a conductive path made of copper ions, that allows current to flow between the metal contacts. In c) is shown an approximate sketch of the energetics of the Ti/anodic TiO_2/Cu structure.

ascribed to the formation and rupture of copper ions filaments [20]-[22]. However, because of Ti oxidation during device operation, the small barrier height at the Ti/TiO_2 interface (see Fig. 4) may collapse during the negative voltage sweep, producing an ohmic contact which favors, together with the copper filaments formation, the transition from the HRS to the LRS [2], [23], [24]. Conversely, during the positive voltage sweep, copper filaments dissolve, leading to the transition from the LRS to the HRS. Moreover, in this case, the Ti/TiO_2 interface behaves as a non-ohmic contact and limits together with the Cu/TiO_2 barrier the current down to the μA scale. The rectifying behavior for positive voltages should mostly due to the Cu/TiO_2 interface that forms a Schottky diode, as reported not only for TiO_2-based memristor [24] but also for other oxides, such as HfO_2 [25], [26], ZnO [27], [28], Al_2O_3 [29], [30], and CeO_2 [31].

The strong rectifying behavior shown by our devices could be profitably implemented in a crossbar array configuration for solving the sneak path issue, typical of these structures. The sneak path influences the readout operation performed on a cell operating in the HRS surrounded by, at least, three cells operating in the LRS. In particular, the three surrounding LRS cells create a conductive path that electrically shorts the top and bottom contacts of the HRS cell, thus resulting in a misreading of the stored data. Normally this problem is solved by integrating an extra diode together with the memory cell. A self-rectifying memristor owns already this diode capability, and can therefore surely both simplify the fabrication process and decrease the area of a crossbar structure [7].

In order to gain deeper insight on the behavior of our devices, a study was carried out by applying step-like voltages. In Fig. 5 is shown the hysteresis loop obtained after

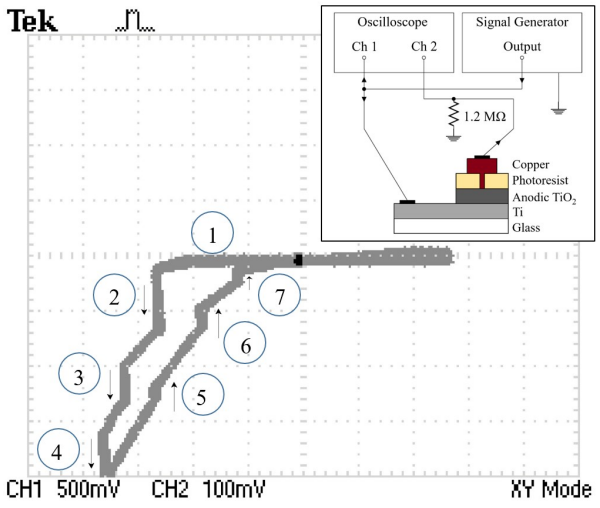

Fig. 5. Device response after step-like voltage stimuli. The horizontal axis indicates the applied voltages (scale 500 mV/div), while the vertical axis indicates the voltage measured on the reference 1.2 MΩ resistor (scale 100 mV/div). In the inset, a schematic of the oscilloscope-based characterization setup is shown.

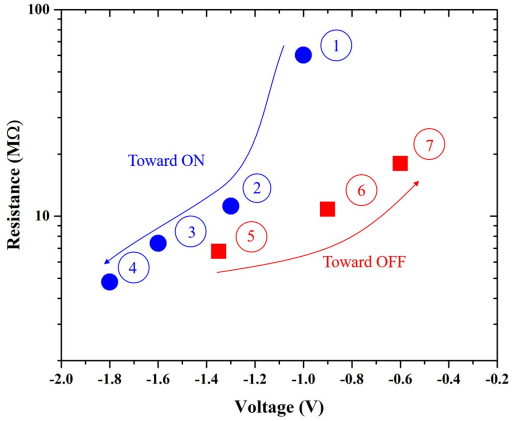

Fig. 6. Resistance intermediate states obtained for increasing (dots) and decreasing (squares) step-like voltages. The numbered circles represent the same points depicted in Fig. 5 at which the resistances were calculated. Increasing voltage steps lead to lower and lower resistances, and finally to the LRS, whilst decreasing voltages lead to a small variation of resistance.

such experiment. The inset reports a schematic of the setup employed for this measurements. If the device is in its OFF state (see point 1 of Fig. 5), by applying a negative voltage step at −1.3 V, a switching towards the LRS is noticed (see point 2 of Fig. 5). During the transition from the HRS to the LRS, the current starts increasing, while the voltage is kept constant, until it stabilizes at a certain value. If the voltage is further (negatively) increased, others switches are observed (points 3 and 4) toward higher currents (and lower resistances). After the complete transition to the LRS, a slight decrease of the voltage to a lower step (lower than the one necessary to the complete transition from the LRS to the HRS) causes a decrease of the current, but the resistance is almost constant (point 5). Reverse scan to 0 V is then characterized by quasi linear behavior, with more constant currents for applied voltage steps (points 5, 6 and 7) and a resistance which slightly increases with decreasing voltage steps. The sequence of these intermediate resistance levels obtained for negative voltages is plotted in Fig. 6, where the dots represent the intermediate resistance states toward the ON state, whilst the squares represent the resistance states in the ON state for negative voltage steps toward 0 V, and then toward the OFF state (obtained for positive voltages). Because of the strong rectifying behavior of our devices, it was not possible to conduct the same experiment by applying positive step-like voltages, and only a flattened loop was visible. The above described behavior, observed during sep-like voltage stimuli, could be explained as follow: during the switching from the OFF state to the ON state, a slow conductive channel formation occurs after a particular step voltage is applied to the device. Once all channels related to the temporary applied electric field are formed, the current (and then the resistance)

stabilizes, until another voltage step is applied. The process ends up after the full transition to the LRS has been reached, implying that all the possible conductive channels were formed. The gradual switching gives then rise to discrete resistance states between R_{OFF} and R_{ON}, thus allowing potentially the possibility to store more information per device.

IV. Conclusion

We have presented here low cost, forming-free and self-rectifying memristor devices potentially capable of multi-level memory retention. 8 nm-thick anodic TiO_2 was prepared electrochemically by anodizing a Ti thin film deposited by electron beam evaporation. Microscale Ti/anodic-TiO_2/Cu memristive devices were then fabricated by direct laser-assisted lithography. Electrical characterization of the devices demonstrated the presence of a memristive behavior with a strong rectifying characteristic suitable for avoiding the sneak path issue normally present in crossbar array structures. Further electrical characterizations, consisting of stress tests at constant step-like voltages, revealed that the devices show multiple discrete resistance states.

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