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The SKARAB Board in the Framework of Single-Dish Radio Astronomy

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The Square Kilometer Array Reconfigurable Application Board (SKARAB) is a Xilinx Virtex-7 FPGA-based platform designed for the MeerKAT array, to be used for both F- and X/B-engines. The MeerKAT F-engine receives digitized data, thus no samplers are required on the SKARAB-based platform. Among the alternative options available, a high-performing ADC mezzanine board can be used in conjunction with the SKARAB, which allows four 1.4-GHz-wide input channels to be digitized and processed. In this paper, we outline how the SKARAB has been successfully used for single-dish applications including imaging, spectroscopy, and spectro-polarimetry.

Keywords: SKARAB; spectrometer; FPGA.

1. Introduction

SKARAB is an acronym for Square Kilometer Array Reconfigurable Application Board, a digital FPGA-based platform that was engineered and built by Peralex Electronics (Pty) Ltd[(a)] in South Africa, in close collaboration with the SARAO[(b)] (South African Radio Astronomy Observatory) institute. Specifically, Peralex won a nationwide tender to design and manufacture 300 SKARAB units for the MeerKAT[(c)] precursor to the SKA radio telescope in South Africa, which is an array composed of 64 13.5-m dishes. Originally conceived for processing data produced by an array of radio telescope antennas, SKARAB is a networked, FPGA-based computing node in a 19″ 1U form factor that is not application-specific, and is thus suitable for single-dish applications as well.

In the field of the digital signal processing in radio astronomy, the Collaboration for Astronomy Signal Processing and Electronics Research[(d)] (CASPER) stands out as an open-source hardware and software consortium that was devised with the purpose of streamlining and simplifying the design flow of radio astronomy instrumentation. CASPER has a specific focus on Xilinx (now AMD) FPGAs. A graphical environment relying on a Matlab/Simulink framework provides a modern user-friendly design tool, and an extensive DSP library is

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[a]https://www.peralex.com.

[b]https://www.sarao.ac.za/.

[c]https://www.sarao.ac.za/science/meerkat.

[d]https://casper.berkeley.edu/.

provided along with all of the existing Xilinx blocksets.

In the past decade Hickish *et al.* (2016), many "CASPERized" boards were designed and commercialized. Among them are the well-known ROACH (Reconfigurable Open Architecture and Computing Hardware) and ROACH2, which was mass-adopted in radio astronomical facilities, including single-dish antennas like the Green Bank (Prestage *et al.,* 2015), Effelsberg,[e] Parkes (Price *et al.,* 2018), Sardinia (Melis *et al.,* 2018), and others. With the advent of high-performance off-the-shelf hardware, CASPER is slowly moving away from designing custom digital boards. The new trend is to exploit commercial hardware, for instance, the Xilinx Alveo accelerator cards and the Xilinx RFSoC evaluation kits (ZCU111 and ZCU216).

SKARAB is the last piece of hardware specifically conceived and manufactured for use in the CASPER environment. SARAO championed the full integration of the board into the CASPER environment, also called "Toolflow," and we subsequently decided to explore the potential of SKARAB in the framework of single-dish astronomy. In this paper, we describe our work to make SKARAB an effective solution in the field of single-dish radio astronomical applications. Specifically, we will describe a few digital spectrometers with different bandwidths and numbers of channels which are planned to be used at the Italian radio telescopes.

The paper is organized as follows: In Sec. 2, we briefly list the SKARAB major features and in Sec. 3, we describe the scientific benefits provided by these features in single-dish applications. In Sec. 4, we outline the FPGA firmware that was designed and in Sec. 5, the SKARAB FPGA resource utilization for each developed design. In Sec. 6, we give an overview of the hardware/software employed to test the various SKARAB firmware and in Sec. 7, we discuss the on-field results that we achieved at the Medicina 32-m radio telescope,[f] located near Bologna in Italy, by also comparing them with the literature. Finally, in Sec. 8 we present our conclusions.

2. Description of SKARAB

SKARAB[g] is an FPGA-based platform that represents the next generation/successor to the ROACH2[h] platform, conceptualized by the Square Kilometer Array South Africa (SKA-SA).

Central to the SKARAB motherboard is a Xilinx Virtex 7 690T FPGA, which provides 1,927 pins, $80 \times$ SERDES, 693,120 Logic Cells, $1{,}470 \times 36$-kb RAM Blocks (approximately 53 Mb), and 3,600 DSP Slices. The board has four mezzanine sites, each having a 400-pin FCI Meg-Array connector; 16×10-Gbps SERDES are available from the FPGA for each mezzanine slot.

Unlike previous CASPER boards (iBOBs, BEE2s, ROACH1s, and ROACH2s) which use a PowerPC for communicating with the FPGA, SKARAB uses a lightweight on-FPGA softcore MicroBlaze processor, which is reloaded whenever the FPGA is reprogrammed. Thus, there is no need for managing boot servers and Linux file systems which adds system complexity; the entire platform can be managed remotely, including upgrading the processor firmware over the network. Specifically, reconfiguration data is transferred from the host to the SKARAB over the network, the softcore MicroBlaze checks the integrity of the data, and if valid, stores it in an external (to the FPGA) SDRAM memory device. Once the entire FPGA image has been transferred and fully stored in the SDRAM memory device, a reconfiguration of the FPGA is triggered. Another non-volatile FPGA makes the SDRAM memory device appear as a NOR flash to the FPGA, allowing the FPGA to boot from the SDRAM memory device. The advantage of this process is that it does not wear out a non-volatile flash device. Since the softcore MicroBlaze checks the reconfiguration data received over the network, the process is robust against network failures. Any packet loss or incomplete configuration would be detected. Also, if somehow something does go wrong with the reconfiguration, a "golden" boot image is stored in a non-volatile flash device, so that the SKARAB can be recovered by power cycling the board.

Up to four mezzanine cards can be simultaneously accommodated in a SKARAB, each plugged into a Meg-Array connector. Three kinds of

[e] https://www.mpifr-bonn.mpg.de/4648370/pulsar_instruments.
[f] http://www.med.ira.inaf.it/parabola32m.html.
[g] https://github.com/casper-astro/casper-hardware/blob/master/FPGA_Hosts/SKARAB/README.md.
[h] https://github.com/casper-astro/casper-hardware/blob/master/FPGA_Hosts/ROACH2/README.md.

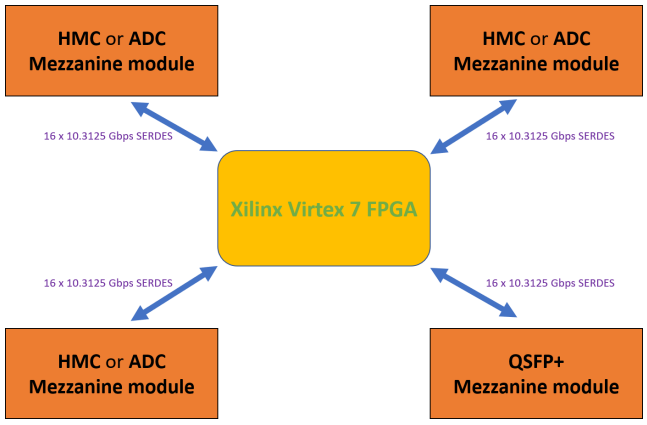

Fig. 1. Simplified block diagram of the SKARAB board. The centerpiece of the board is a Xilinx Virtex-7 XC7VX690T FPGA, around which up to four mezzanine cards are allowed to be accommodated in the four available Meg-Array connectors. In principle, all the three kinds of mezzanine cards can be placed in any slot; however, the CASPER Toolflow only supports a single QSFP+ card, also used to control the SKARAB. The other three slots can be populated with a combination of HMC and ADC cards.

ADC Sample Rate	ADC Decimation Rate	FPGA Decimation	FPGA Resampler	Output Sample Rate	Output Type
2800	1	1	1	2800	Real
2560	1	1	1	2560	Real
2560	1	1	0.8	2048	Real
3000	4	1	1	750	Complex
2560	4	1	1	640	Complex
2560	4	1	0.8	512	Complex
3000	8	1	1	375	Complex
2560	8	1	1	320	Complex
2560	8	1	0.8	256	Complex
3000	16	1	1	187.5	Complex
2560	16	1	1	160	Complex
2560	16	1	0.8	128	Complex
3000	16	2	1	93.75	Complex
2560	16	2	1	80	Complex
2560	16	2	0.8	64	Complex
3000	16	4	1	46.875	Complex
2560	16	4	1	40	Complex
2560	16	4	0.8	32	Complex
3000	16	8	1	23.4375	Complex
2560	16	8	1	20	Complex
2560	16	8	0.8	16	Complex

Fig. 2. Details of sample rates provided by the two ADC yellow blocks. First three rows refer to the Bypass mode (output type real): default ADC sample rate is 2,800 MSample/s, which can be reduced to 2,560 MSample/s by changing the ADC clock; to achieve 2,048 MSample/s, a 4/5 FPGA resampling (fourth column) is required. From the fourth row, the DDC modes are shown. ADC Decimation Rate specifies the three possible decimation cases implemented in the ADC unit. The FPGA decimation and the 4/5 resampler are implemented in the FPGA fabric. These three parameters are specified in the Python method which initializes the ADC.

mezzanine cards are currently available: 4 × 40-GbE Quad Small Form Pluggable (QSFP+), a 4-GB Hybrid Memory Cube, and an ADC with four 1.4-GHz-wide signals. This allows a trade-off between memory, I/O capacity, and number of analog RF signals. Figure 1 shows a simplified block diagram of the board in which the allowed interchangeability of the three kinds of mezzanine cards is shown.

- The QSFP+ mezzanine card provides the SKARAB with 40-GbE functionality. It consists of four 40-GbE QSFP+ ports. The QSFP+ mezzanine card can be placed in any mezzanine slot, but the CASPER Toolflow only supports one QSFP+ card per board. This limits the maximum bandwidth to 160 Gbit/s. A 40-Gb link is required to control the board, thus this mezzanine has to be installed in any case, as shown in Fig. 1. Further details can be found elsewhere.[i]
- The HMC mezzanine card designed for the SKARAB is fitted with a single Micron HMC MT43A4G80200 — 4-GB 8H DRAM stack device, which uses 16×10-Gbps SERDES lanes to the FPGA per mezzanine site. The HMC yellow block designed by CASPER makes provision for two (2 and 3) of the four (1, 2, 3, 4) links, so only half of the memory can be accessed directly. Each link uses 8×TX/RX GTH full duplex lanes rated at 10 Gbps each, thus each link can handle 80-Gbps throughput. FLIT (floating Unit) protocol with 128 bits (64-bit header and 64-bit tail) is used, limiting the actual throughput to 40 Gbps for each link, both in read and write.
- The SKARAB ADC mezzanine board has four analog channels. Each channel can be sampled at a maximum rate of 3 GSPS. The sampling is performed by either two dual-channel TI ADC32RF80[j] ADCs or two dual-channel TI ADC32RF45[k] ADCs depending on the PCB build configuration. The board also contains a clock generation PLL which provides sampling clocks to the ADCs locked to an external reference clock. Both the ADC32RF45 and ADC32RF80 include a Digital Down-Converter (DDC) for each input. The ADC32RF45 additionally allows the DDCs to be bypassed to provide the full

[i] https://github.com/ska-sa/skarab_docs/blob/master/per-alex/HDD-123801-01_QSFP%2B_Mezzanine.pdf.

[j] https://www.ti.com/product/ADC32RF80.
[k] https://www.ti.com/product/ADC32RF45.

bandwidth of the ADC; all of the designs described in this paper refer to the latter case. Two different yellow blocks (described in Secs. 4.1.1 and 4.1.2) are provided in the CASPER Toolflow to control the mezzanine in bypass and DDC modes, respectively. The DDC yellow block includes an optional decimation filter implemented in the FPGA logic, to further reduce the band or resample it to a different sampling rate. By changing the ADC sample rate, the decimation factors, and including an optional 4/5 resampler, a wide set of bandwidths that satisfy all of the scientific requests are available. These modes are listed in Fig. 2, along with the details about how each output sample rate provided by the ADC yellow blocks is achieved.

3. Scientific Motivation to Use the SKARAB in Single-Dish Observations

Although ROACH2s are continuing to guarantee cutting-edge science in all of the aforementioned telescopes (GBT, Parkes, Effelsberg, and SRT), its technology is no longer supported and marketed. In addition, the development environment requires very old Linux and Matlab versions, as well as the Xilinx ISE that has now been abandoned in favor of the more modern Vivado and Vitis tools.

As a consequence, we have identified SKARAB as one of the possible boards — that are fully integrated into the CASPER environment — to replace ROACH2. This also takes advantage of the higher FPGA resources available on the Virtex-7 chip, the improved I/O capacity, the greater off-chip memory (up to 12 GB) the SKARAB can be equipped with, as well as the high-performing (especially in terms of high dynamic range) ADC mezzanine boards specifically designed for SKARAB. These features allow a number of possible scientific improvements.

3.1. *High-performing ADC mezzanine card*

In terms of scientific improvements, the SKARAB coupled with the ADC card provides a relevant step forward:

(1) The total input bandwidth which can be handled by SKARAB is very large, which of course increases the overall sensitivity. Up to three ADC mezzanine boards can be simultaneously accommodated into a single SKARAB, which means a total bandwidth of 16.8 GHz (divided into 12 chunks 1.4-GHz wide). With a specific FPGA speed grade request, each input signal band can be widened from 1.4 GHz to 1.5 GHz: in this case, the overall bandwidth becomes 18 GHz.

(2) Spectroscopy is one of the major applications of the SKARAB platform. The ADC DDC functionality allows one to narrow the bandwidths to achieve better frequency resolution, in the kHz range. As shown in Fig. 2, different narrow bandwidths (750, 640, 375, 320, 187.5, and 160 MHz) can be achieved by exploiting processing carried out on the ADC board itself (namely, without using FPGA resources). FPGA decimation can be used to further narrow the bandwidth or if the resampling is used to get one of the bandwidths that require it, but this comes at the expense of reducing the FPGA resources available for further processing.

(3) As discussed in Secs. 4.1.1 and 4.2.1, dynamic range is very high thanks to the number of bits (from 12 bits to 16 bits) used to code the digital samples. This is extremely useful for conducting solar studies (in which the total intensity is particularly high), as well as when we operate at low frequency, where the RF interferences (RFI) can be strong. Pulsar search/timing and Fast Radio Bursts studies are typically carried out at low frequency and therefore are those which benefit most of this increased RFI immunity.

(4) The ADC mezzanine board provides a general-purpose nine-pin LEMO I/O connector. We use one of these pins to drive a fast noise injection signal for calibration procedures. The ADC yellow block allows both the options to drive this signal externally and to receive it from outside.

3.2. *Number of FFT channels that can be implemented on board*

The SKARAB FPGA has a significant (53 Mb) amount of Block Random Access Memory (BRAM). By combining this feature with the FPGA fabric technology (28 nm) which helps with the timing closure, up to 65,536 Fast Fourier Transform (FFT) channels can be smoothly achieved for at least two polarizations. Such a high number of FFT channels allows one to implement on-board zoom modes for

high-frequency spectroscopic observations, for instance, for astrochemistry observations.

Another SKARAB feature which can be exploited to implement spectrometers with a larger number of FFT channels is the off-chip HMC 4-GB-wide memory. The large I/O bandwidth of the HMC module, up to 80 Gbps, allows for the implementation of wideband high-frequency-resolution spectrometers, which is helpful for large spectroscopic surveys, i.e. to cover a large portion of the sky looking for narrowband emission at unknown frequencies. Specifically, we propose an architecture with a two-stage polyphase filter bank composed of a first-stage 1k-channel filterbank followed by a corner turn (matrix transpose) logic which collects these spectra, simultaneously presenting one channel at a time to one or more second-stage 1k-channel PFBs. The final result would be a spectrometer with 1 million channels on a bandwidth of 512 MHz or 1,024 MHz, thus with frequency resolution suitable for a spectroscopic survey.

Alternatively, digitized bandwidth can be handled and processed by a GPU cluster to achieve fine channelization; in the next subsection, we outline how the SKARAB 40G technology can help in this regard.

3.3. *Base-band recording/post-processing mode with wide uniform bandwidths*

Several scientific applications, like VLBI (Very Long Baseline Interferometry), pulsar timing, and high-frequency-resolution spectrometers to be implemented on GPUs, require that the data be just digitized, packetized, and sent out to a recorder or post-processed in real time. For these applications, it is very useful to be able to transmit the widest possible bandwidth on a single link. Each of the 40G links of the SKARAB allows transmitting a dual-polarization signal sampled at full bandwidth, with 6 bits per sample, or a single unprocessed full precision (14 bits per sample) signal. This means that all the four input signals provided by the ADC mezzanine board can be digitized and sent packetized as they are. Current CPU/GPU-based acquisition systems are able to process such whole (1–2 GHz) bandwidths in real time.

If the bandwidth needed to be recorded/post-processed exceeds the available I/O throughput of the post-processing system, a polyphase filter bank is usually used to split up the bandwidth into sub-bands of suitable bandwidth, subsequently sent out to different parallel processing units. Even in this case, the total transmitted bandwidth must fit in the available link bandwidth. The 160-Gb/s aggregate bandwidth allows up to 10 GHz of total observed band with 8-bit resampling, e.g. eight signals with 1.2 GHz of effective band.

4. The Digital Signal Processing Firmware Designed for the SKARAB

4.1. *A full-Stokes 2,048-channel spectrometer 1.4-GHz wide*

We designed a wideband spectrometer which is capable of handling two input signals 1.4-GHz wide and provides four spectra with 2,048 channels, suitable for spectral–polarimetric imaging applications. Figure 3 shows the (somewhat conventional) block diagram of the spectrometer.

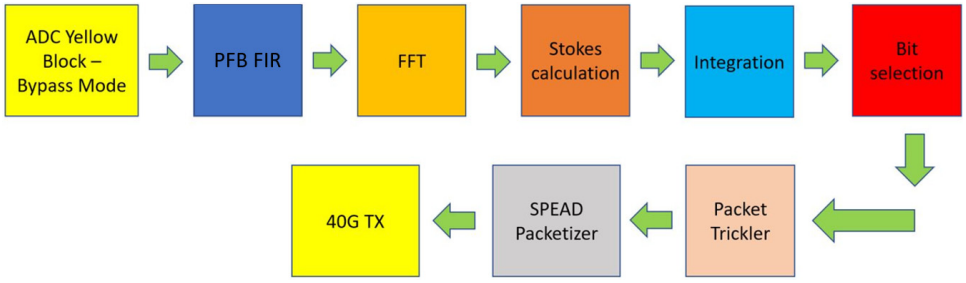

Fig. 3. (Color online) Block diagram of the wideband (1,400 MHz) spectrometer. The green arrow represents the data flow for the two processed polarizations. The ADC bypass yellow block provides 16 parallel samples for the two signals of interest, a polyphase filter followed by an FFT engine provides the two signals in the frequency domain and the Stokes calculation stage provides both auto- and cross-correlations. Signals are then summed up channel-wise for a user-specified time in the Integration block, and rescaled in the Bit Selection stage. Finally, data are bufferized (Packet Trickler), packetized (SPEAD Packetizer), and sent out (40G TX) toward a single 40G cage of the QSFP+ mezzanine card.

4.1.1. *ADC yellow block and RMS calculation*

The ADC bypass yellow block (the first block in Fig. 3) provides 16 parallel real sample outputs for each of the four input signals. The highest (which is also the standard) sample rate that can be supported for each signal is 2,800 MS/s at a clock rate of 175 MHz, thus the maximum bandwidth which can be achieved is 4×1.4 GHz, for a total of 5.6 GHz. Most software for pulsar and fast transient studies require a sampling period which exactly divides 1 s. This is not the case for a sampling rate of 2,800 MS/s decimated in a 2,048-channel spectrometer. Thus, two alternative sample rates have recently been added: 2,560 MS/s and 2,048 MS/s. Here, 2,560 MS/s is achieved by adjusting the sample clock provided by the clock generation PLL, whereas 2,048 MS/s requires a clock rate that is out of the acceptable range of the clock generation PLL. Therefore, a specific resampling module was designed by Peralex and implemented in the FPGA to provide 2,048 MS/s from a 2,560-MS/s rate. In addition to fast transients science, 2,048 MS/s is a standard for VLBI applications.

Inputs are sampled and digitized into 12-bit 2's-complement binary numbers in the range of −2048–2047. A 1-PPS (Pulse Per Second) signal is externally injected for synchronization purposes. The ADC yellow block outputs the 1-PPS signal for use in the FPGA logic as well, usually to synchronize all of the signal processing logics and to provide accurate timing.

To achieve good linearity for a noise-like signal, even in the presence of strong RFI, the input signal RMS (Root-Mean Square) amplitude should be set around 1/8 of the ADC highest coded value. Thus, logic was designed for calculating the signal RMS power for each input, integrated for 65,536 clock cycles (2^{20} samples). The sum is then read using a 32-bit-wide register. The value is then used to derive the RMS signal amplitude, and to adjust the input RF power level.

4.1.2. *PFB FIR + FFT engine*

In order to channelize the signals in the frequency domain, we use a polyphase filter followed by a Fast Fourier Transform. This is massively more efficient than implementing a set of pass-band filters placed adjacent to each other. The filter is a low-pass FIR (Finite Impulse Response) architecture and, according to the subsequent Fourier transform algorithm, the filter shape is replicated along all of the overall spectra. This mathematical approach basically allows the design of only one high-performing low-pass filter which is translated in frequency to the center of each of the FFT outputs. We chose a Hamming filter with 14 taps per spectral channel, giving a rejection of 60 dB in the adjacent channel, more than 120 dB at an offset of eight channels, and a flat band-pass over 80% of the channel width. The very high rejection is desirable for observing the weak astronomic signals in an RFI-contaminated environment.

We have used a green block available in the CASPER DSP library for both the polyphase filter and the FFT. We have chosen an FFT length of 4,096 in order to achieve 2,048 channels from the real-valued input signal.

4.1.3. *Stokes calculation*

The Stokes digital block implements logic for performing both auto- and cross-correlations, from now on marked as XX, YY, $\Re(XY^*)$, and $\Im(XY^*)$. Specifically, XX and YY represent the power spectra of the first and the second polarizations, respectively, whereas the other two elements provide the real and imaginary parts of the complex cross-polarization. These four values represent the base for calculating the four Stokes parameters.

4.1.4. *Integration block*

Accumulations are performed with single-vector accumulators available in the CASPER library. Since the polyphase block provides eight spectral channels at a time, we need a total of 32 accumulators with 256 (i.e. 2048/8) elements each. Accumulation is computed with full-precision 64-bit values. Accumulation duration is defined by the observer as a programmable number of FFT frames.

4.1.5. *Bit selection block and total power read*

The integration time may vary from tens of milliseconds to a few seconds, so the accumulated value may vary by orders of magnitude. The 64-bit values provided by the integration logic are subsequently rescaled by a programmable number of bits to fit in a 32-bit register. This is implemented using a barrel shift block (also available in the CASPER library).

Snapshots of the requantized spectra can be made available for direct readout. This is used to evaluate the broadband power in the signal, excising in software the channels affected by RFI. This

feature is used to measure the receiver system temperature before and during the actual observation. Although the broadband total power described above can be used for this purpose, this does not discriminate between any possible RFI contributions. RFIs are almost always variable in time, thus two measurements carried out in different moments would result in marked differences. The XX and YY spectra are captured via eight memories (one for each of the eight powers) which are fully written after each integration and read from the control software.

4.1.6. *Packet rate limiter module (Packet Trickler)*

Once all of the spectra are summed over the programmed integration time, the data has to be encapsulated into UDP packets and sent out via one (or more if needed) QSFP+ 40-GbE interface(s). Since the ADC bypass mode in the FPGA has a clock rate of 175 MHz and the QSFP+ mezzanine has a clock rate of 156.25 MHz, the data needs to be manipulated. Moreover, the 40-GbE yellow block manages digital streams as 256-bit wide only, while the integrator produces a total of 1,024 bits of parallel data, with eight parallel streams, four polarizations (XX, YY, and the two XY), and 32 bits per sample. In order to handle the mismatch in data width and clock frequency, we designed a Packet Rate Limiter module. The Packet Rate Limiter uses a Dual-Port Block RAM, around which logic has been added for writing the memory, reading the memory, and implementing an inter-packet delay to limit the packet data rate on the 40-GbE output. Write and read ports have different widths to accommodate the different bus sizes.

Write logic is implemented as a counter that generates the memory write address. When a whole integration has been stored, further writing is stopped and the read section is started.

The memory is read in blocks of 8,192 bytes (over 256 read cycles), to produce a single output packet. A packet contains all polarization values for 512 consecutive channels. The read is then inhibited for a predefined time, which allows the packet to be safely transmitted on the 40-GbE link. Further delay can be added depending on the capability of the receiving computer to handle the resulting data rate, but it must not be too large so as to avoid any data memory overflow. The process is repeated until all samples are sent.

4.1.7. *SPEAD packetizer*

SPEAD stands for *Streaming Protocol for Exchanging Astronomical Data*, a data stream format that became standard in radio astronomy applications. SPEAD uses the UDP protocol to transmit data packets from one host to another. Each packet is composed of a SPEAD header including spectral metadata and a data payload. Details can be found elsewhere.[1] We use a payload size of 8,192 bytes plus 96 bytes in the header, thus requiring the use of jumbo packets. A total of four UDP packets are needed to send out four products XX, YY, $\Re(XY^*)$, and $\Im(XY^*)$ for all of the 2,048 channels (each one represented with 4 bytes). In order for the packet capture program on the acquisition computer to reconstruct the proper sequence, SPEAD metadata contains a packet index.

4.1.8. *40-GbE output*

The last stage frames the data (header and payload) in UDP packets and then transmits these packets over one of the 40-GbE ports (port 0 in our case) of the QSFP+ mezzanine card. A 40-GbE CASPER yellow block is dedicated to this function. Data is encapsulated into UDP packets by adding a header containing the UDP, IPv4, and Ethernet protocols. The yellow block requires both the IP address and the port number of the destination host; both are provided via two dedicated registers. The block retrieves the destination MAC using a simple version of the ARP protocol.

4.2. *A tunable 65,536-channel spectrometer with 93.75/187.5-MHz bandwidth*

In this subsection, we describe a spectrometer (shown in Fig. 4) with 65,536 channels over a bandwidth of 93.75 MHz or 187.5 MHz, which provides frequency resolutions of 1.4 kHz and 2.8 kHz, respectively. This design is conceptually similar to the previous one, so we focus on the difference in implementation.

4.2.1. *ADC DDC yellow block*

The ADC DDC yellow block provides four complex (four in i and four in q) sample outputs for each of

[1] https://spead2.readthedocs.io/en/latest/_downloads/6160ba1748b1812337d9c7766bdf747a/SPEAD_Protocol_Rev1-_2012.pdf.

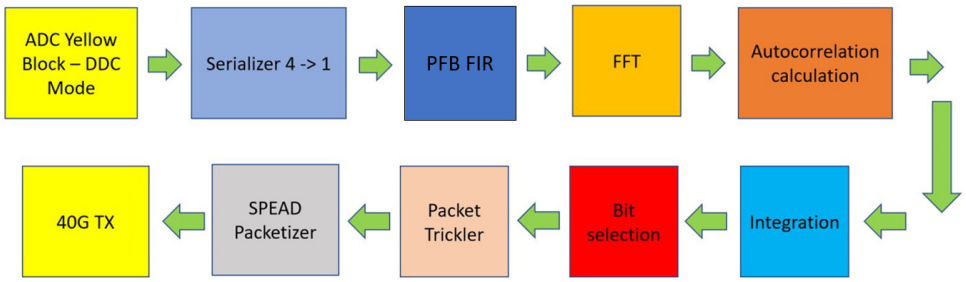

Fig. 4. (Color online) Block diagram of the narrowband (93.75/187.5 MHz) spectrometer. We draw a single green arrow that represents the data flow to simplify the scheme, actually streams from two polarizations are processed. The ADC DDC yellow block provides four parallel complex samples for the two signals of interest. Since a decimation 32 is used to narrow the bandwidth, the Serializer 4-to-1 block serializes the four parallel input samples into a single sample stream. A polyphase filter followed by an FFT engine provides the two signals in the frequency domain and the Auto-correlation calculation stage provides auto-correlations. Signals are then summed up channel-wise for a time set by the user in the Integration block, then a bit rescaling is done in the Bit Selection stage. Finally, data are bufferized (Packet Trickler), packetized (SPEAD Packetizer), and sent out (40G TX) toward a single 40G cage of the QSFP+ mezzanine card.

the four input signals. In this case, each sample is a 16-bit 2's-complement binary number in the range of −32,768–32,767. The ADC runs at 3 GS/s, with a decimated clock rate of 187.5 MHz.

The DDC operation consists of mixing the digitized signals with a complex continuous wave signal; after this mixing, the down-converted signals have a complex (real and imaginary) representation. The minimum decimation rate is four, corresponding to a decimated complex sample rate of 750 MS/s, which is reduced to 640 MS/s when the ADC sample rate is set to 2,560 MS/s. The resampling logic is also available in DDC mode to allow a sample rate of 512 MS/s. The same philosophy is applied with decimation by a factor eight, which provides sample rates of 375, 320, and 256 MS/s, respectively. The final decimation implemented on the ADC mezzanine board is 16. This forms the basis for all of the other sample rates shown in Fig. 2. To achieve smaller sample rates, further decimation is performed in the FPGA fabric. The ADC DDC yellow block was designed to provide four complex output samples, which is suitable in the case of decimation by four. For higher decimation values, the ADC generates blocks of four samples at a reduced rate, interleaved with empty samples. For efficient processing, the number of parallel samples is reduced from four to two for decimation by eight and from four to one for decimation by 16 and 32.

4.2.2. *Serializer four samples to one*

This spectrometer works at a bandwidth of 187.5 MHz or 93.75 MHz, respectively, for decimation by 16 and 32. This requires only a single complex stream, whose actual sample rate is determined by the decimation factor, set by the user via software. However, the ADC yellow block provides the data in bursts: 42 consecutive valid samples every 84 clock cycles in decimation-by-16 mode, and 21 consecutive valid samples every 84 clock cycles in decimation-by-32 mode. These data bursts are reordered as a single sequential data stream, using a FIFO buffer. Samples are present at every clock cycle in decimation by 16, while in decimation by 32 a data valid signal is used to mark valid samples. As a consequence, the signal processing chain has been modified to process only these valid samples.

4.2.3. *PFB FIR + FFT engine*

A narrow-bandwidth channelizer needs an asynchronous chain since signals are not always valid, thus we selected a PFB with an enable input signal, provided by the CASPER library. We aimed to maximize the number of spectral channels, which is limited by the amount of Block RAM available in the SKARAB FPGA. As a consequence, we selected a filter design with only four taps in the PFB block. This provides a wider transition band between channels, with the pass-band roll-off beginning in the outer half of each channel, and extending up to half of the adjacent channel.

We used the FFT version 9.1.2 IP core available in the Xilinx repository. This supports 8–65,536 channels. In order to save Block RAM, we omitted the option of reordering the channels in natural order in the FFT block. Reordering from bit reversal has been implemented in the *Packet Rate Limiter* block.

4.2.4. *Auto-correlation calculation*

To limit the amount of memory used in the accumulation block, cross-correlation could not be implemented with FPGA resources only. As a consequence, we calculate the auto-correlation XX and YY elements only. The feasibility of using the HMC external memory as an accumulator to provide cross-correlations is currently under investigation.

4.2.5. *Accumulation block*

The CASPER library does not provide any asynchronous accumulation block, thus we had to design an accumulation block that accepts a data valid input. This block uses a Dual-Port RAM with logic that only accumulates the input data when it is valid. This block was recently added in the CASPER library.

4.2.6. *Bit selection block and total power read*

This block is similar to the one outlined in Sec. 4.1.5. Here, only two (instead of 32) barrel shifters are instantiated. Two memories of 65,536 elements of 4 bytes each are used to retrieve the spectra needed to calculate the *Tsys*.

4.2.7. *Packet rate limiter module (Packet Trickler)*

This module is similar to the one described in Sec. 4.1.6. Major differences are due to the different input stream widths, which in this case is composed of two words of 32 bits each, for a total of 64 bits. As the input data width is smaller than the fixed output width (256 bits) to the 40-GbE yellow block, the memory block must reverse the ports used for read and write. The memory address for the write is modified in order to write the spectral channels in bit-reverse order, correcting for the FFT bit-reversal. The total block size is 512 kbytes, requiring a total of 64 UDP packets of 8,192 bytes each to be generated in the memory read part. The delay logic part did not change.

4.2.8. *SPEAD packetizer and 40-GbE output*

With respect to Sec. 4.1.7, the SPEAD packetizer change includes only the different metadata for the heap size, the frequency scale, and the larger number of packets in each heap. The same decoding routines can be used to assemble and tag packets from the two configurations. The 40-GbE UDP/IP logic part is identical to the one described in Sec. 4.1.8.

4.3. *Pulsar search full-Stokes spectrometer with 2,048 channels and a bandwidth of 1,280 MHz or 1,024 MHz*

A pulsar is a fast spinning, highly magnetized neutron star. Pulsars generate beamed radiation observed as very precise periodic pulses (of order of seconds down to milliseconds). Since the observation goal is to determine the rotation period as accurately as possible, digital spectrometers need to be designed with specific care to provide such precision. The standard bandwidth of 1,400 MHz presents the problem that when channelized into a number of channels which is a power of 2 larger than 2^9, the resulting channelized sample rate does not exactly divide 1 s. Most pulsar data reduction software assume that samples are aligned with the second, and thus are incompatible with this data rate. To avoid such drawbacks, the sample rate must be chosen appropriately. As described in Sec. 4.1.1, two further bandwidths were made available, 1,280 MHz and 1,024 MHz. Both these sample rates can support channelization of up to 2^{14} channels (2^{16} for the latter). Our application uses a channelizer with 2,048 channels, resulting in channelized sample rates of 625,000 spectra per second and 500,000 spectra per second, respectively. In the simplest application (coherent observations), a subset of channel samples, requantized to 8 bits, is sent as SPEAD packets over the 40-GbE links, for further processing. In incoherent mode, spectra rate can vary according to the object under investigation. In the case of pulsar, the worst case is represented by the millisecond pulsars, which require an integration time of a few tens of microseconds. The entire infrastructure (hardware, firmware, and software) is still under development.

5. SKARAB FPGA Resource Utilization

In this section, we show the FPGA resource utilization for the presented personalities; we have used the Vivado 2019.1.1 version to synthesize all the designs.

The three main resources of the device will be examined: slices, hardware multipliers (DSP48E1), and the BRAM. The Virtex-7 FPGA 7vx690tffg1927-2 has the following capacity: 108,300 logic slices, 3,600 DSP slices, and 53-Mb BRAM; percentages that we will mention refer to these values. Regarding the DSP slices, usage can be markedly different based on whether FPGA decimation/resampling (see third and

fourth columns in Fig. 2) is used, thus two different values are shown.

(1) **Wideband full-Stokes spectrometer with 2,048 channels.** The designs occupy approximately 56% of slices and 50% of the BRAM. DSP slices usage is 53.5% with the decimation/resampling logic and 32% without it.
(2) **Narrowband spectrometer with 65,536 channels.** The design occupies approximately 27% of slices and 90% of the BRAM. DSP slices usage is 20% with the decimation/resampling logic and 10% without it.

Displayed results show that, by implementing single spectrometers (only two of the four ADC inputs involved), the only critical resource usage appears to be the BRAM in 65k-channel narrowband spectrometer. Preliminary further tests show that two spectrometers (which would involve all of the four ADC input signals) can be simultaneously placed in the same design for both wide- and narrow-band described designs, as long as the FFT channels are halved in the narrowband spectrometers. In order to save BRAM, one can use the HMC memories to do vector accumulations. Each instantiated HMC requires both BRAM (roughly 8%) and slice (roughly 13%), thus a trade-off according to need can be done. In general, since part of the logic is common regardless of the number of spectrometers, enough logic remains to implement other possible algorithms like RFI mitigation techniques, total power engines, etc.

6. Hardware/Software Infrastructure Employed to Commission the SKARAB Spectrometers

Medicina radio telescope is a 32-m antenna located approximately 30 km from Bologna, in Italy. The telescope is equipped with different receivers, and the frequency agility is available so as to change the observing frequency very fast. The list of available receivers[(m)] is as follows: *L*-band, *S*-band, *C*-band, *M*-band, *X*-band, and *K*-band. Both *M*-band and *X*-band were used to do observations outlined in this paper.

In this section, we describe the commissioning effort to couple the SKARAB board and the outlined spectrometers with the telescope's hardware/software environment. Specifically, an RF signal conditioning module had to be designed and tested to avoid any aliasing phenomena and provide the proper signal level to the spectrometers, along with the time and frequency needed for reference signals. With regard to the firmware, we have done a few tests to set up the relevant parameters of the spectrometers properly, as well as to deal with ADC DDC local oscillator improper rounding. Finally, a data acquisition framework was designed to manage data produced by the SKARAB spectrometers, as well as the needed software to integrate the new hardware in the software controlling the telescope.

6.1. *RF signal conditioning and time and frequency reference*

Once RF signals for each receiver are properly conditioned and down-converted into the frequency interval of 0–2 GHz, a set of anti-aliasing filters is used to feed signals to the various backends; available frequency ranges are 100–300, 100–730, 100–1,250, and 100–2,000 MHz. Since we are dealing with a spectrometer whose maximum bandwidth is 1.4 GHz, we had to design and build a signal conditioning board suitable to be used with this additional bandwidth; the board is shown in Fig. 5. The board accepts four analog signals in input and provides two different outputs, one for the SKARAB (band limited to 1.4 GHz) and one for the other equipment (unfiltered). The board also provides signal amplification to the appropriate SKARAB RF level. The filtering is performed by a Reactel low-pass filter model 7LMX-X1350S11 whose cut-off is 1,350 MHz and whose featuring is shown in Fig. 5. For our tests, we used only two of the four signal chains. The Medicina's signal conditioning hardware was set to provide two signals for the two received polarizations, at full bandwidth (2 GHz).

As indicated in the literature, input analog RMS level ought to be around 1/8 of the maximum representable number. Thus, we adjusted the gain in the telescope receiver chain to obtain an RMS level around 256 for the wideband spectrometer and around 4,096 for the narrowband spectrometer. The SKARAB board also needs the 1-PPS and the 10-MHz reference signals in input, they were provided by a MASER available at the observing station.

6.2. *Setting of the FPGA DSP chain*

Regarding the FPGA DSP chain, it is important to keep the signal level in the appropriate range to

[m] https://www.radiotelescopes.inaf.it/summary.html.

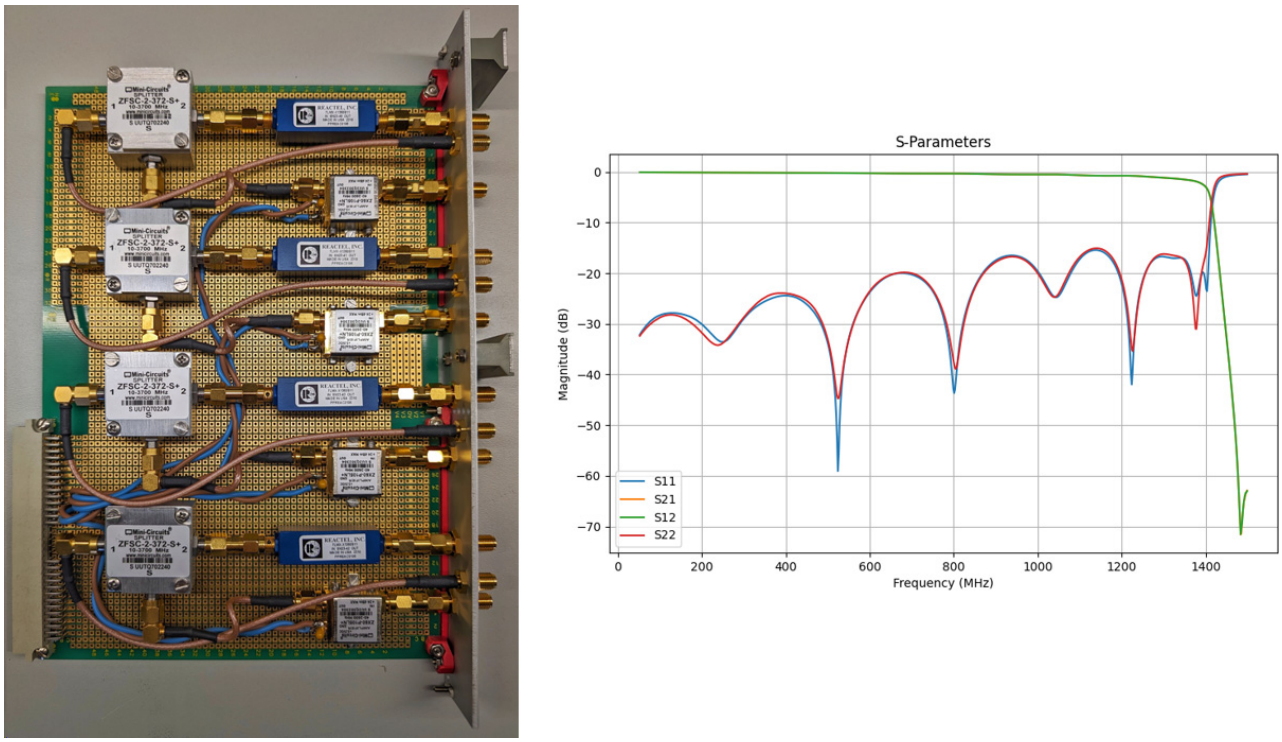

Fig. 5. On the left, we show a picture of the signal-conditioning board that we coupled with the SKARAB. Each analog input signal is amplified by 16.8 dB by the RF amplifier ZX60-P105LN+, and split into two signals by a Mini Circuits splitter ZFSC-2-372-S+. The first unfiltered copy is provided at the output, the second copy goes through a Reactel, Inc. band-pass filter (BPF) model 7LMX-X1350S11, whose *S*-parameters that we have measured are shown in the right panel.

avoid both clipping noise and excessive quantization noise at all processing stages. This depends on several factors, both predictable (as the variable integration time) and to be measured experimentally (as the received signal spectral distribution). Our designs allow one to control the signal level by selecting the rescaling along the FFT module, and by controlling the barrel shifter after the integrator. The FFT rescaling has been determined empirically for each design and receiver. The shift parameter determines the suitable bits range to be set according to the chosen integration time. As a standard value, we used shift $= 29 - \lg2(\text{acc\_len})$ for both auto- and cross-correlations.

We verified that the spectra for both wide- and narrow-bandwidth spectrometers did not show any artifact; specifically, no birdies were present at the center of the bandwidth as well as at multiples of the clock frequency.

The local oscillator for the DDC engine implemented in the ADC mezzanine board, which is used in the narrowband spectrometers, has a finite resolution. As a consequence, the actual LO frequency may differ from the desired one. As we recorded the latter in the observation files, a small frequency discrepancy was observed in the plotted spectra. This was solved by logging the actual programmed value for the LO frequency.

6.3. *Data acquisition software*

The data acquisition software (DAQ) runs on the server controlling the SKARAB. A 40-Gbit/s NIC (Network Interface Card) provides a point-to-point connection between the SKARAB and the server itself. The server is also equipped with enough RAM memory to manage all of the incoming data safely, i.e. to guarantee that no packet loss occurs. The DAQ is responsible for various tasks, including receiving packets from the NIC, retrieving ancillary data from the antenna control software, known as DISCOS (Development of the Italian Single-dish Control System) Orlati *et al.* (2016), and merging these two sets of information to create the final files in FITS (Flexible Image Transport System) format, as illustrated in Fig. 6.

For enhanced control and customization, the software was internally developed by drawing inspiration from the one designed for the SARDARA

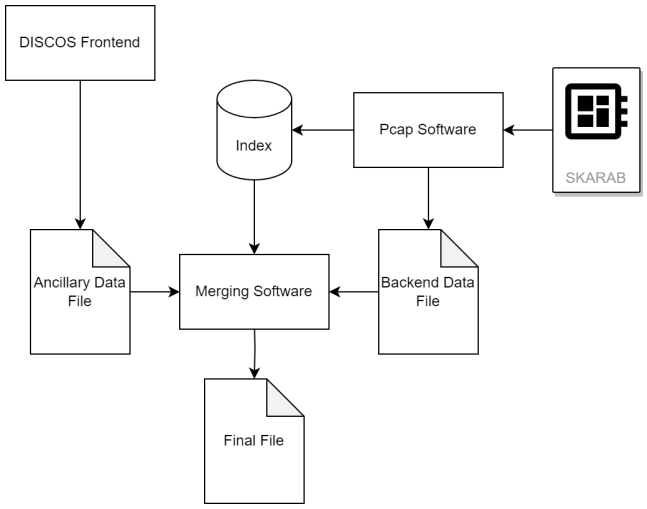

Fig. 6. Schematic representation of the data acquisition process. The DAQ system receives packets from the NIC and retrieves ancillary data from the DISCOS antenna control software. These two sets of information are merged to generate the final files in FITS format.

backend. The main difference is that with SARDARA the integration was done partially in the FPGA and completed in the server, whilst the SKARAB system does a complete integration in the FPGA. Following subsections provide a more detailed overview of these three modules.

6.3.1. *Packet capture*

All of the designed FPGA firmware output the data in UDP packet streams, thus a UDP packet capture software has been written in C language. The program defines a callback function that is invoked every time a UDP packet is received. As described in Secs. 4.1.7 and 4.2.8, each UDP packet has a header 96 bytes long and a payload with a size of 8,192 bytes. The header also contains a packet counter to ensure that data is properly reassembled. Specifically, the spectra captured from the incoming UDP packets are written into a FITS file containing spectra and a corresponding timestamp. Each spectrum has the four elements XX, YY, $\Re(XY^*)$, and $\Im(XY^*)$ repeatedly mentioned; the first two are saved as unsigned values whereas the next two are saved as long-signed values; the number of spectra to be saved into a given FITS file is programmable. Once the chosen number of spectra has been recorded and the FITS file is saved in a specific folder, an index file located in the same folder is also updated. This index file contains a line for each new FITS file that is written: each line contains the complete directory path, the timestamp of the first recorded spectrum, and the timestamp of the last recorded spectrum. An index file is properly read by the merging program described in the next subsection, which also opens a listening socket to receive *start* and *stop* acquisition commands.

6.3.2. *Merging algorithm*

The "only-data" FITS files lack antenna information, which is, in fact, available in the ancillary FITS files generated periodically by DISCOS at a specific rate. For each ancillary FITS file provided by DISCOS, the merging program examines the timestamps of the first and last records. These values define the time interval for searching the files that need to be paired with the "only-data" FITS files. The relevant files are identified using the previously mentioned index file, and a linear interpolation of timestamps is applied accordingly.

6.3.3. *DISCOS frontend*

This last module handles interactions with the DISCOS software component using the communication protocols that can be found in the *discos-backend*[n] Python library. The aim of the library is to map the high-level commands typed by the user into low-level commands to configure the SKARAB appropriately. According to the chosen observation mode, the correct bit file is uploaded into the FPGA, and all of the registers are properly initialized. Additionally, comprehensive monitoring of all involved actions, including the initiation of data acquisition and the merging of FITS files, is ensured. Moreover, the capability for both reading and writing registers from the console during data acquisition is also available.

7. Scientific Commissioning Carried Out at Medicina Radio Telescope

In this section, we outline the results that we have achieved carrying out the radio astronomical observations at the Medicina radio telescope. Two subsections describe the two kinds of observations performed: wideband spectro-polarimetry and narrowband spectroscopy.

The targets used for the commissioning tests are the two very bright supernova remnants (Crab Nebula and 3C58) and the interstellar MASER source W3 (OH). We selected these sources because they have

[n] https://github.com/discos/discos-backend.

been extensively studied in the radio band with many radio telescopes and there are observations in the literature that can be used for comparison.

7.1. *Wideband spectral-polarimetry X-band observations of the 3C58 and of the Crab*

We tested the full-Stokes spectrometer described in Sec. 4.1: bandwidth of 1.4 GHz, 2,048 channels. We filtered a frequency bandwidth of 680 MHz, centered at 8.52 GHz, and sampled with 996 channels of 0.7 MHz in width. We observed the bright supernova remnants 3C58 and the Crab (Tau A). We used the On-The-Fly (OTF) technique to obtain two sets of orthogonal scans, along RA and DEC directions, in the equatorial frame for each object. We observed the sources 3C147, 3C84, and 3C138, respectively, as flux density, polarization leakage, and polarization angle calibrators. We also performed a *sky dip* (i.e. a technique consisting in measurements of the sky brightness at several zenith angles) to model the variation of atmospheric opacity with elevation. The data reduction and imaging were done with the Single-dish Spectral-polarimetry Software (SCUBE) Murgia *et al.* (2016). The main steps of the data reduction pipeline included: RFI flagging, total intensity and polarization calibration, baseline subtraction, and imaging. The final products of the data reduction pipeline are the spectral cubes of the L and R circular polarizations and of the Stokes parameters U and Q. To improve the signal-to-noise ratio, we combined the orthogonal RA and DEC scans. Finally, from the L and R circular polarizations, we obtained the total intensity $I = L + R$. From the Stokes parameters U and Q, we obtained the linear polarization intensity, $P = \sqrt{U^2 + Q^2}$, and angle, $\phi = 0.5 \arctan(U/Q)$.

7.1.1. *Observation of 3C58*

We acquired three RA scans and two DEC scans of a field of view of $1^\circ \times 1^\circ$ centered on 3C58. In the left panel of Fig. 7, we show the total intensity image of 3C58 at 8.52 GHz obtained from the spectral average of all channels in the 680-MHz bandwidth. In the right panel of Fig. 7, we show the polarized intensity image with the total intensity contours overlaid. The length of the polarization vector is proportional to the fractional polarization while their orientation indicates the $\vec{B}$-field polarization angle.

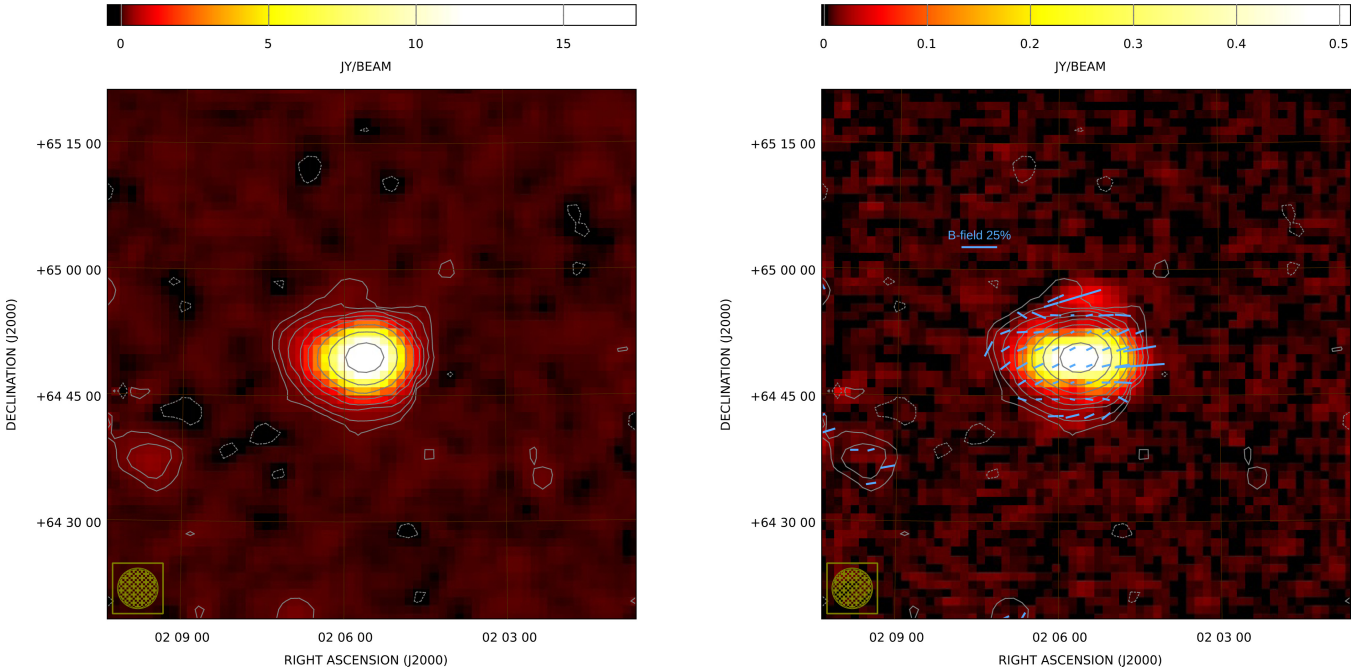

Fig. 7. Supernova remnant 3C58: Left: Total intensity image at 8.52 GHz obtained from the spectral average of all channels at the 680-MHz bandwidth. The noise RMS is 33 mJy/beam (4.75-arcmin FWHM beam). Contour levels start from 3σ and increase by a factor of 2. One dotted negative contour is traced at -3σ. The unresolved source in the left is LQAC 032 + 064 001. Right: Linear polarized intensity image of 3C58 with the total intensity contours and the $\vec{B}$-field polarization vectors overlaid (not corrected for Galactic RM).

For 3C58, at 8.52 GHz, we found a flux density of $S_\nu = 27.2 \pm 0.1$ Jy, consistent with the measurements at nearby frequencies available in the literature. In particular, we compared our data with the same value of flux density of 27.2 ± 1.4 Jy at 5 GHz reported by the 3CR catalog (Kellermann *et al.*, 1969) and with the value of 32.9 ± 5 Jy at 4.85 GHz reported by the GB6 catalog (Becker *et al.*, 1991). The consistency of these values is in agreement with the relatively flat spectral index $\alpha \simeq 0.1 \pm 0.02$ of 3C58 (Green, 1986), where α is defined according to $S_\nu \propto \nu^{-\alpha}$.

The right panel of Fig. 7 shows the image of the linearly polarized intensity with the $\vec{B}$-field polarization angle vectors superimposed, for direct comparison with a similar image obtained with the Effelsberg 100-m radio telescope (Reich *et al.*, 1998). The polarization angle is not corrected for the Galactic Faraday rotation measure (RM), see e.g. Oppermann *et al.* (2012). The point-to-point distribution of the $\vec{B}$-field polarization angle across the source is qualitatively comparable between the two images, despite the coarser resolution of our observation at 8.52 GHz. We also calculated an average value for the polarization angle of 3C58 by integrating the intensities of Stokes parameters U and Q shown in Fig. 8. For Stokes Q, we measure a total flux density of 0.75 ± 0.02 Jy, while for Stokes U, we measure 0.62 ± 0.02 Jy. The linearly polarized flux is of 0.97 Jy with an $\vec{E}$-field polarization angle, in the equatorial frame, of approximately $\phi \simeq (19.8 \pm 0.8)^\circ$ at 8.52 GHz. The value can be compared with the WMAP results of Weiland *et al.* (2011) who reported an angle of 5.4° at a frequency of 22.7 GHz. The two measurements differ by approximately $\Delta\phi \simeq 14^\circ$. This could be an instrumental effect, due to the different frequencies and resolutions of the two observations. It is also possible that the Faraday rotation effect occurring in the intervening interstellar medium (or in 3C58 itself) could play a role in explaining the offset of the polarization angle at the two frequencies.

Therefore, the image of the point-to-point distribution of the polarization angle corresponds to that obtained with the Effelsberg telescope. However, the integrated value of the polarization angle across the entire source differs from the WMAP result by approximately 14°.

7.1.2. *Observation of the Crab Nebula*

We acquired three RA scans and two DEC scans of a field of view of $1^\circ \times 1^\circ$ centered on the Crab Nebula. In the left panel of Fig. 9, we show the total intensity image of the Crab Nebula at 8.52 GHz obtained from the spectral average of all channels in

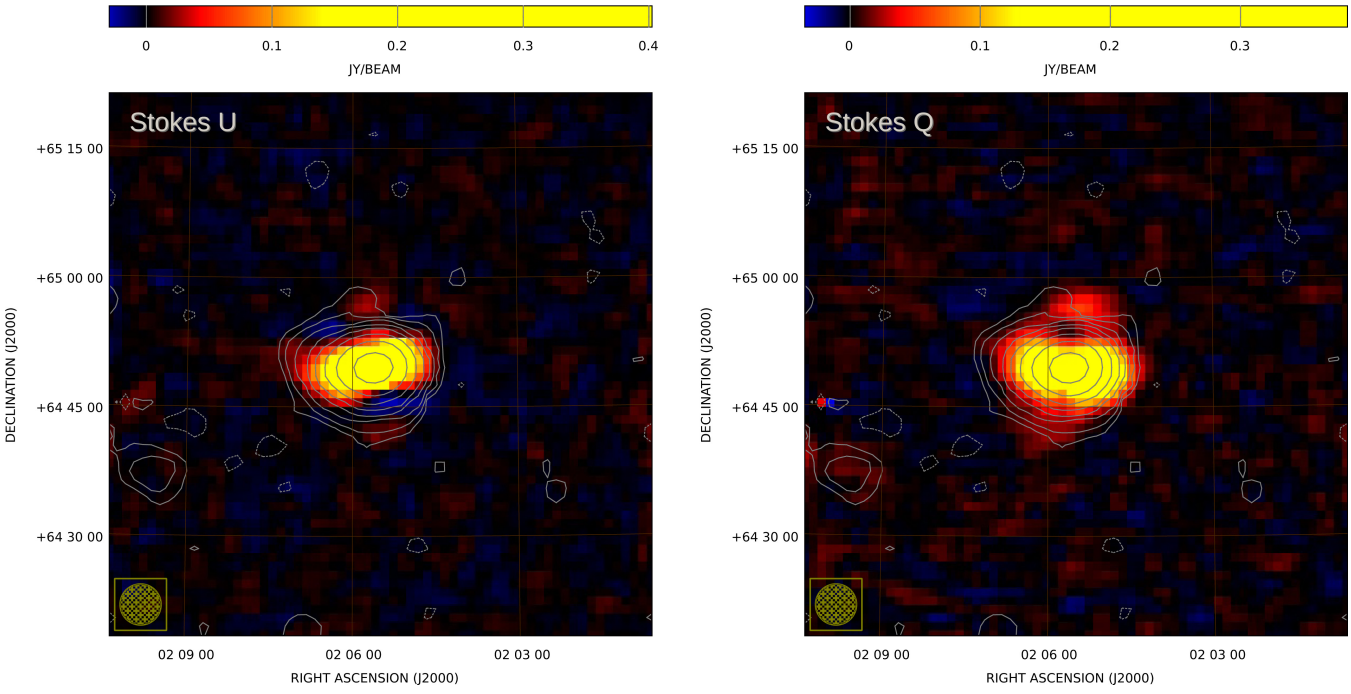

Fig. 8. Supernova remnant 3C58: Stokes parameters U (left) and Q (right) at 8.52 GHz with the total intensity contours overlaid.

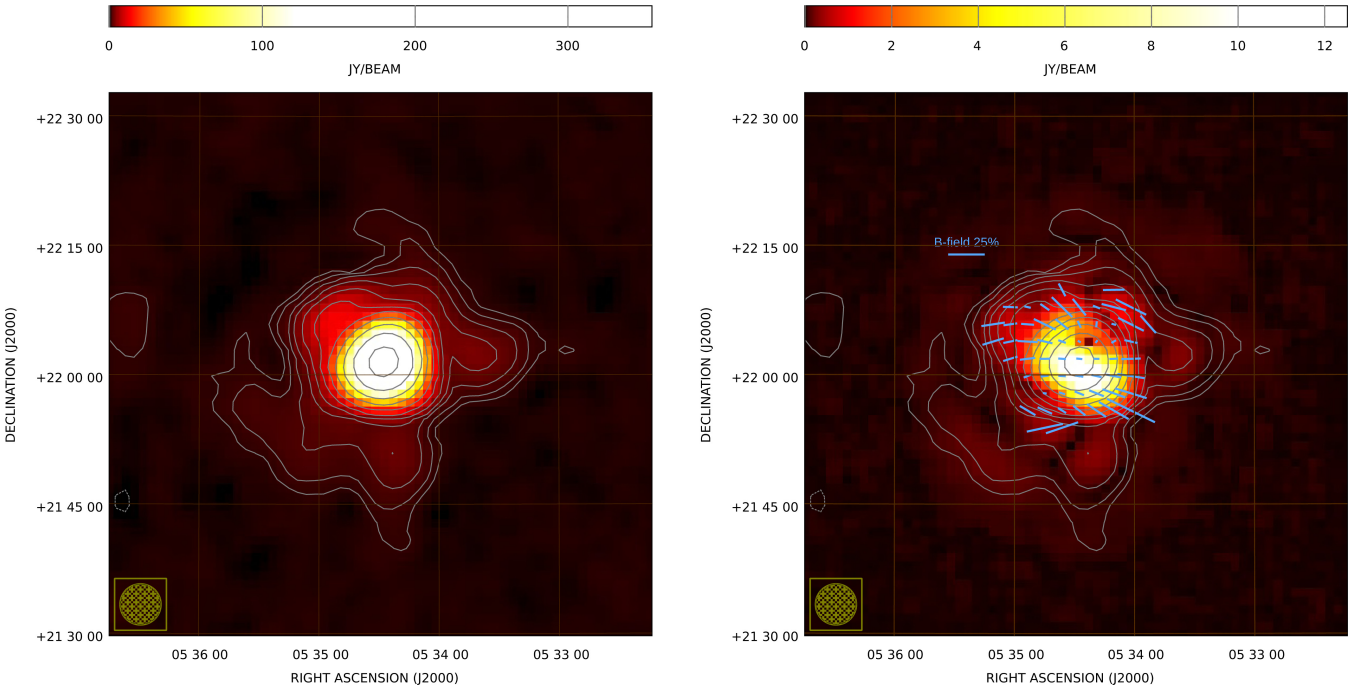

Fig. 9. Supernova remnant Crab Nebula. Left: Total intensity image at 8.52 GHz obtained from the spectral average of all channels at the 680-MHz bandwidth. The noise RMS is 90 mJy/beam (4.75-arcmin FWHM beam). Contour levels start from 3σ and increase by a factor of 2. One dotted negative contour is traced at -3σ. The Crab Nebula is so bright that a "halo," an instrumental emission originated by the side lobes of the telescope beam, is visible around the source. Right: Linear polarized intensity image of the Crab Nebula with the total intensity contours and the $\vec{B}$-field polarization vectors overlaid.

the 680-MHz bandwidth. The "halo" surrounding the source is instrumental emission originated by the side lobes of the telescope beam. In the right panel of Fig. 9, we show the polarized intensity image with the total intensity contours overlaid. The length of the polarization vector is proportional to the fractional polarization while their orientation indicates the $\vec{B}$-field polarization angle. The level of Galactic RM toward the Crab Nebula is negligible at 8.52 GHz.

For the Crab Nebula at 8.52 GHz, we found a flux density of $S_\nu = 504.1 \pm 0.2$ Jy, consistent with the measurements at nearby frequencies available in the literature. According to the spectral fit presented in Ritacco *et al.* (2018), $S_\nu = 1010.2 \pm 3.8(\nu/\mathrm{G}Hz)^{-0.32}$ Jy, and the expected flux density at 8.52 GHz is 509 Jy. The $\vec{B}$-field polarization angle in the central part of the source is shown in the right panel of Fig. 9. The polarization vectors are not corrected for the significant amount of off-axis instrumental polarization visible in Fig. 9. The Crab Nebula is significantly brighter than 3C58 and consequently, the off-axis beam polarization makes it very difficult to measure the true intensity and polarization angle in these observations. The fractional polarization at 8.52 GHz and 4.75-arcmin resolution is of about 5%. The images of the Stokes parameters U and Q are shown in Fig. 10.

7.2. *Observation of W3(OH)*

W3(OH) is one of the most intensively studied star-forming regions. We performed one RA scan of a field of view of $1^\circ \times 1^\circ$ centered on W3(OH) to obtain a high-frequency-resolution spectroscopy of the 6.7-GHz MASER methanol line. We observed a bandwidth of 93.75 MHz sampled with 65,536 spectral channels. In Fig. 11, we show a zoomed view of the spectral cube close to the methanol MASER emission and a plot of the line profile at a spectral resolution of 1.43 kHz.

The profile of the MASER methanol line obtained with SKARAB can be compared to a similar observation performed with the XARCOS backend during the Astronomical Validation of the SRT (Prandoni *et al.*, 2017, Fig. 10). The XARCOS spectro-polarimeter provided four bands with increasing spectral resolutions of 30.5, 3.8, 1, and 0.2 kHz. The spectral resolution of the last two bands approximately corresponds to that of SKARAB and the profile of the observed line in Fig. 11 matches the published results.

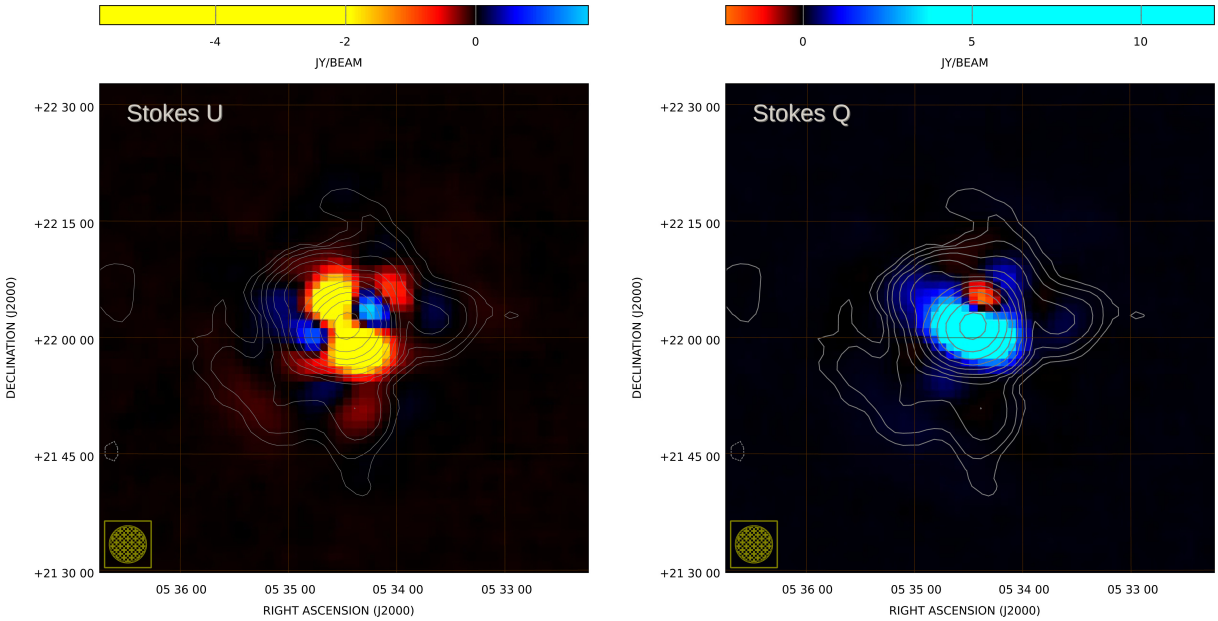

Fig. 10. Supernova Crab Nebula. Stokes parameters U (left) and Q (right) at 8.52 GHz with the total intensity contours overlaid.

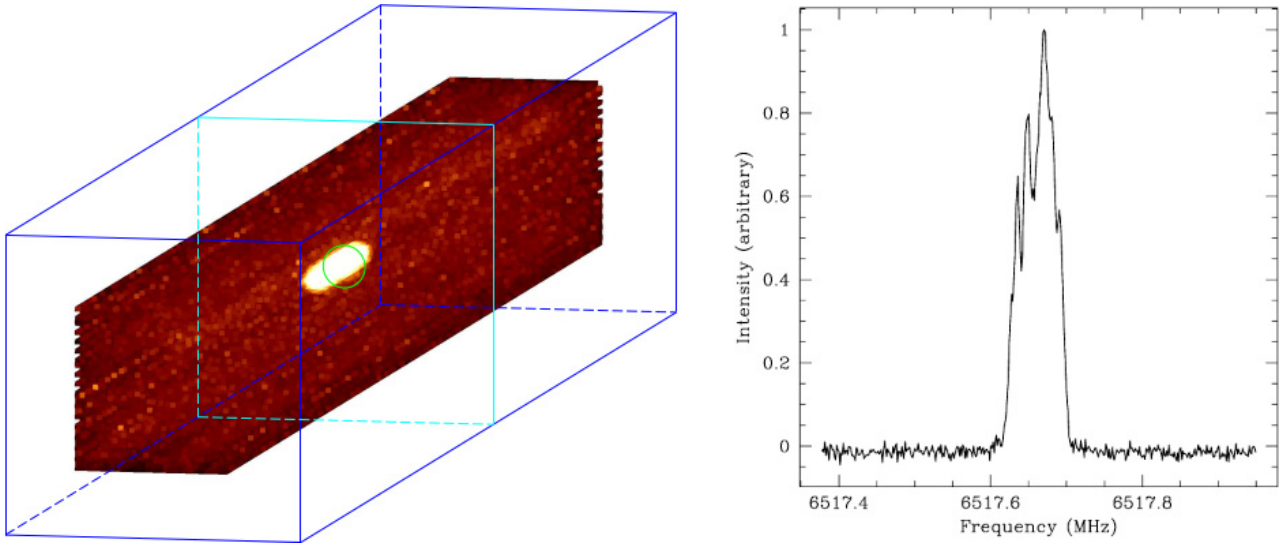

Fig. 11. Star-forming region W3(OH): Left: The 3D rendering of the spectral cube. Right: Profile of the spectral line average in the circular region shown in the left panel.

8. Conclusion and Future Works

In this paper, we have exhibited the potential of the SKARAB platform in single-dish radio astronomical applications. Specifically, we have shown how the platform has been successfully employed for different scientific purposes that a single-dish radio telescope might provide: full-Stokes wideband imaging and high-frequency-resolution spectroscopy to study narrowband emissions like those from astronomical MASER. Tests for high-resolution timing to study fast transients like pulsar and Fast Radio Bursts will be shown in a specific paper. SKARAB displayed promising performance in all of the aforementioned observation modes, also due to the high-performance ADC mezzanine board that provides a very high dynamic range for both wide- and narrow-bandwidth applications.

As all of the outlined SKARAB spectrometers are solely FPGA implementations, future work will focus on improving FPGA resource usage to

enable additional data outputs and resolution. The current planned development includes implementing vector accumulations on HMC in order to save Virtex-7 Block RAM and implementing a corner turner stage in the two HMC memories as described in Sec. 3.2.

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