Publication Year	2021
Acceptance in OA	2025-02-11T14:17:27Z
Title	The electronics of the High-Energy Particle Detector on board the CSES-01 satellite
Authors	Ambrosi, G., Bartocci, S., Basara, L., Battiston, R., Burger, W. J., Campana, D., Caprai, M., Carfora, L., Castellini, G., Cipollone, P., Conti, L., Contin, A., De Donato, C., De Persio, F., De Santis, C., Follega, F. M., Guandalini, C., Gebbia, G., Ionica, M., Iuppa, R., Laurenti, G., Lazzizzera, I, Lolli, M, Manea, C., Martucci, M., Masciantonio, G., Merge, M., Mese, M., Osteria, G., Pacini, L., Palma, F., Palmonari, F., Panico, B., PARMENTIER, Alexandra, Patrizii, L., Perfetto, F., Picozza, P., Pozzato, M., Puel, M., Rashevskaya, I, Ricci, E., Ricci, M., Ricciarini, S., Sahnoun, Z., Scotti, V, Sotgiu, A., Sparvoli, R., Vitale, V., Zoffoli, S., Zuccon, P.
Publisher's version (DOI)	10.1016/J.NIMA.2021.165639
Handle	http://hdl.handle.net/20.500.12386/35891
Journal	NUCLEAR INSTRUMENTS & METHODS IN PHYSICS RESEARCH. SECTION A, ACCELERATORS, SPECTROMETERS, DETECTORS AND ASSOCIATED EQUIPMENT

The electronics of the High-Energy Particle Detector on board the CSES satellite

G. Ambrosi[a], S. Bartocci[b], L. Basara[c], R. Battiston[c,d], W.J. Burger[c], D. Campana[e], M. Caprai[a], L. Carfora[f,b], G. Castellini[g], P. Cipollone[b], L. Conti[h,b], A. Contin[i,j], C. De Donato[b], F. De Persio[b], C. De Santis[b], F.M. Follega[c,d], C. Guandalini[j], M. Ionica[a], R. Iuppa[c,d], G. Laurenti[j], I. Lazzizzera[c,d], M. Lolli[j], C. Manea[c], M. Martucci[f,b], G. Masciantonio[b], M. Mergé[b], M.Mese[e,k], G. Osteria[e,*], L. Pacini[g], F. Palma[b], F. Palmonari[i,j], B. Panico[e], A. Parmentier[b], L. Patrizii[j], F. Perfetto[e], P. Picozza[f,b], M. Pozzato[j], M. Puel[c], I. Rashevskaya[d], E. Ricci[c,d], M. Ricci[l], S. Ricciarini[g], V. Scotti[e,k], A. Sotgiu[b], R. Sparvoli[f,b], V. Vitale[b], S. Zoffoli[m], P. Zuccon[c,d]

[a] *INFN Sezione di Perugia, V. A. Pascoli, 06123, Perugia, Italy*
[b] *INFN, Sezione di Rome "Tor Vergata", I-00133 Rome, Italy*
[c] *INFN - TIFPA, V. Sommarive 14, 38123 Povo (Trento), Italy*
[d] *University of Trento, V. Sommarive 14, 38123 Povo (Trento), Italy*
[e] *INFN - Sezione di Napoli, V. Cintia, 80126, Naples, Italy*
[f] *University of Rome "Tor Vergata", Department of Physics, I-00133 Rome, Italy*
[g] *IFAC-CNR, V. Madonna del Piano, 10, 50019 Sesto Fiorentino (Florence), Italy*
[h] *Uninettuno University, C.so V. Emanuele II, 39, 00186, Rome, Italy*
[i] *University of Bologna, V.le Berti Pichat 6/2, Bologna, Italy*
[j] *INFN - Sezione di Bologna, V.le Berti Pichat 6/2, Bologna, Italy*
[k] *University of Naples "Federico II ", Department of Physics, I-80126 Naples, Italy*
[l] *INFN - LNF, V. E. Fermi, 40, 00044 Frascati (Rome), Italy*
[m] *Italian Space Agency, V. del Politecnico, 00133 Rome, Italy*

Abstract

CSES (China Seismo-Electromagnetic Satellite) is a Chinese-Italian scientific space mission dedicated to monitor the variations of the main parameters of the topside ionosphere (electric and magnetic fields, plasma parameters, charge particles fluxes) caused by either natural emitters - especially earthquakes - or artificial ones.

The CSES satellite was successfully launched from the Jiuquan Satellite Launch Center located in the west of Inner Mongolia on February 2^{nd}, 2018, and it is now orbiting under nominal conditions. The expected mission lifetime amounts to 5 years. CSES is the first element of a multi-satellite monitoring system; several satellites are scheduled for the next few years.

The High Energy Particle Detector (HEPD) is the main contribution of the Italian collaboration to the mission. It was designed and built in order to detect electrons in the energy range between 3 and 100 MeV, protons between 30 and 200 MeV, and light nuclei in the MeV energy window.

The electronics of the detector was designed following stringent requirements on mechanical and thermal stability, power consumption, radiation hardness and double redundancy. The system successfully went through the space qualification tests. In this paper, we describe the HEPD electronics, the space qualification tests performed before launch, and the in-flight performance of the detector.

Keywords: Detector techniques for Cosmology and Astroparticle Physics, Satellite experiment, electronics
PACS: 29.40.Cs, 29.40.Gx

1. Introduction

CSES (China Seismo-Electromagnetic Satellite) [1] is a Chinese-Italian scientific space mission devoted to the monitoring of electromagnetic fields and waves, plasma and particles perturbations of the atmosphere, ionosphere and magnetosphere induced by natural sources and anthropogenic emitters, and to investigate their correlations with the occurrence of seismic events. In general, CSES is intended to study the structure and dynamics of the topside ionosphere, the coupling mechanisms with the lower and higher plasma layers, and the temporal variations of the geomagnetic field, under quiet and disturbed conditions. Solar-terrestrial interactions and solar physics phenomena, namely Coronal Mass Ejections (CMEs), solar flares and cosmic ray solar modulation, will also be studied.

Eight payloads are installed on board the CSES satellite for the measurement of electromagnetic field components, plasma parameters and energetic particles, as well the as the X-ray flux, namely: a High-Precision Magnetometer (HPM), a Search-Coil Magnetometer (SCM), an Electric Field Detector (EFD), a Plasma Analyzer Package (PAP),

*Corresponding author. E-mail: giuseppe.osteria@na.infn.it

a Langmuir Probe (LP), a Global Navigation Satellite System (GNSS) Occultation Receiver, and a set of particle detectors, the High-Energy Particle Package (HEPP) and the High-Energy Particle Detector (HEPD). The Italian contribution to the mission includes the design and construction of HEPD, which is devised to detect electrons in the energy range between 3 and 100 MeV, protons between 30 and 200 MeV, and light nuclei.

The article is organized as follows: after an overview of the CSES satellite (section 2) and HEPD instrument (Section 3), Section 4 describes the general architecture of HEPD electronics and each of its sub-systems in detail. Section 5 summarizes the tests and qualification campaigns carried out on the four models of HEPD before launch. Section 6 is devoted to the presentation of the in-orbit performance of HEPD electronics after two years of flight. Finally, Section 7 presents a summary and conclusions.

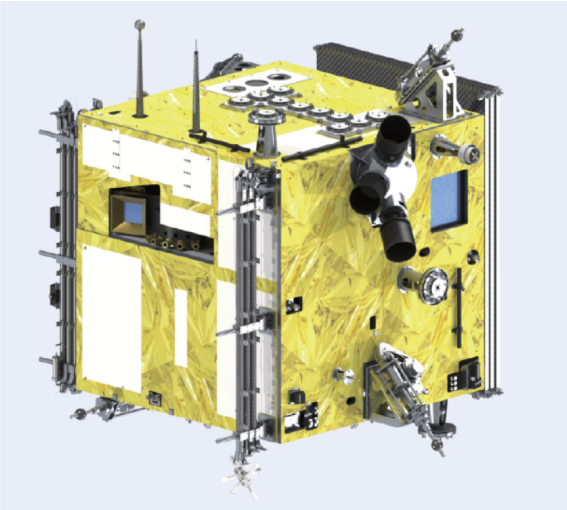


Figure 1: *Layout of the CSES satellite with stowed solar panel.*

2. CSES satellite

The CSES program plans to put multiple satellites into orbit to allow concurrent observations of the physical phenomena of interest. Zhangheng-1, the first CSES satellite (aka CSES-01), has been in orbit since February 2^{nd}, 2018. The second satellite (Zhangheng-2 or CSES-02) is under development, and its launch is currently foreseen for early 2022.

CSES-01 is a 3-axis stabilized satellite based on the CAST2000 platform with a mass of 730 kg and a size of 145 cm (Y) $\times$ 144 cm (Z) $\times$ 143 cm (X) (see figure 1). It mounts a single deployable solar array and has a peak of power consumption of about 900 W. Scientific data are downloaded 6 to 8 times a day for about 500 seconds. The maximum transmission speed is 120 Mbit/s. CSES-01 is maintained in a Sun-synchronous orbit at an average altitude of 500 km, an inclination of 97.32°, a period of 94.6 minutes, a revisit time of 5 days, and the LTDN (Local Time of Descending Node) is at 14:00 PM. The planned life of the mission is 5 years.

CSES-01 comprises the following platform subsystems: Attitude and Orbit Control (AOC), On-Board Data Handling (OBDH), Tracking, Telemetry and Command (TTC), Power Supply (composed of an 80-Ah Li-ion battery and solar panels), and Thermal Control.

The AOC makes use of Earth-oriented 3-axis stabilization; attitude sensors (three star trackers, two groups of gyros, and one digital sun sensor) are used to measure the attitude, reaction wheel and magnetic torque in order to maintain the zero-momentum control.

To reduce any interference over the scientific payloads from solar panel rotation or AOC adjustments, two operating regions are selected:

- the payload working zone at latitudes between $-65°$ and $+65°$,
- the platform adjustment zone at latitudes $> +65°$ or $< -65°$, where the payloads stop working.

When in working zone, each instrument collects data in two operating modes: "burst mode" and "survey mode". The burst mode is usually activated when the satellite passes over China and regions of the world marked by the strongest seismic activity. The survey mode is thought for the remaining areas of the Earth. When in orbit, the X axis of the satellite is oriented along the velocity vector, while the Z axis points to nadir. The solar panel located on one side of the satellite can be rotated around the Y axis at latitudes $> +65°$ and $< -65°$ in order to optimize power consumption.

3. The High Energy Particle Detector

The High Energy Particle Detector aims to investigate the precipitation of trapped particles induced by atmospheric electromagnetic (EM) emissions and seismo-EM disturbances [2, 3, 4]. HEPD provides good energy and angular resolution for electrons (3-100 MeV), protons (30-200 MeV), and light nuclei.

The instrument consists of two main active sensors, a silicon tracker to measure the impact point and arrival direction of any impinging particle, and a range calorimeter to measure particle energy. In more detail, as shown in Figure 2, the instrument consists of:

- two planes of double-side silicon microstrip sensors placed on top of the instrument (silicon tracker);
- one layer of segmented plastic scintillator (trigger plane);
- 16 plastic scintillator layers, plus a layer of LYSO (Lutetium-Yttrium Oxyorthosilicate) inorganic scintillator crystals (range calorimeter);

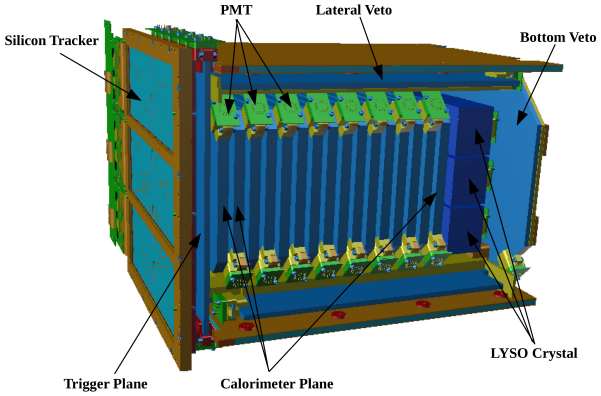


Figure 2: View of the HEPD apparatus: lateral and top panels have been removed for visualization purposes.

- one layer of plastic scintillator (veto bottom).

Additional plastic scintillators cover the four sides of the apparatus, completing the veto system.

Every plastic scintillator is read out by two photomultipliers (PMTs), while the LYSO crystals are read out by one single PMT located to its bottom side. In all cases, the readout is performed by R9880U-210 Hamamatsu PMTs. The HEPD detector is contained within an aluminum box with dimensions $40.36 \times 53.00 \times 38.15$ cm^3. The box is housed in the satellite cabin space, which provides the contact surface for heat dissipation The total instrument mass is about 45 kg, the power budget is 43 W. A detailed description of the HEPD sub-detectors can be found in [5, 6].

4. The electronics of HEPD

4.1. General architecture

HEPD electronics has been designed according to the general requirements imposed on the payload by satellite operations: in this specific case, a power budget of 43 W, a temperature operating range between -10 °C and +35 °C, a limit on the maximum amount of data transferable to the ground per day (data budget: 50 Gb/day) and a lifetime longer than 5 years.

The HEPD electronic system is composed of seven subsystems:

- Main Control System;
- Front-end electronics and Analog-to-Digital conversion (ADC) electronics of the Silicon tracker;
- Front-end electronics and Analog-to-Digital conversion electronics of the PMTs (Trigger, Calo and Veto systems);
- Trigger system;
- Data acquisition (DAQ) system;
- Housekeeping system;
- Power system.

The **Main Control system** acts as the main command interface of HEPD with the satellite platform. The bidirectional CAN-bus interface allows to receive both satellite broadcast commands and ground-originated telecommands. It also allows to send command replies and instrument telemetry back. Power-on and power-off sequences, as well as the transition across different HEPD operational modes (SAFE, NOMINAL and STAND-BY), are performed via telecommands received onto the CAN-bus interface.

The Silicon Tracker **Front-end** allows to read out the signals on the silicon microstrips via a hybrid analog and digital electronics. The signals are then sent to the ADCs, and to a Digital Signal Processor that performs the zero suppression and sends digital data to the DAQ system. The PMT front-end and DAQ system similarly digitize signal amplitudes and forward them as digital data to the DAQ system.

The **Trigger System** continuously collects above-threshold digital information from the PMTs, starting digitization of interesting events. It also produces digital data about the triggered signal pattern that are sent to the DAQ system to be included in the scientific datastream.

The **Data Acquisition System**, as previously stated, collects data from the Silicon Tracker, the PMTs and the Trigger system, thus producing the scientific data packets that consist - for each acquired event - of the information on the impact point of the particle in the Silicon tracker and the energy released into the trigger planes, the calorimeter and possibly the veto system. These data are sent to ground using a data link, based on the RS422 protocol, which allows the transmission of the compressed scientific data to the Satellite On Board Data Handler (OBDH).

The **Housekeeping system** monitors the status of the instrument by periodically acquiring the parameters and status register of the subsystems via the internal control link bus (SpaceWire link). The housekeeping data are sent to the satellite and/or the DAQ in order to be integrated into the scientific datastream.

The **Power system** receives the 29 V primary bus from the satellite and provides supply voltages to the other electronic systems, and the bias voltages to the silicon sensors and the PMTs.

The block diagram of HEPD electronics is shown in figure 3.

The HEPD-01 electronics systems are physically hosted in seven boards, all located in a dedicated box connected to the HEPD baseplate (figure 4) apart from the Silicon tracker front-ends, which are located close to the detector. The seven boards are:

- CPU board - it hosts the Main Control system and the Housekeeping system;

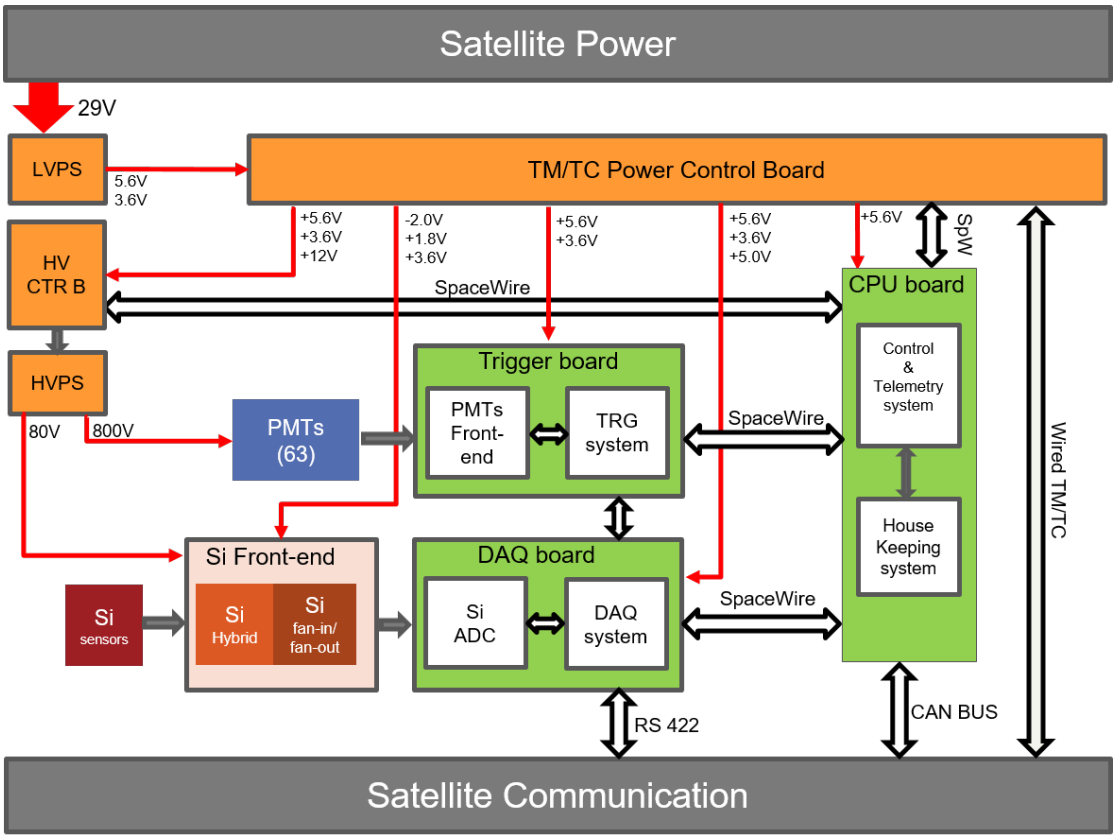


Figure 3: HEPD electronics block diagram - Connections with satellite and voltage distributions are shown.

- DAQ board - it hosts the Data acquisition system and the ADCs for the Silicon Front-end electronics;
- PMT/TRIGGER board - it hosts the front-end electronics of the PMTs and Trigger system;
- TeleMetry & TeleCommand (TM/TC) Power Control board (PCB) - it hosts a direct link to the satellite to receive specific hardware commands, and it distributes the digital voltages to all other electronic systems; it is part of the Power system;
- LVPS (Low-Voltage Power Supply) - it hosts the DC/DC converters (29 V to 5.6 V and 3.6 V, respectively) and provides the input voltages to the TM/TC PCB; it is part of the Power system;
- HV Control Board - it hosts the system controlling the High-Voltage Power Supply; it is part of the Power system;
- HVPS (High-Voltage Power Supply) - it hosts 10 HV units (0-1200 V) that provide bias voltages to the PMTs, and two HV units (0-150 V) that give voltage to the silicon sensors; it is part of the Power system.

Heat dissipation is managed by pure conduction through the aluminum mechanical modules where electronic boards are fixed. Board interconnections are provided by means of a dedicated harness made of Glenair Micro-D connectors[1] and Glenair Ambestrand braided EMI shield[2].

Each electronic board hosts two identical copies of the same electronics (main/hot and spare/cold side) for redundancy. Main and spare sides are completely independent of each other and cannot be powered at the same time. A second level of redundancy has also been applied to some important components of each board.

All the programmable logic arrays (FPGAs) used in HEPD belong to the ProASIC3E Microsemi family[3], which features several advantages for use in Space. The ProASIC3E family implements an on-chip non-volatile flash EEPROM that stores the configuration of the FPGA logic structure; this technology features good performance for what concerns radiation effects. For the programmable logic cells, there is no susceptibility to Total Ionization Dose (TID) up to at least 20 krad, while the overall cross-section for Single Event Effects (SEE) is of the order of 10^{-4} cm^2/kbit, with a component of Single Event Latchup per device (SEL/device) thet returns a negligible contribution to the overall SEE rate.

[1] https://www.glenair.com/micro-d/index.htm
[2] https://www.glenair.com/composite/d.htm
[3] https://www.microsemi.com/product-directory/fpgas/1690-proasic3

On the other hand, the flash configuration system (i.e., the part of the FPGA logic that is responsible for overwriting the previously stored logic configuration with a new one) has higher sensitivity to ionizing radiation, but it is disabled and never used in flight.

For the storage of non-volatile data (firmware as well as run-time data), the HEPD electronics relies on Ferroelectric Random Access Memories (FRAMs) and flash type memories. These FRAMs use a ferroelectric layer instead of a dielectric one, nonetheless offering the same functionalities as flash memories, but with noticeable advantages over them. FRAM memories require lower voltage to perform a write operation, which implies lower power consumption (1:21 ratio). Moreover, write operations are faster (16:1 ratio), and several tests show that *Single Event Upset*[4] response is good. Another, and probably most significant feature, is the device endurance: the number of write cycles is much higher than in flash memories and EEPROMs. The endurance to the write cycles is a crucial issue in the HEPD framework, since the FRAMs are not only used to store the program codes of the Digital Signal Processors (DSPs), but also detector calibration data that are calculated at every satellite orbit.

The following sections describe HEPD electronic subsystems in detail.

4.2. Control system

The Control system is responsible for the management of the detector and communications with the satellite platform. It manages the following functionalities:

- Communication with Satellite OBDH computer via CAN-bus (both nominal and redundant):
  - Management of TeleCommands (TCs);
  - Management of satellite information (broadcast);
  - Management of TeleMetry data (Fast and Slow TM);
- Storage of non-volatile information;
- Management of system configuration and in-flight operations (orbital configurations, calibration and acquisition runs);
- Configuration, test, and upgrade of the DAQ software via the Mail box interface;
- Temporal tag of runs and broadcast (local time, absolute time);
- Management, via SpaceWire link, of:
  - DAQ board;
  - PMT/TRIGGER board;
  - Low-Voltage control board (LVCB);
  - High-Voltage control board (HVCB).

The Control system is located in the CPU board. The board is divided into three areas: common, hot and cold. In the common area, the signals of the nominal and redundant CAN-bus links in the hot and cold areas are combined together by means of an impedance matching network. The electronics accommodated in the hot and cold areas are identical, and their architecture is based on the use of a Microsemi FPGA and a DSP of the class ADSP2189M by Analog Device [5]. The interconnection between the FPGA, DSP and various peripherals is shown in the block diagram in figure 5.

The main program that performs the board routines runs on the DSP, while the main functionalities of the FPGA are:

- Safe boot management;
- DSP Watch Dog management;
- Non-Volatile (NV) memory management;
- DATA memory (SRAM) management;
- SpaceWire Slow Control links management (see §4.2.1 for details);
- CAN-bus links management (see §4.2.1 for details).

After boot, the Control system is responsible for the power-on sequence and initialization of HEPD subsystems, following a proper sequence. The first step is

[4] A Single Event Upset (SEU) is a change of state in electronic devices caused by one single ionizing particle striking the component.

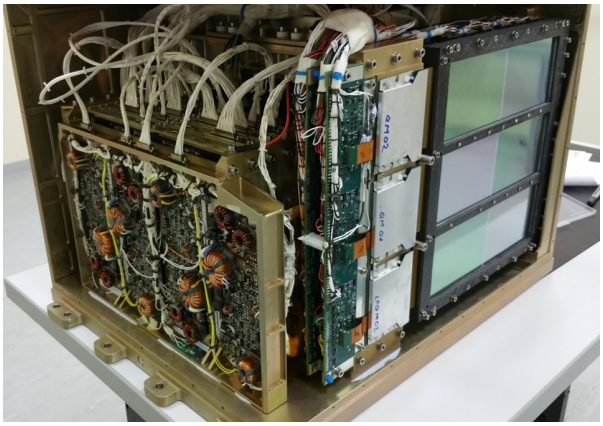


Figure 4: The electronics block and front-end electronics of the silicon tracker.

[5] https://www.analog.com/en/products/adsp-2189m.html

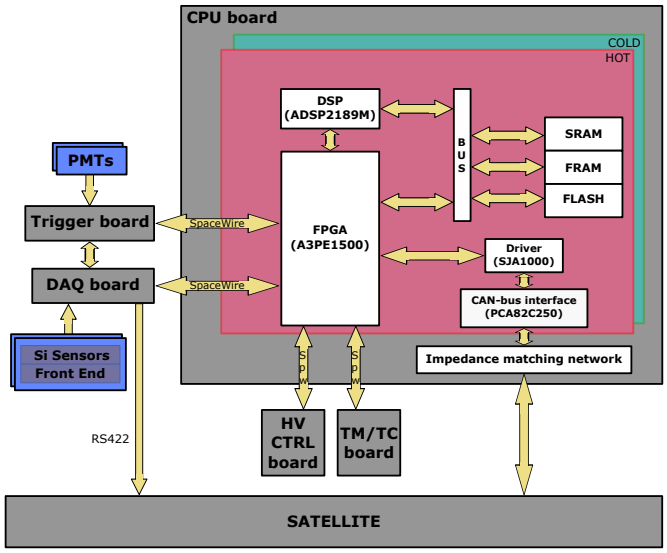


Figure 5: The CPU board block diagram

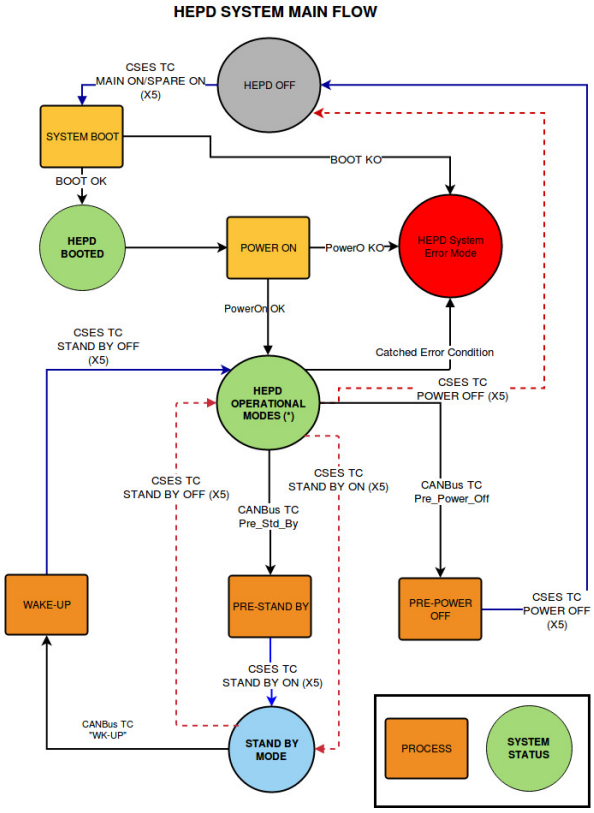


Figure 6: *HEPD Main flow: any main HEPD status is shown, together with TCs required to status change.*

to power each board on and immediately check its basic functionalities.

If all boards are booted correctly, HEPD is set either in NOMINAL or in SAFE mode (together called OPERATIONAL modes) depending on the saved configuration; if set in NOMINAL mode, the High-Voltage Control boards are powered at their nominal values, providing bias to the PMTs and Silicon ladders. At the same time, the Control system stores non-volatile information, such as the Boot Number and HEPD status before and after the first step, into the FRAM. On the other hand, if set in SAFE mode, the Low Voltage Power Supply and all boards are powered, but the PMTs and Silicon planes are not biased; this mode is mainly used for tests, in-flight health-check procedures at first power-on, and during some stages of the commissioning phase.

Once in either OPERATIONAL mode, the Control system starts a main loop during which data acquisition and calibration runs are configured and automatically executed depending on the orbital zone configurations[6].

From an OPERATIONAL mode, the HEPD can be powered off or set in STAND-BY mode (used for non acquisition zones such as geographic poles, where platform adjustments are performed) by means of dedicated telecommands, received from the satellite OBDH.

Figure 6 illustrates the flow chart of any HEPD status, the paths from any status to the others, and the corresponding telecommands that trigger HEPD status change.

Four types of broadcast messages are periodically sent by the satellite to all payloads on board CSES, providing information about position, velocity, time and attitude: OBDH time, GPS position and velocity, attitude and star tracker data. Satellite latitude and longitude are used by the Control system to identify the orbital region of the satellite, to decide the next operation to execute (either an acquisition or calibration run), and to change the configuration of the apparatus. The satellite timing information, together with CPU timestamp, is forwarded to the DAQ system for the temporal tag of acquisition and calibration runs.

During operations, the Control system updates the HEPD configuration and receives information about the status of each subsystem collected by the Housekeeping system. The status of the apparatus is periodically sent to the satellite as Fast Telemetry (Fast TM) and Slow Telemetry (Slow TM) with a cycle of 1 s and 8 s, respectively; the former basically contains the monitored status register of each subsystem, while the latter includes a larger set of parameters. All the acquired telemetries are transmitted to ground once a day.
HEPD configuration and board status, as well as complete broadcast and timing information, are stored into the SRAM and sent to the DAQ via Mail Box to be integrated into the scientific data.

The design and implementation of the software responsible for HEPD management - i.e., handling instrument

[6] In SAFE mode, since HVPS are switched off, the Trigger board generates fake triggers to test the whole electronic chain, including data transmission to the satellite via the RS422 link.

data acquisition, performing periodic calibration of sub-detectors, monitoring system status, performing data compression, and communicating with the satellite - has been reported in detail in [7].

4.2.1. CPU interfaces

This section describes the different communication interfaces implemented on the CPU board for data exchange with the satellite (CAN-bus link), electronic boards (slow control link) and DSP of the DAQ board.

- **CAN-bus interface**

The physics layer of the interface has been designed in accordance with the CAN-bus 2.0 protocol. On the CSES satellite, two physical CAN-buses (A and B) are used for redundancy purposes; nevertheless, only one bus must be active at any time. In order to manage the CAN-bus, the registers of the two controllers (A and B) are memory mapped into the FPGA memory, and the DSP uses the I/O space interface to access and configure these registers.

A custom driver has been designed, implemented and qualified to manage the two SJA1000 CAN-bus controllers by PHILIPS[7] on the CPU board, considering the timing constraints defined for CSES by the satellite designers. The transceivers used for the CAN-bus electrical interface belong to the PCA82C250 class produced by PHILIPS[8]. The driver performs the following tasks:

- initialization and configuration of both controllers: i.e., setting the filter and bit rate according to CSES specifications;
- management of both CAN-bus channels;
- management of the HEPD CAN-bus protocol:
  - reception of four different types of Broadcast messages;
  - reception of Telemetry pool process messages and transmission of the Telemetry responses within prefixed time constraints (Fast/Slow TM);
  - reception of single- and multi-frame telecommand messages and transmission of telecommand message acknowledge within prefixed time constraints.

All the payloads on board CSES-01 can be considered as nodes on the CAN network. Each message has a well defined identification, priority and structure in order to be recognized by the payloads.

- **Slow Control interface**

The communication between the CPU and the electronic boards is based on the SpaceWire Light standard, according to which the controllers are implemented in the FPGA of each electronic board. Network nodes are connected through a serial link with low latency and allowed speeds between 2 and 200 Mbits/s. Four channels are managed: DAQ board, HV board, Power Control board and Trigger board.

The CPU board always acts as the master of the control link, while the other electronic boards act as slaves; each board is designed to export a memory mapped interface, which can be accessed by the CPU by means of the I/O memory interface. The slow control link is continuously used to read the status and error register, and to configure each board. Each link is managed by a finite state machine as specified by the SpaceWire standard.

- **Mail box interface**

The last communication protocol (Mail box) regards data exchange between the DSP on the CPU board and the one of the DAQ board, the CPU one being the master of the protocol.

The protocol is implemented on the main FPGA of the DAQ board using 32-bit data registers and two control bits. The CPU accesses these registers via the slow control link, while the DSP of the DAQ uses the memory mapped space by means of the I/O interface. Specific registers are used to notify when a message from the CPU/DAQ must or can be read (i.e., the mail box is not busy), and to store data from the DAQ to the CPU or from the CPU to the DAQ. In order to avoid a conflict accessing the same register at the same time, the data register access from the CPU is possible after verification of the control bits, ensuring the mail box is not busy; once data are written, an interrupt is generated from the FPGA to the DAQ-DSP that extracts the data content, processes the command and writes a response onto a dedicated register.

4.3. Silicon Tracker Front-end and DAQ electronics

The readout of the Silicon Tracker is based on the IDE1140[9] front end chip, a 64 channel low-noise/low-power high-dynamic-range charge-sensitive preamplifier-shaper circuit. The 64 channels are connected to an output buffer by means of an analog multiplexer that allows the sequential readout. A total of 36 chips are used to read out the two sides of the silicon sensors, 18 chips each side (ohmic and junction side), mounted on three hybrid boards. Due to the high density of the detector channels, there is no redundancy. The six chips on each hybrid board are arranged in two groups for signal amplification and A/D conversion, as shown in Figure 7. Each hybrid board is connected to the DAQ board via a fan-in/fan-out where decoupling circuits are presents for all the control

[7] https://www.nxp.com/docs/en/data-sheet/SJA1000.pdf
[8] https://www.nxp.com/docs/en/data-sheet/PCA82C250.pdf
[9] https://ideas.no/products/ide1140/

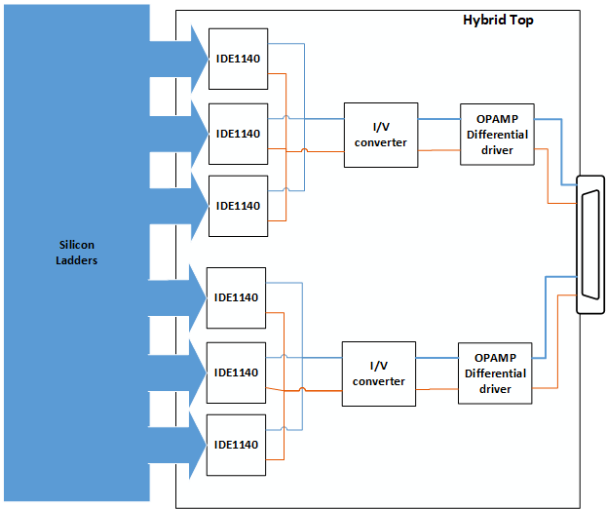


Figure 7: Hybrid Electronic block diagram. Only the analog signals are reported; the IDE1140 control signals are not shown.

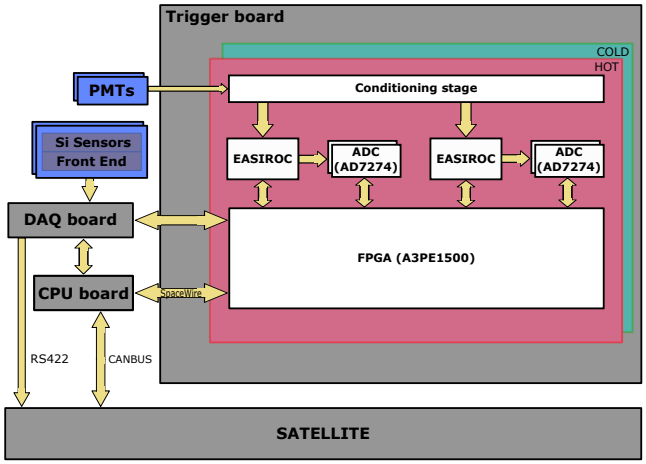


Figure 8: Block diagram of the trigger board.

signals generated by the DAQ board itself. The fan-in/fan-out board plays a crucial role also in power distribution: hot/cold redundant lines from the HVPS that bias the silicon detector, as well as hot/cold redundant lines from the LVPS that power the IDE1140 and the analog amplifier on the hybrid board, are all ORed in this board to properly power the hybrids and silicon detectors. Furthermore, this board receives the enable signals that allow to independently power on/off each detector column (two corresponding hybrids on both planes). Once a trigger is received, the DAQ board produces the HOLD signal for the IDE1140 chips, as well as the clock signal to control the analog output multiplexer. The amplified analog signals from the detector are digitized on the DAQ board using one ADC AD7274 every three front-end chips and producing a total of 27 kbit of raw data. The DAQ board applies a zero suppression algorithm in order to reduce data volume for transmission to ground.

4.4. Trigger/Calo/Veto front-end and DAQ electronics

The readout of the scintillator detectors (Trigger, Calorimeter and Veto) is performed through a dedicated board (Trigger Board) divided into two identical sections (Hot/Cold). Each section features an FPGA and two ASIC integrated circuits, followed by four ADCs. For redundancy, the signals coming from the PMTs placed on the same scintillator plane/paddle are driven to different front-end ASICs, with the exception of the LYSO plane where each cube is read out by only one PMT. In this way, a possible problem occurring in one of the ASIC chips does not harm the operation of the whole apparatus.

Figure 8 shows the block scheme of the Trigger Board. The board can handle 64 analog signals coming from the PMTs. The incoming signals are routed to a conditioning stage and then to two ASIC chips, which are used to integrate, shape and store the incoming signals. The analog signals coming from the ASICs are sent to the ADCs. The digitized signals are finally routed to the FPGA, which controls the whole process and handles the communication with the rest of the apparatus [8].

The ASIC performing the readout is the EASIROC by Weeroc[10]. This chip has been chosen because it represents a compact low-power solution to read out 32 channels (power consumption = 7 mW/channel). In addition, it has a wide dynamic range thanks to two independently-programmable variable-gain analog outputs (high gain and low gain), which offer multiplexed charge measurement from 160 fC up to 320 pC. These charge paths are composed of two variable gain preamplifiers, followed by two tunable shapers and a track-and-hold system that can be controlled by external signals. Slow shaping time can be adjusted between 25 and 175 ns for both low and high gain. A block scheme of the EASIROC chip is shown in figure 9.

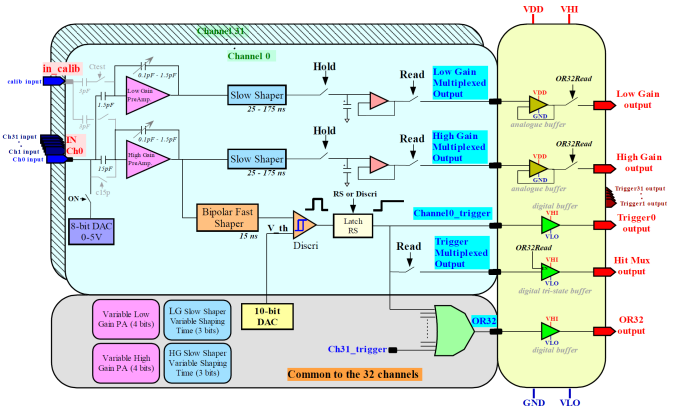


Figure 9: Block diagram of the EASIROC chip [9]

Since the EASIROC was originally developed to read out signals from silicon photomultipliers (SiPMs), there-

[10]https://www.weeroc.com/

fore requiring positive signals as an input, we have designed a conditioning stage to invert and attenuate the analog signals from any PMT. The input attenuation is necessary because the signals produced by the photomultipliers can reach 5 V, which is well above the maximum allowed input signal to the ASIC. The implemented attenuation factor is 30.

The EASIROC chip is also equipped with a fast shaper, fed by the signals from high gain preamplifiers, in order to generate a fast trigger output for each channel with adjustable threshold. These outputs are directly routed to the FPGA, where they are used to drive a more complex trigger logic generation described in section 4.5. The generated trigger signal drives data acquisition of the signals from the PMTs, allowing the track-and-hold cells of the EASIROC to save the amplitude of the preamplified and shaped signal at its peaking time.

The 32 high and low gain channels are then driven to two different ADCs to convert the EASIROC readout signals into digital ones. The ADCs used on the Trigger Board are produced by Analog Devices, Inc., model AD7274[11]. These ADCs are 12-bit, high-speed, low-power, successive approximation ADCs, and they feature throughput rates of up to 3 MSPS.

For each event, the digitized signals from the PMTs ($12\times32 = 384$ bits) are associated with other scientific data, such as the rate meters for each trigger configuration (8×32 bit counters), and the dead and live times of the whole instrument. These data are transmitted to the DAQ Board following the protocol described in section 4.6.

A slow control and command interface with the CPU has been designed and implemented to configure the EASIROC, and to configure the trigger generation algorithm. The acquisition and calibration runs are also controlled through this interface, described in section 4.2.1.

Finally, the Trigger Board implements 63 additional counters to measure single PMT "rate meters", which are transmitted along with scientific data. These counters measure the trigger rate of every PMT over 1 second, and allow to understand whether a single PMT is damaged or misbehaving, such that it can be masked and ignored in the generation of the trigger configuration.

4.5. Trigger system

The Trigger Board implements the trigger system of the apparatus. Besides the analog output, the EASIROC chip provides 32 individual digital output signals, one for each channel, and an additional signal that is generated via the logical OR of the single channel triggers ("OR32" in figure 9). These outputs are produced every time a signal exceeds a certain threshold value on the corresponding input. The threshold value is the same for all the channels, it can be changed through a CPU command, also from ground, by sending a command to the Trigger board through the slow control. The FPGA firmware is configured to issue a global trigger each time the trigger pattern of an event complies with a mask that can be chosen in a predefined set. When a global trigger is generated, the Trigger board starts the handshaking process described in section 4.6, in order to start the acquisition of scientific data from the tracker and the scintillator detectors.

HEPD can tap into 8 predefined "trigger masks" plus a configurable Generic Trigger Mask. Said T the "OR" of the six T_i trigger counters, P_i the i_{th} scintillator plane of the calorimeter, and L the "OR" of the 9 LYSO crystals, the eight masks are obtained by different logic combinations of T, P_i and L. The Generic Trigger Mask can be configured as any "AND" combination of calorimeter planes and trigger counters.

The different trigger masks define the aperture and the energy acceptance of the instrument: by requiring a deeper penetration of the particle inside the detector (i.e., using the trigger counters and a larger set of P_i scintillator planes in "AND" configuration), the geometric factor of HEPD decreases and the energy threshold for triggering increases.

Each of these predefined trigger masks can be used with different VETO settings: no veto, lateral veto alone, bottom veto alone, whole veto (lateral+bottom).

For each of the predefined masks, even when not selected for the online acquisition, a rate meter provides the corresponding trigger counting rate, allowing to simultaneously give independent estimates of count rates of different particle populations crossing the instrument, indirectly limiting the energy thresholds. These data are provided for each event and are part of the scientific data.

Depending on the selected HEPD acquisition mode, the Trigger system can work in different modes: either "Calibration" or "Event Acquisition" mode.

In Calibration mode, the Trigger board generates and sends fake trigger signals to the DAQ board, which acquires the ADC signals from the scintillators and silicon detector. Such data are sent to the DSP of the DAQ board for processing, in order to evaluate the pedestal, RMS and status of each silicon detector strip and each PMT. These calibration data are used online for the silicon detector data reduction, and offline for data analysis.

In Event Acquisition mode, the Trigger board generates and sends triggers to the DAQ board according to the specified threshold of the PMTs, on-line trigger mask configuration and VETO setting. The PMT signals, digitized in the Trigger Board, are then sent to the DAQ, where silicon data are acquired and processed.

In Event Acquisition mode, the Trigger Board also activates two counters to measure the dead and live times of the apparatus, which are appended to the scientific data sent to the DAQ. The calculation of both dead and live time of the apparatus is fundamental to evaluate the fluxes of incoming particles.

[11] https://www.analog.com/en/products/ad7274.html

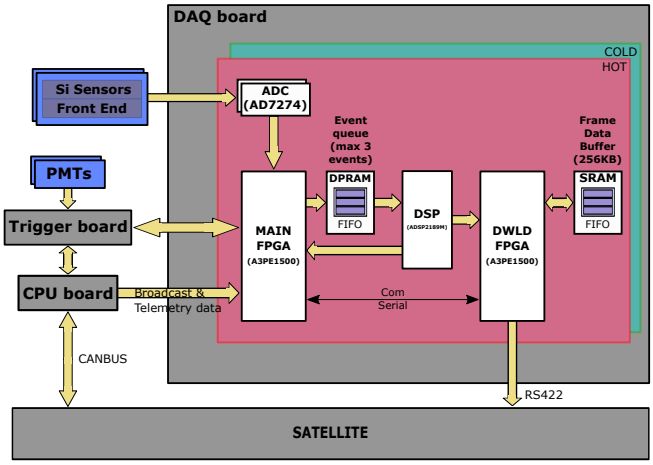


Figure 10: The Data Acquisition System involves DAQ board, Trigger board, CPU board and front-end electronics of the silicon and PMT detectors. All the scientific data are transferred to the DAQ board, where they are processed and compressed before transmission to the satellite via the RS422 link.

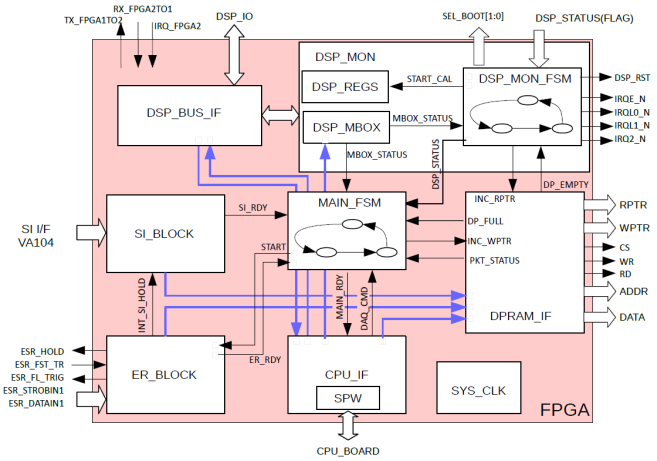


Figure 11: Block diagram of the firmware implemented on the Main FPGA. It is divided into six macro blocks, each one implementing a specific task: *SI_BLOCK* controls the silicon data acquisition and digitization; *ER_BLOCK* handles the communication with the Trigger Board for trigger generation; *CPU_IF* handles the communication with the CPU board; *DPRAM_IF* regulates the access to the DPRAM for the FPGA and DSP; *MAIN_FSM* is the finite state machine of the FPGA; *DSP_MON_FSM* is the monitor of the DSP finite state machine.

4.6. Data Acquisition System

The Data Acquisition System is responsible for the acquisition and management of the scientific data, as well as the processing of the digital signals and their transmission to the satellite. It is located in the DAQ board, but it also involves the CPU and Trigger board. The DAQ system manages the following main functionalities:

- configuration of the tracker detector for acquisition runs (Event Acquisition or Calibration mode);
- handshake with the Trigger board for the generation of the trigger pulse, coordination of all sub-systems for event acquisition, and calculation of the dead/live time of the apparatus;
- acquisition of tracker data and consequent signal compression;
- acquisition of PMT data from the Trigger board;
- scientific data compression and formatting;
- temporal tag of the event;
- transmission of the compressed scientific data to the satellite.

A block diagram of scientific data handling and all sub-systems responsible for acquisition is shown in Figure 10. The DAQ board is the main element: it contains a section with all the analog and digital circuits for the interface with the silicon front-end and the digitization of the silicon data; two FPGAs (called MAIN and DOWNLOAD); and a DSP. The other components of the DAQ are: two FRAMs used for the storage of the DSP code and other ancillary data (calibrations) that must be preserved after board power-off; a Dual-Port Random Access Memory (DPRAM) used for data exchange between the MAIN FPGA and the DSP; a static RAM (SRAM) used as a FIFO buffer for the final output of HEPD scientific data that must be transferred to the satellite. The operating frequency of the board is 48 MHz, good enough for computing power needs while keeping an acceptable electric power consumption.

When HEPD operates in NOMINAL mode, the generation of a trigger pulse is coordinated by the DAQ and Trigger systems through a handshake procedure. If a particle releases an above-threshold signal on the PMTs involved in the trigger mask (as defined in 4.5), the Trigger Board asserts the *fast_trigger_signal*, to which the DAQ responds with an acknowledge and inhibits the generation of new triggers. The acquisition of PMT and silicon signals starts. The PMT signals are digitized directly on the Trigger board, and then sent to the DAQ by using a simplified version of the serial protocol adopted for the CPU link. The acquisition of the silicon detectors is coordinated by a dedicated firmware block on the MAIN FPGA of the DAQ (*SI_BLOCK* in Figure 11).

The readout and following digitization of the Silicon tracker data are the main source of instrumental dead time. Other contributions to dead time come from the transfer of digitized PMT data from the Trigger Board to the internal memory of the MAIN FPGA, the write operation of silicon and PMT data to the DPRAM, and event compression performed by the DSP itself.

It has been observed that data transmission from the Trigger Board via the serial link induces a noise on the

readout of the silicon signals, resulting in a significant worsening of the RMS values of each channel. For this reason, the two operations are serialized, in spite of a slight increase in the total dead time. The time necessary to acquire and write all the detector data into the DPRAM, ready to be read out and processed by the DSP, is fixed because it only depends on the clock of the board. This time has been found to be $\simeq 2.5$ ms. The access to the DPRAM by the MAIN FPGA and DSP is managed and synchronizes through a handler present in the FPGA (*DPRAM_IF* in Figure 11).

This DPRAM works as a buffer that can contain up to 8 events. When the FPGA copies the acquired data to the DPRAM, it becomes also free to process a new trigger in parallel with the DSP processing the previous one. Only in the case when all the 8 DPRAM pages are full, the DSP stops the acquisition of a new event. The DPRAM acts like a FIFO where the first event written by the FPGA will be the first event processed by the DSP. Another firmware block in the MAIN FPGA (*DPS_MON* in Figure 11) operates as a monitor of the DSP; it controls the finite state machine of the processor by sending interrupt signals or resetting the DSP in case of an unexpected change of state.

The DSP compresses the Silicon data (reduced by a factor $\simeq 80$) using a custom "zero suppression" algorithm. Processed events are continuously stored into the SRAM; as soon as 4110 bytes are written, the DOWNLOAD FPGA sends a packet to the satellite via the RS422 link, adding a frame header and a second checksum at the end of the frame. In this way, event processing and transfer to the satellite are carried out in parallel, and all RS422 packets have the same fixed dimension as required by satellite specifications. The end of an acquisition run is handled by the CPU, which stops the acquisition after a given time window or when specific orbital conditions are met (e.g., when HEPD is about to be set in STAND-BY mode for satellite attitude adjustment operations).

4.7. Housekeeping system

The Housekeeping system is responsible for HEPD diagnostic routines, and, like the Control System, it is implemented as an application program running on the CPU.

During the power-on and operations phases, the Housekeeping system periodically polls each electronic subsystem via the slow control link, ensuring complete monitoring of the whole detector.
The Housekeeping system also periodically collects information about the High Voltage Power Supply modules - by reading each HV value - and the temperatures recorded by the sensors placed on the CPU and Trigger boards. Such information is sent to the Control System and then relayed to the satellite through Fast Telemetry (TM) and Slow TM with cycles of 1 s and 8 s, respectively.

The Fast TM contains the monitored status register of each subsystem, while the Slow TM includes more parameters, such as error registers for each electronic board, the value of the temperature sensors placed on the CPU and Trigger Boards, the monitored values of the high voltages for the PMT and silicon detectors, and the last TC received.
Part of the monitored data (the board status) is also sent to the DAQ via the Slow Control link to be integrated into the scientific data (Run Header and Tail).

At the same time the Housekeeping system monitors the good functionality of PMTs by reading the 63 single PMT rate meters provided by the Trigger board. Those values can be analyzed offline to identify broken or bad working PMTs (for example, noisy PMTs) that could affect the Trigger system efficiency; these PMTs can be excluded from the trigger by means of a dedicated configuration telecommand.

The collected PMT information, as well as temperature and timing, are sent to the DAQ via the Slow Control link in order to be integrated into the scientific data.

A block diagram of the housekeeping data handling and transmission is shown in Figure 12.

4.8. Power system

The power supply subsystem provides low voltages (main power supply unit, LVPS) to the detector electronics, and the high voltage (HV) bias for PMTs and silicon planes (secondary power supply unit, HVPS). A schematic diagram of power supply distribution is shown in Figure 3.

4.8.1. Low-Voltage Power Supply (LVPS)

The Low Voltage Power supply (LVPS) unit includes:

- two LV modules, customized versions of CAEN[12] S9074 and S9053 DC/DC converters, which receive the main 29 V power line input from satellite and deliver the appropriate voltages (5.6 V and 3.6 V, respectively) to the rest of the system via the Low Voltage Control Board (LVCB);
- the LVCB, which a) communicates with the satellite for wired telecommands and telemetries concerning the status of the LV modules, and b) generates and controls the various supply voltages for the rest of the system.

For the sake of redundancy, each LV module is doubled, while the LVCB consists of two identical parts (hot and cold).

The LV module is a high-reliability DC/DC converter designed for space applications; the output current is

[12] https://www.caen.it/

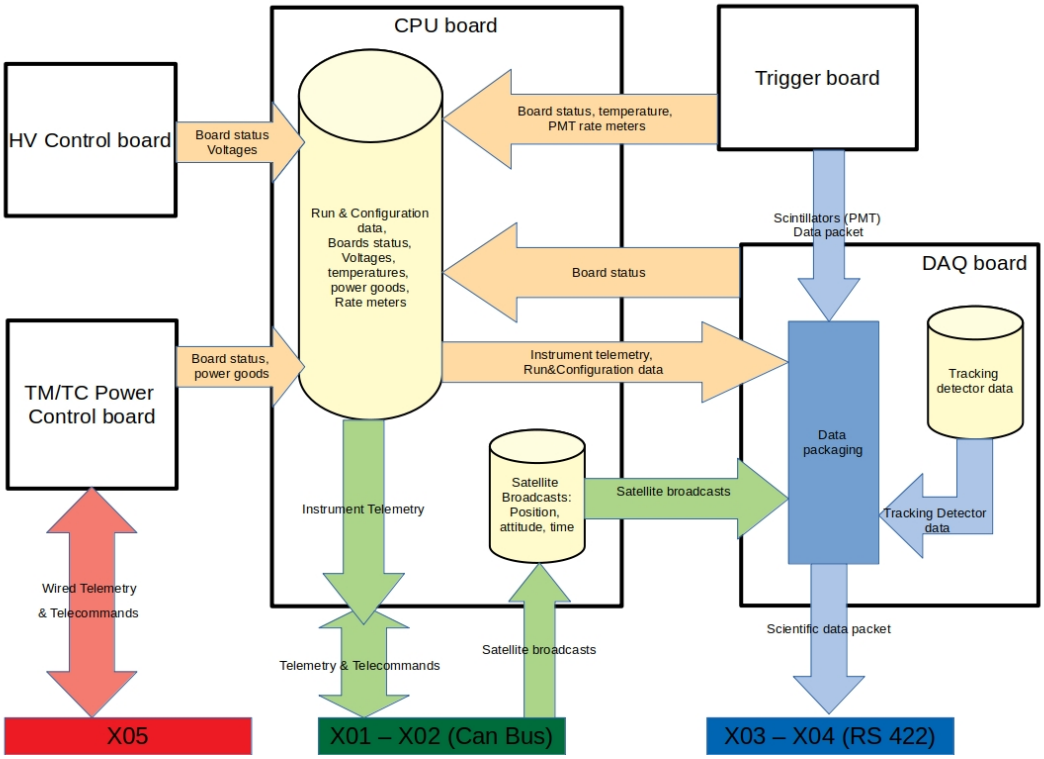


Figure 12: Block diagram of scientific and housekeeping data handling and transmission.

pulse-by-pulse controlled, in order to protect the circuits from overload and short circuit. The main features of the module are summarized here:

- radiation tolerance up to 30 krad;
- device protection to keep operating parameters within safe limits: input over/undervoltage control, output overcurrent control, maximum duty-cycle control, solid-state fuse;
- guaranteed DC isolation between power input and output circuitry up to voltage differences of 250 V;
- output voltage temperature stability within 0.5 mV/°C;
- line regulation better than 35 mV and 2 mV for the 5.6 V and 3.6 V module, respectively, with input voltage in the range from 26.5 V to 30.5 V;
- load regulation better than 220 mV and 130 mV, respectively, over the full dynamic range and recommended temperature range (-20°C to +70°C);
- peak-to-peak output ripple < 40 mV and 20 mV, respectively, in the bandwidth up to 20 MHz;
- typical power efficiency of 79% at full output power.

4.8.2. High-Voltage Power Supply (HVPS)

The High Voltage Power Supply (HVPS) unit is composed by the following electronic subsystems assembled in a common metallic frame:

- 10 step-up HV modules with negative output (up to 1200 V DC) for PMTs (each module serves several PMTs between 4 and 7);
- 2 step-up HV modules with positive output (up to 150 V DC) for the silicon planes (one module serves one silicon plane);
- HV control board (HVCB) to set and monitor the HV output values and interface with the CPU board.

A block diagram of the HVPS is shown in Figure 13.

Like LV modules, each HV module is doubled for redundancy, while the HV control board comprises two identical parts (hot and cold). Each pair of hot/cold HV output cables are short-circuited into a dedicated diode protection circuit PCB housed externally to the HVPS on the support mechanics of the unit, which produces a single HV output line in turn split into a number of cables adequate to reach the corresponding loads.

The employed HV module is Aerospazio HV3, a high-reliability HV DC/DC converter [13] unit designed for space

[13] https://www.aerospazio.com/high_voltage_DC-DC_converters.html

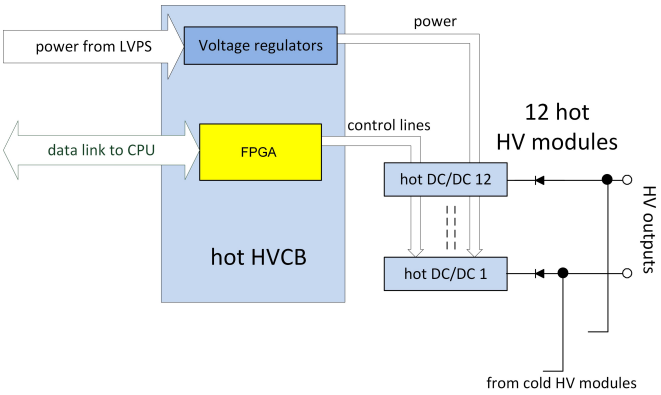


Figure 13: Block diagram of the HVPS hot part.

applications, optimized for low ripple, low power consumption, wide operating temperature range, compact size and light weight. The circuit design of this unit is suitable for generation of both negative and positive HVs, for PMTs and silicon planes, respectively. The main features of the module are summarized here:

- maximum HV output: ±1200 V;
- output voltage analog monitor line;
- programmable output current limiter (maximum 500 μA) with overcurrent status and current monitor lines;
- output load regulation stability within 0.4%;
- output voltage linearity better than 0.4%;
- output voltage temperature stability better than 100 ppm/°C;
- peak-to-peak output ripple < 25 mV (in the bandwidth 20 Hz to 20 MHz).

To guarantee proper operation under any pressure condition from room to space environment, and taking into account the compactness of the unit which implies reduced distances between circuit elements, the HV module PCB has been installed in a housing frame filled with potting substance (Arathane 5753-A/B LV) that assures a high enough dielectric constant to avoid discharges between the circuit parts at different voltages. The low-outgassing properties of the potting material are compatible with the requirements for space application.

The main functionalities of the HVCB allow to:

- configure the HV value (with 0.1% resolution) for single HV modules by means of dedicated voltage control lines;
- switch on/off single HV modules by means of dedicated enable lines;
- check for SEUs in the critical voltage setting registers;
- interface with the CPU board (SpaceWire light link).

The setting of the HV voltage for a given channel is operated by the HVCB on-board logics either automatically at power-on or when a suitable command is sent by the CPU board. The change in the HV voltage can be operated through a sequence of steps of max 300 V at 1 s time intervals, to properly limit the inrush current at each step. The HV output resolution is 0.1%, while the combination of channel fabrication tolerances and non-linearities returns a total uncertainty < 1% on the actual HV value with respect to the nominal one.

The setting of the HV output is operated on the HVCB by driving the voltage set analog input V_SET of the HV module through the output of a RC-RC filter (time constant order of 1 ms). The RC-RC, in turn, is fed by a by an FPGA output producing a square wave with fixed period (22 μs, i.e., much smaller than the filter time constant) and variable duty cycle; the filter output is therefore a voltage level that is proportional to the chosen duty cycle. With this method, the accuracy of the analog V_SET value is given by the accuracy of the duty cycle, which has negligible dependence on environmental conditions and aging of devices.

Though SEUs in HVCB logics are highly improbable with the expected in-orbit charged-particle fluxes, each HV setting register is individually protected by an Error Detection And Correction (EDAC) Hamming function, with continuous (each 50 ns) automatic correction of single bit upset and detection of double bit upset (with internal alarm raised while the HV setting is automatically brought to 0). The fast correction rate is such that, taking into account the RC delays in the HV line, any upset has no significant effect on the corresponding HV output voltage.

The actual HV value of each channel can be monitored through both the readout of the setting register and the analog monitor output of the HV module. This monitor output voltage linearly replicates the HV output (in a voltage range scaled by a factor 300) and is in turn digitally converted by a dedicated 10-bit ADC (Analog AD7276[14]) to fill the AN_MON internal register of the FPGA. The overall combined fabrication tolerance + non-linearity of the monitor line with respect to the actual HV output voltage is within 3%.

At power-on, the on-board logic performs a fixed sequence of operations, in such a way that, even in the absence of any command from the CPU board (because of a failure of the command interface), each HV channel is set to an adequate default value: the default values are loaded during the final FPGA configuration (HVCB acceptance test). Though they differ from the optimized values, they are still capable of assuring satisfying operation

[14] https://www.analog.com/en/products/ad7276.html

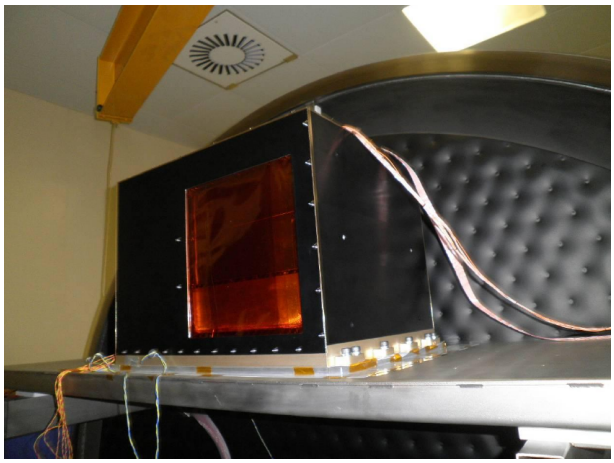


Figure 14: HEPD Flight Model (FM) in the thermal vacuum chamber at the SERMS facility in Terni (Italy) during the payload acceptance campaign in November 2016.

of the PMTs and silicon planes. The automatic sequence with ramp-up of HV outputs to default values can be interrupted if a suitable command from the CPU board arrives within a predefined time (4 s) from HVCB power-on.

The interface with CPU boards allows commands to be received to switch on/off single HV modules, to set HV values, and to read voltage monitors and alarm conditions (such as double-bit upset in the HV set register or failure in the board power circuitry).

5. Test and Qualification Campaigns

In compliance with the model philosophy of the project arranged with the Chinese DFH Satellite Co. - located in Beijing (China) - four HEPD models have been developed.

The Electrical Model (EM) is a mock-up of HEPD where all electric and electronic interfaces (power bus, TM/TC, CAN-bus and RS422) with satellite are developed. This model was realized to demonstrate the hardware and software design of the payload, to verify the electric and electronic compatibility between payload and satellite, and to test the compatibility between HEPD and its Electrical Ground Support Equipment (EGSE). The HEPD EM was successfully tested at the DFH test facility in October 2014.

The Structural and Thermal Model (STM) is a complete mechanical mock-up with dummy sensors and electronics in place of electronic boards to emulate the real heat dissipation. This model was developed to validate the structural and mechanical design, to test the payload thermal control design, and to verify the compatibility between HEPD and its Mechanical Ground Support Equipment (MGSE). Also the HEPD STM was successfully tested at the DFH test facility in October 2014.

The Qualification Model (QM), identical to the flight version of the payload, was developed and submitted to a complete qualification test campaign to assess the design and the technological solutions, and to demonstrate its performance.

In compliance with the enviromental test requirements, the QM underwent an extensive qualification test campaign, which included pyroshock, sinusoidal and random vibration, thermal-cycling and thermal vacuum tests. These tests were carried out at the SERMS Laboratory in Terni (Italy) between May and August 2016.

Specifically, in the pyrotechnic shock test HEPD QM was exposed to two different shocks along each of its three axes. The Shock Response Spectrum (SRS) of this test had frequencies ranging from 600 to 4000 Hz and acceleration up to 1000 g. A Sinusoidal vibration test was performed along the three axes with amplitude 7.5 mm in the frequency range 10-20 Hz and 12 g acceleration in the frequency range 20-100 Hz with a scan rate of 2 oct/min. A Random vibration test was carried out along the three axes in the frequency range 10-2000 Hz with a total GRMS 11.3 g and 2 minutes of loading duration.

The thermal-cycling test was performed in a climatic chamber at ambient pressure: 25.5 cycles were run in a temperature range between $-30°$C to $+50°$C with a temperature gradient of (3-5)°C/min and a dwell time of ≥ 4 hours. The dwell time is the minimum required time to achieve the thermal stabilization of the tested device.

The thermal vacuum test was carried out in a large vacuum chamber at a pressure $\leq 6.66 \times 10^{-3}$ Pa: six cycles were run in a temperature range between $-30°$C and $+50°$C. The chamber temperature gradients were 2°C/min and 1°C/min during the heating and cooling, respectively, with a dwell time of ≥ 4 hours.

Each cycle of thermal-cycling and thermal vacuum tests included different steps corresponding to different operations for HEPD, such as data acquisition, calibration, stand-by or power off, in order to simulate in-flight procedures. During these operations, HEPD telemetry packets were continuously monitored to check for anomalies. The EGSE was used to power and manage HEPD, in order to change its status and operating mode according to test requirements.

Once the QM successfully passed the qualification test campaign in Italy, it was delivered to DFH. Then, HEPD QM was installed on the QM model of the satellite and successfully tested at the DFH test facility in October 2016. It was returned to the Italian side the following month.

The acceptance campaign for the Flight Model (FM) was carried out between October and November 2016. In compliance with ECSS (European Cooperation for Space Standardization) standards, no pyroshock test was performed. All other tests were performed under the same conditions as the QM, but with lower qualification levels or temperatures: a sinusoidal vibration test was performed along the three axes with amplitude 5.0 mm in the frequency range 10-20 Hz and 8 g acceleration in the

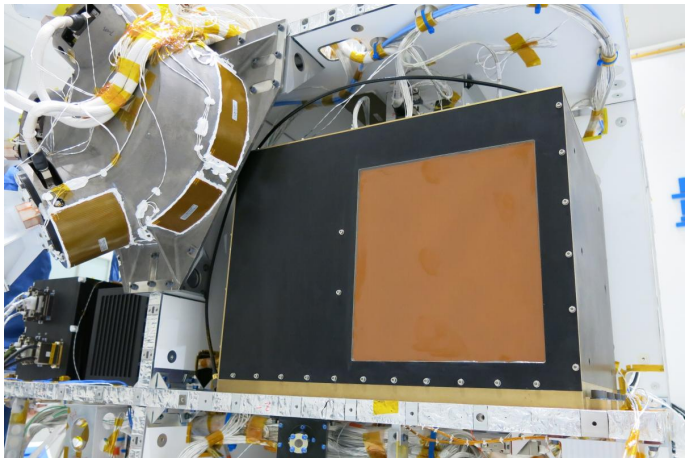
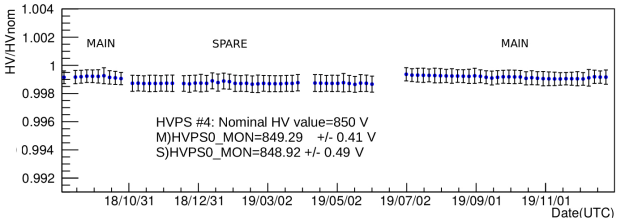
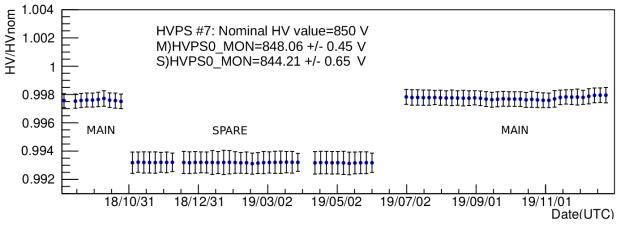


Figure 15: HEPD Flight Model installed on CSES satellite at DFH Satellite Company, Ltd. (Beijing, China)



(a) HVPS 4



(b) HVPS 7

Figure 16: Variation of Monitored HV values with respect to the nominal ones for main/spare sides; mean values over the whole period for each side are also specified. Monitored HV values have been averaged over 5 days for the period September 2018- December 2019.

frequency range 20-100 Hz with a scan rate 4 oct/min. A random vibration test was carried out along the three axes in the frequency range 10-2000 Hz with a total GRMS 7.55 g and 1 minute of loading duration. For the thermal-cycling test, 17.5 cycles were run in a temperature range between $-20°$C to $+45°$C. For the thermal vacuum test, 4.5 cycles were run in a temperature range between $-20°$C and $+45°$C. Figure 14 presents the HEPD Flight Model in the thermal vacuum chamber at the SERMS facility in Terni during the payload acceptance campaign in November 2016.

The acceptance test campaign was successfully passed by HEPD FM. Therefore, it was delivered to DFH in December 2016.

In January 2017, HEPD FM successfully passed a stand-alone assembly and integration verification procedure carried out by means of its EGSE. Then, it was cleared for the installation on CSES satellite at DFH, as shown in figure 15. Sinusoidal and random vibration tests, as well as thermal-vacuum and thermal balance tests, were successfully performed on board CSES satellite between February and April 2017. Magnetic cleanliness and aging tests were completed in May 2017.

Before delivery to China, the HEPD FM was tested under particle beams in different beam test facilities. In October 2016, the detector was exposed to electron beams of 30, 60, 90 and 120 MeV at the INFN-LNF BTF (Beam Test Facility) in Frascati (Italy). In November 2016, it was exposed to proton beams of 37, 51, 70, 100, 125, 154, 202, and 228 MeV at the Trento Protontherapy Center in Trento (Italy). Results from the teast-beam calibrations of HEPD can be found in [10].

6. In-flight performance

CSES satellite was launched from the Jiuquan Satellite Launch Center in the Gobi desert (Inner Mongolia, China) on February 2^{nd}, 2018. Four days later, the HEPD instrument was switched on for the first time. All detectors were functioning properly.

After launch, a long commissioning phase (February–July 2018) started, during which several on-board configurations were implemented and tested in order to optimize the operational parameters of the instrument. Since August 2018, HEPD has been in science run and data-taking mode.

6.1. Housekeeping data

The status of the apparatus is continuously monitored by the Housekeeping System. The Telemetry data are mostly used to check the stability of the electronics, in order to identify anomalous behaviors and - if necessary - to investigate the possible source of malfunctions. An example of the continuous monitoring of the high voltage values that bias the PMTs is given in figure 16, where monitored HV values divided by the nominal values are shown over more than 1 year of life (September 2018 - December 2019), for two HVPS (no.4 and no.7) taken as an example. The HVPSs show a very stable behavior, with a variation below 0.5%. The discontinuity visible in the period November 2018 to July 2019 is due to the switch from the main to the spare side of the electronics, with different offsets for the two different High Voltage Power Supplies.

6.2. Scientific data

In addition to housekeeping data, also the scientific output is continuously monitored in order to perform offline calibration and check the stability of the detector response.

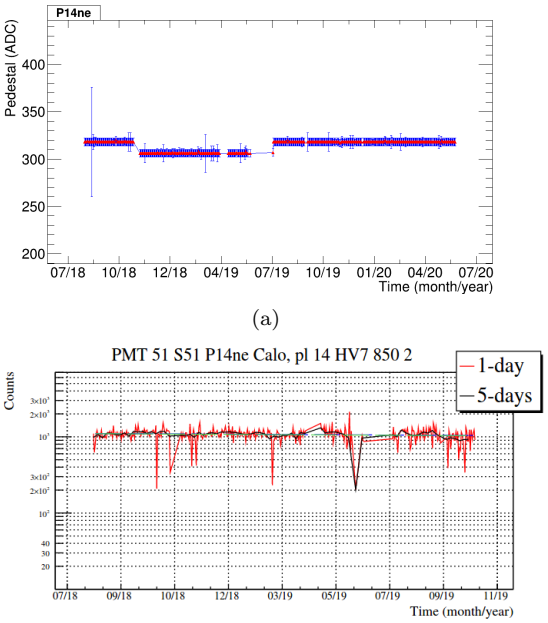


Figure 17: a) Pedestal of a specific PMT in plane 14 of the calorimeter, as calculated online during the calibration procedure. The steps at November 2018 and July 2019 are due to transitions from main side to spare electronics and viceversa. b) Rate meter for the same PMT by average over 1 day (red curve) and 5 days (black curve).

From the end of the commissioning operations to the end of June 2020, more than 10000 hours of acquisition have been collected, corresponding to about 10000 CSES orbits.

PMT output is checked by studying mean and variance of the pedestal for every channel. These quantities are calculated for each CSES orbit during the normal functioning of HEPD, and they show a very good stability over the entire period. As an example, in figure 17a , the pedestal of one of the two PMTs of the 14^{th} plane is reported as a function of time. Each point corresponds to the value of the pedestal obtained from a single calibration run. A sudden decrease of the pedestal during the period from November 2018 to July 2019 can be observed, due to the switch from the main to the spare side of the electronics, while no significant variations are visible when the pedestals are measured under the same electronic conditions. Figure 17b shows the rate meter (i.e., the number of events that released a signal above the PMT threshold in 1 second) for the same PMT, by averaging over a single day (red curve) and five days (black curve). The single day trend shows some sharp depressions that can be explained either by intervals in which the detector was powered off or missing data (for example, because of data corruption during transmission to the ground). The black curve shows a rather constant trend, as expected for a PMT in the 14^{th} plane, placed deep inside in the calorimeter, and for this reason not sensitive to fluctuations of low-energy particle fluxes (e.g., during geomagnetic storms or solar events).

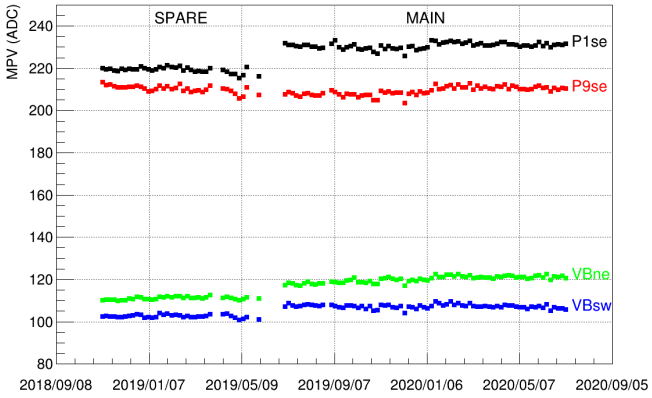


Figure 18: "mip" response as a function of time (from November 2019 until September 2020, in spare and main electronic acquisition) for four PMTs; one concerning the first calorimeter plane (black line), one for the 9th plane (red line), and two for the bottom veto plane (green and blue lines).

The acquisition of particles with relativistic speed, called minimum ionizing particles ("mip"s), is also used to monitor and calibrate the PMT energy response. Although it is not possible to individually select mips by means of HEPD (due to the impossibility to measure the energy of particles not fully contained within the calorimeter), events passing through the entire instrument and bottom veto plane without releasing signal on the lateral veto, represent a sample statistically dominated by mips. Figure 18 shows the mip response as a function of time (from November 2019 until September 2020, in both spare and main electronic configuration) for four PMTs; one concerning the first calorimeter plane (black line), one for the 9th plane (red line), and two for the bottom veto plane (green and blue lines). On the Y axis the Most Probable Value (MPV) of the PMT ADC count is reported. The MPV is obtained by a Landau fit on the PMT global signal distribution. The MPV behavior looks stable over the period considered, suggesting a stable state of the electronics over time.

Eight rate meters, one for each trigger mask defined in §4.5, are also implemented. In figure 19 , three of them are reported for the configurations:

- T (only trigger plane);
- T & P1 (trigger plane and first calorimeter plane);
- T & P1 & P2 (trigger plane and first two calorimeter planes).

The three rate meters as a function of L-shell (McIlwain parameter [11]) and time are shown for the period from August to September 2018; in this time interval a geomagnetic G3-class storm occurred. The initial phase of the storm started on late Aug 25^{th} (as it can be inferred

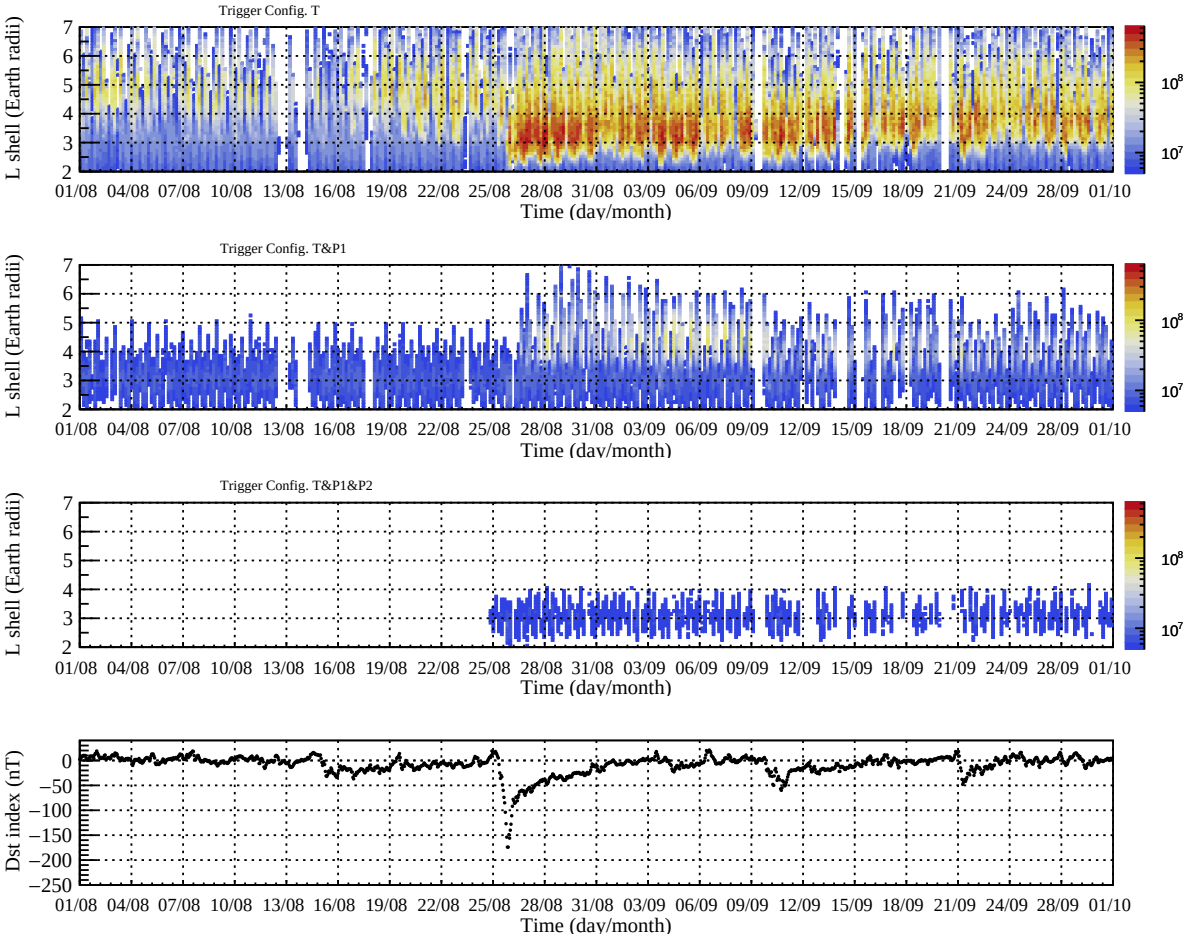


Figure 19: Rate meter of three different trigger configurations during the G3 geomagnetic storm of August 25-26, 2018 (marked by strong decrease in the Dst index shown in the bottom panel) increasing the number of planes used for the generation of the trigger.

from the trend of the Dst index in the bottom panel of figure 19) and the injection of low-energy particles is visible from the increase in counts detected by the first rate meter (figure 19 top panel). Adding more planes in the trigger configuration results in increasing the energy threshold for the detection, thus reducing the particle rate; that is why the second and third rate meters (figure 19 central panels) only detect very faint increases at storm onset.

So far, HEPD has been functioning in orbit as expected after 33 months of lifetime. The measurement of the galactic protons flux in the interval 40–250 MeV has been successfully concluded, as reported in [12].

7. Conclusion

In this article, we have described the electronics architecture of the High Energy Particle Detector (HEPD), an instrument that has been flying on board the Chinese CSES satellite since February 2018. HEPD electronics has been designed according to the general requirements imposed by satellite operations: in this specific case, limited power (43 W), limited temperature operating range (operating temperature: -10 °C ÷ +35 °C), limits on max number of data transferable to the ground per day (data budget: 50 Gb/day), and scheduled satellite lifetime of 5 years.

Both housekeeping and scientific data have allowed us to verify that the instrument is working according to nominal in-flight parameters, and that no substantial criticality has been observed in the first 33 months of life. The measurement of the galactic protons flux in the interval 40÷ 250 MeV has been successfully concluded, and data analysis is continuing in order to fulfill the scientific objectives of the mission.

Acknowledgments

This work was supported by the Italian Space Agency in the framework of the “Accordo Attuativo 2020-32.HH.0 Limadou Scienza+” (CUP F19C20000110005) and the ASI-INFN agreement n.2014-037-R.0, addendum 2014-037-R-1-2017. We would like to thank the staff of Electronics and Detectors Service (SER) of INFN Section of Naples,

in particular V. Masone, A Boiano, A Vanzanella and A. Anastasio, for their strong and undivided support all along this project.

References

[1] X. Shen, *et al.*, *The state-of-art of the China Seismo-Electromagnetic Satellite mission*, Science China Technological Sciencies, vol. 61, no. 5, pp.634-642, May 2018.

[2] S. Alexandrin, *et al.*, *High-energy charged particle bursts in the near-Earth space as earthquake precursors*, Ann. Geophys. 21 (2003) 597.

[3] V. Sgrigna, *et al.*, *Correlations between earthquakes and anomalous particle bursts from SAMPEX/PET satellite observations*, J. Atmos. Sol.-Terr. Phys. 67 (15) (2005) 1448.

[4] R. Battiston, *et al.*, *First evidence for correlations between electron fluxes measured by NOAA-POES satellites and large seismic events*, Nuclear Phys. B Proc. Suppl. 244 (2011) 249.

[5] P. Picozza, *et al.*, *Scientific Goals and In-orbit Performance of the High-energy Particle Detector on Board the CSES*, The Astrophysical Journal Supplement Series, vol. 243, pp. 16, July 2019.

[6] G. Ambrosi, *et al.*, *The HEPD particle detector of the CSES satellite mission for investigating seismo-associated perturbations of the Van Allen belts*, Sci China Tech Sci, 2018, 61: 643-652.

[7] A. Sotgiu, *et al.*, *Control and Data Acquisition Software of the High-Energy Particle Detector on board the CSES Space Mission*, Software: Practice and Experience, in press.

[8] V. Scotti and G. Osteria, *The electronics of the HEPD of the CSES experiment*, Nuclear and Particle Physics Proceedings 291-293 (2017) 118. https://doi.org/10.1016/j.nuclphysbps.2017.06.024.

[9] Callier, S. et al., *EASIROC, an Easy & Versatile ReadOut Device for SiPM*, Physics Procedia, Volume 37, 2012, Pages 1569-1576, ISSN 1875-3892, https://doi.org/10.1016/j.phpro.2012.02.486.

[10] G. Ambrosi, *et al.*, *Beam test calibrations of the HEPD detector on board the China Seismo-Electromagnetic Satellite*, Nuclear Inst. and Methods in Physics Research, A 974 (2020) 164170, September 2020.

[11] McIlwain, *et al.*, *Coordinates for mapping the distribution of magnetically trapped particles*, J. Geophys. 349 Res., 66 (11), 3681– 3691, 1961.

[12] S. Bartocci, *et al.*, *Galactic Cosmic-Ray Hydrogen Spectra in the 40–250 MeV Range Measured by the High-energy Particle Detector (HEPD) on board the CSES-01 Satellite between 2018 and 2020*, The Astrophysical Journal, 901:8 (7pp), 2020 September 20.