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# Design and performance of the prototype Schwarzschild-Couder telescope camera

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**Abstract.** The prototype Schwarzschild-Couder Telescope (pSCT) is a candidate for a medium-sized telescope in the Cherenkov Telescope Array. The pSCT is based on a dual-mirror optics design that reduces the plate scale and allows for the use of silicon photomultipliers as photo-detectors. The prototype pSCT camera currently has only the central sector instrumented with 25 camera modules (1600 pixels), providing a 2.68-deg field of view (FoV). The camera electronics are based on custom TARGET (TeV array readout with GSA/s sampling and event trigger)

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application-specific integrated circuits. Field programmable gate arrays sample incoming signals at a gigasample per second. A single backplane provides camera-wide triggers. An upgrade of the pSCT camera that will fully populate the focal plane is in progress. This will increase the number of pixels to 11,328, the number of backplanes to 9, and the FoV to 8.04 deg. Here, we give a detailed description of the pSCT camera, including the basic concept, mechanical design, detectors, electronics, current status, and first light. © 2022 Society of Photo-Optical Instrumentation Engineers (SPIE) [DOI: [10.1117/1.JATIS.8.1.014007](https://doi.org/10.1117/1.JATIS.8.1.014007)]

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## 1 Introduction

The current energy frontier for high-energy gamma-ray astronomy is around 50 TeV, and an increased detection area is vital to future high-energy gamma-ray instruments. Along with ground-based extensive air shower arrays (e.g., HAWC or LHAASO), large arrays of imaging atmospheric Cherenkov telescopes (IACTs) are the most promising instruments to push the energy frontier to higher energies.<sup>1</sup>

Earth’s atmosphere is opaque to very-high-energy (VHE;  $\geq 100$  GeV) photons, and the fluxes are too small for satellite detection; thus, they must be detected from the ground through indirect means. VHE gamma rays initiate extensive air showers. The shower constituent particles move faster than the speed of light in the atmosphere and thus emit Cherenkov radiation. Showers reach their maximum development at around 10 km above sea level. Cherenkov angles range from 0.8 deg at 10 km above sea level to 1.4 deg at sea level. For vertical showers, these opening angles produce a Cherenkov light pool with a radius of about 120 m at 1500 m above sea level.<sup>2</sup> IACTs record the Cherenkov light produced by these showers. At energies  $>100$  GeV, cosmic rays are much more abundant than gamma-ray events and hence are the primary backgrounds at these energies.<sup>2</sup>

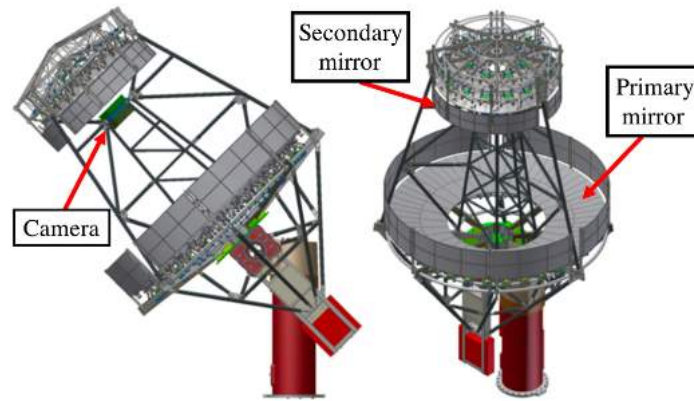
The Cherenkov Telescope Array (CTA) is a ground-based observatory for VHE gamma rays. The CTA “alpha configuration” will have two sites, one in the northern hemisphere in La Palma, Spain, and one in the southern hemisphere in Paranal, Chile. The array will cover 3 km<sup>2</sup> in the south and 0.25 km<sup>2</sup> in the north and will have telescope spacings of 100 to 300 m.

To cover a wide energy range, CTA will use three different sizes of telescopes: small-sized (SST), medium-sized (MST), and large-sized (LST). These three sizes are designed to access different energies between 20 GeV and 300 TeV. The northern site will have four LSTs and nine MSTs. The southern site is planned to have 14 MSTs and 37 SSTs.<sup>3</sup>

Since the highest energy photons from extragalactic sources are absorbed by collisions with the extragalactic background light, and the preponderance of galactic sources is in the southern hemisphere, only the southern site includes SSTs, which are needed for good sensitivity at 100 TeV and above. Together, these sites will cover the whole sky and will have approximately an order of magnitude greater sensitivity than current instruments.<sup>3</sup>

The prototype Schwarzschild-Couder (SC) telescope is a candidate for an MST for CTA and is located at the Fred Lawrence Whipple Observatory in southern Arizona. An artist’s rendition of the pSCT is shown in Fig. 1.

The pSCT will be sensitive to gamma-rays with energies between 100 GeV and 10 TeV. Most IACTs use single-mirror Davies-Cotton or parabolic optics; however, the pSCT uses a dual-mirror design with a 9.66-m primary mirror and a 5.4-m secondary mirror. SC optics produce an excellent optical point spread function (PSF), a wide field of view (FoV), and a much smaller plate scale than traditional Davies–Cotton optics.<sup>5</sup> The small plate scale (1.625 mm per minute of

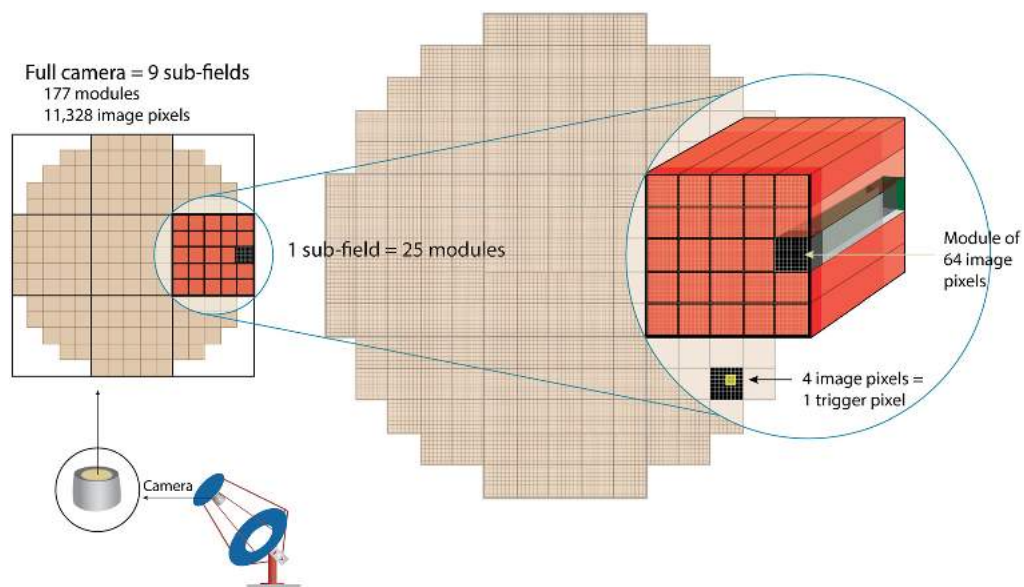


**Fig. 1** Artist's rendition of the prototype SC Telescope. SC optics utilize two mirrors and a curved focal plane to achieve excellent resolution and sensitivity. The primary (9.66 m) and secondary (5.4 m) mirrors along with the location of the camera are labeled. Figure is taken from Ref. 4.

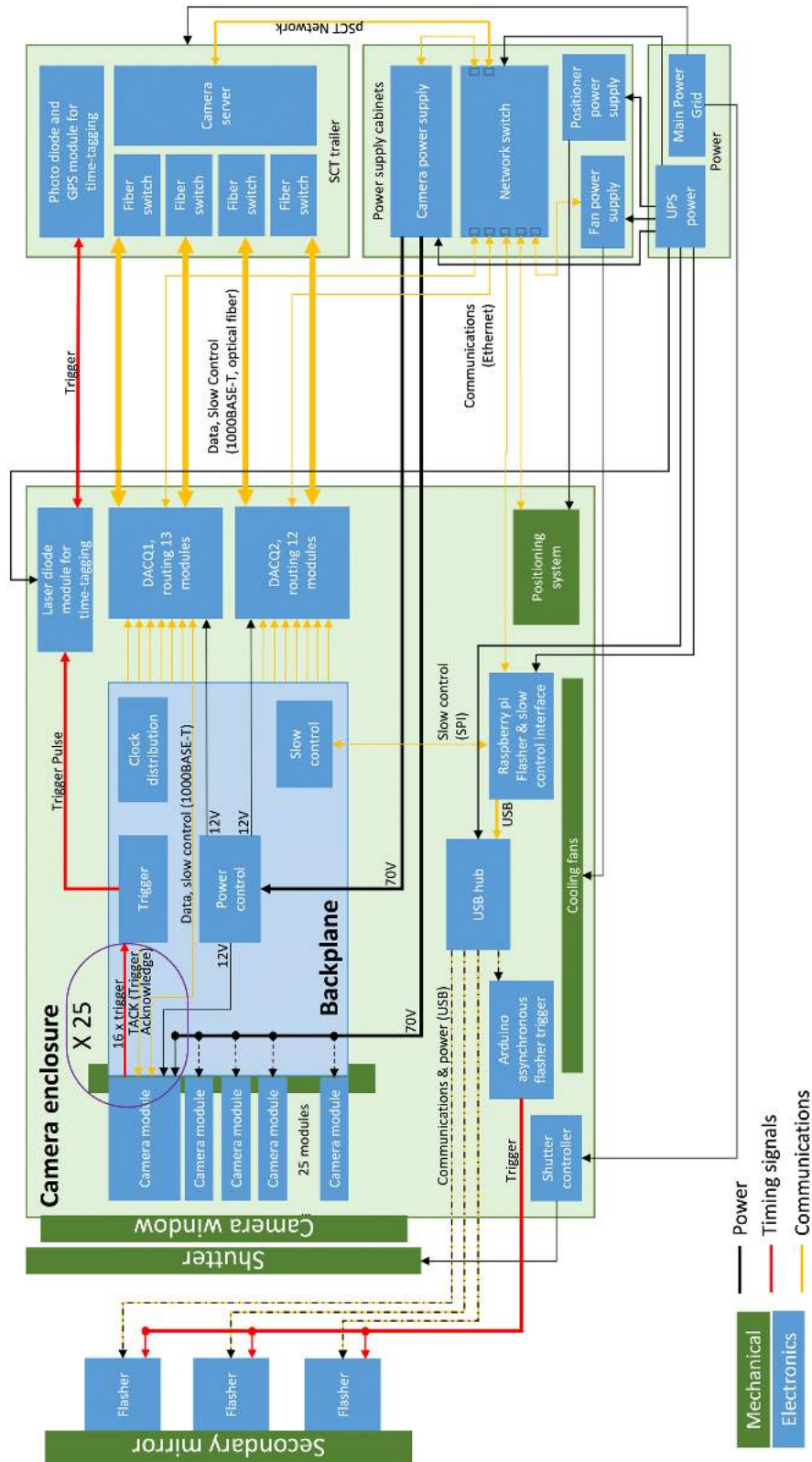
arc<sup>6</sup>) means that silicon photomultipliers (SiPMs) can be used in lieu of traditional photomultiplier tubes (PMTs).<sup>7</sup>

The pSCT camera uses Hamamatsu and FBK SiPMs and custom TARGET (TeV Array Readout with GSA/s sampling and Event Trigger) ASICs. SiPM pixels are much smaller than traditional PMTs, and together these many small pixels are expected to provide a much higher resolution air shower image. This improved image resolution means reduced uncertainty in gamma-ray direction and energy resolution and better background rejection.

The pSCT camera uses a modular design with space for nine backplanes and 177 modules (see Fig. 2). The current pSCT camera has a 2.68-deg FoV and 1600 pixels. A pSCT camera upgrade will increase the FoV to 8.04 deg and the total number of pixels to 11,328. Figure 3 shows a full block diagram of the current pSCT camera. The camera shares common components [front-end electronics (FEE) and backplanes] with the compact high energy camera (CHEC) that is being developed for the dual-mirror CTA SSTs.<sup>8</sup>



**Fig. 2** The pSCT camera has a hierarchical design. The full camera is comprised of nine sectors, each of which can hold up to 25 camera modules (see Sec. 3). The sectors in each corner of the camera are equipped with fewer modules, so the entire camera has 177 modules. Each module has 64 image pixels, so the full camera will have 11,328 pixels. The current pSCT camera has only the center sector populated with modules.



**Fig. 3** Block diagram of all main camera systems. Mechanical elements are shown in green, and electrical elements are in blue. Power connections are black, timing signals are red, and communication signals are gold. The network switch and camera server are connected directly to the pSCT network.

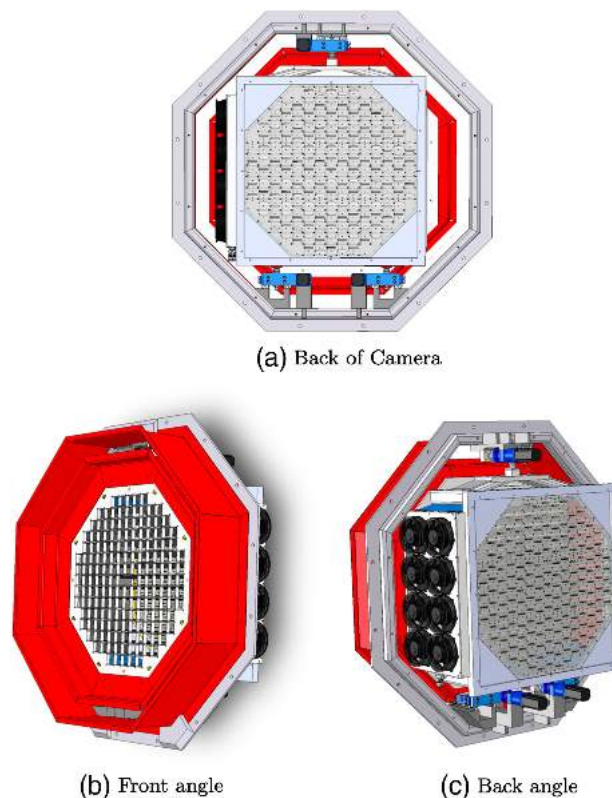
## 2 Mechanical Design

The pSCT camera is located between the primary and secondary mirrors (see Fig. 1). The camera structure is designed to hold up to 177 camera modules. Each module contains FEE as well as a focal-plane module (FPM). Once installed, the focal plane modules together form a curved focal plane that faces the secondary mirror. The camera can be moved via an alignment system (see Sec. 2.2) to achieve the optimum distance and orientation between the focal plane and the secondary mirror (determined by the SC optics). The focal plane and camera electronics are protected from the elements by a retractable shutter (see Sec. 2.3), and the electronics are cooled by a chiller system (see Sec. 2.4).

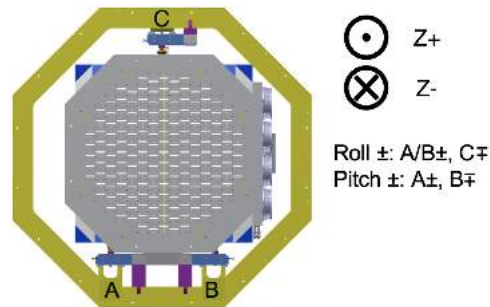
### 2.1 Structure

The pSCT camera is comprised of an outer structure and an inner structure (see Figs. 4 and 5). The inner structure is designed to hold the camera modules (see Sec. 3) and can be moved relative to the outer structure for the purposes of optical alignment (see Sec. 2.2). The inner structure contains a front aluminum lattice and a back bulkhead, which are connected with internal carbon fiber rods to reduce thermal variations in the separation between the lattice and the bulkhead. The lattice was machined precisely to provide a flat front surface and to hold the focal plane component of each camera module (see Sec. 3.1) in the correct position.

The fully populated camera (weight  $\sim 300$  kg) was lifted into the telescope in the summer of 2018 with a crane. Once in position, the outer structure of the camera was bolted to the mounting ring of the telescope. The outer structure is connected rigidly to the telescope and to the outer shroud (which protects the camera from the elements).



**Fig. 4** Mechanical structure of the camera. The outer structure (shown in gray) connects to the shroud and the telescope itself. The inner structure (containing the lattice) can be moved relative to the outer structure via the alignment system described in Sec. 2.2. The shroud and window frame are illustrated in red, the motors in blue, and the fans in black (visible on the left side of view (c)). Modules are inserted into the inner camera structure from the front and are secured through screws in the back bulkhead. Back end electronics (not shown) are also mounted to the back bulkhead and connect with each module through a backplane connector.



**Fig. 5** Motor locations in the pSCT camera as shown from the front. The yellow octagon is the outer structure of the camera and is connected with bolts to the telescope. The inner structure is movable via the three motors labeled A, B, and C. The motion of the camera is described with a right-hand coordinate system with the  $z$  direction labeled along the optical axis of the telescope.  $z$ -motion of the camera requires that all motors move in unison. Pitch (rotation about the  $y$  axis) requires motors A and B move in opposite directions. Roll (rotation about the  $x$  axis) requires motors A and B move together and motor C moves in the opposite direction.

Modules are installed through the front lattice into the gaps between the carbon fiber rods and connected to backend electronics through two holes in the back bulkhead. One hole is for the module connector (which connects the module to its backplane), and the other is for the securing screw (which holds the module in place). This securing screw can be used to pull each camera module into its backplane connector. When tightened, the securing screw keeps the modules tight against the front face of the lattice, ensuring that the module is at the correct location. Modules can be extracted by loosening the securing screw and pushing to eject the module. This system allows for there to be effectively zero clearance between the SiPMs on adjacent modules, while still maintaining the ability to remove individual camera modules for servicing.

## 2.2 Alignment System and Motors

The interior of the pSCT camera (including the focal plane) can be moved relative to the outer structure. This alignment system allows the focal plane to be precisely positioned *in situ* in the correct orientation and at the correct distance to the secondary mirror, as required by SC optics. Initial optical alignment of the pSCT was reported in Ref. 9.

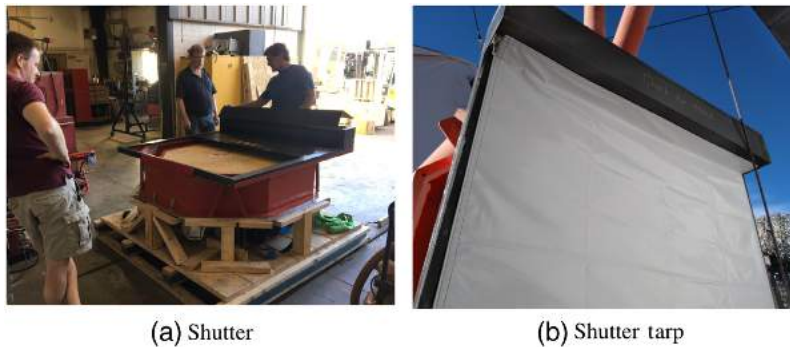
The inner and outer structures of the pSCT camera are connected with three ball pin joints. The inner structure is positioned entirely with these joints and can be moved relative to the outer structure using a camera alignment system. Figure 5 shows both parts of the camera structure as well as the location of the motors used in the alignment system.

The camera can be moved in the  $z$  direction or rotated using the appropriate pattern of three motor assemblies. Each motor assembly contains a step motor that turns a motor driver screw. This screw pushes or pulls a flange that is rigidly connected to the ball pin assembly. The motion of the ball pin assembly is restricted by a rail system to a single direction, in this case in the  $z$  direction (along the optical axis). One step of the motor system corresponds to  $12.7 \mu\text{m}$  of motion along the specified axis. The total range of motion along the  $z$  axis is 5.08 cm.

The camera can also be moved along the  $x$ - and  $y$ -axes by physically rotating the alignment screws. When the horizontal alignment screws are loose, the camera can be moved along a track perpendicular to the rails. Similarly, vertical alignment screws can control the vertical motion of the camera. The motion in these directions is continuous rather than occurring in steps, and the total range of motion is 2.5 cm in both directions.

The motor assemblies are controlled by an Arduino located in the motor electronics box. Each motor can be moved independently or in conjunction with other motors. By moving specific motors in unison, the camera can either be moved in the  $z$  direction (along the optical axis) or rotated. Figure 5 shows which motors are used to achieve each type of movement.

Once the camera is fully aligned, the vertical and horizontal alignment screws can be tightened, keeping the camera in place indefinitely.



**Fig. 6** The focal plane of the camera is shaded and protected from the elements by a commercial AluTech rollup shutter. (a) The shutter installed on the camera prior to its installation. The shutter (black) is mounted onto the camera (red) with four cantilever triangles (red). This photo shows the shutter slats partially rolled up, so the shutter is halfway closed. (b) The shutter tarp (white), which is fixed to the face of the shutter (black) with Velcro to provide additional water protection.

### 2.3 Shutter

A shutter, mounted to the front of the camera enclosure, is used to protect and shade the camera in daylight. After the camera and front shroud were installed into the telescope, the shutter was lifted into place and mated to the front shroud of the camera using four triangle brackets to cantilever the shutter weight.

The shutter is a  $142 \times 142$  cm motorized commercial rollup shutter (AluTech, Inc.) with manual override and remote control. A photograph of the shutter installed onto the camera is shown in Fig. 6.

The shutter is composed of interlocking slats that form a continuous curtain that rolls up onto a mechanical spool when in the open position. To close the shutter, the motor drives the curtain sheet to slide along a continuous, brush-hair-sealed slot in the  $5 \times 2.5$  cm extruded aluminum support frame. The motor uses 120 V, 60 Hz AC power.

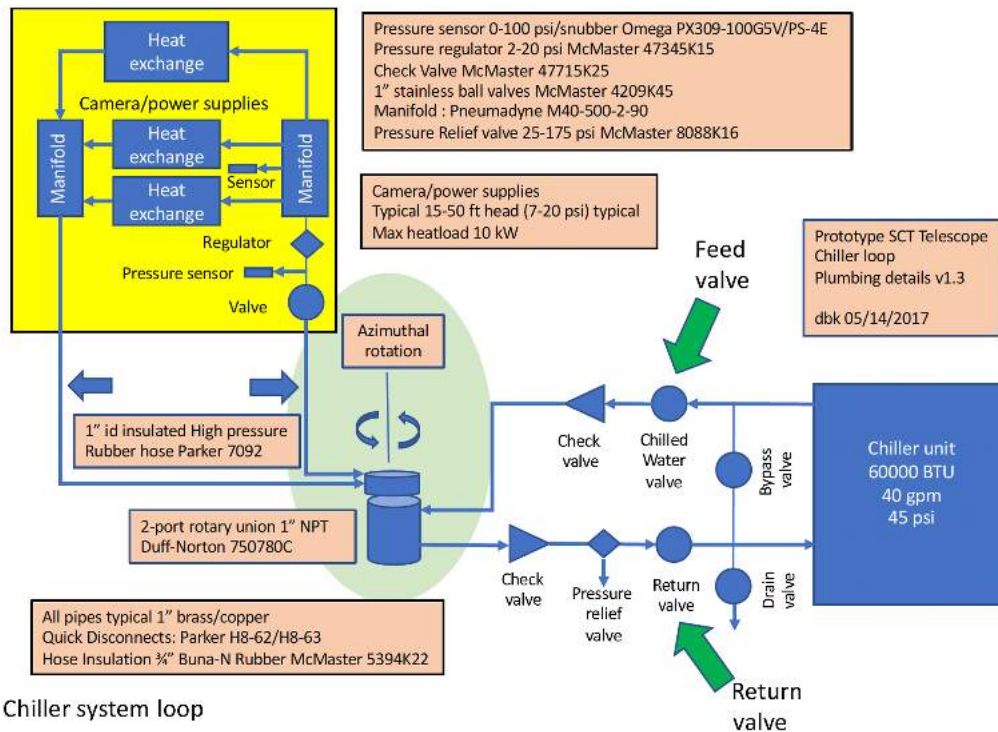
The shutter support frame is bolted to an interface frame that is mounted on the camera using four cantilever triangles. The interface frame provides stiffness to the commercial shutter as well as the transition between the camera octagonal front shroud and the square camera shutter. The interface frame also provides a weatherproof seal to the back of the shutter. The shutter can be controlled in four different ways: the web page, a handheld remote control, a local mechanical switch, or a manual crank.

The camera shutter uses a Simu RTS Radio Micro Receiver 2008191 shutter motor controller, which can be controlled using a handheld (RF) remote as well as with an external waterproof SPDT switch mounted on the side of the camera. The Simu controller is also interfaced to a ControlByWeb X-301 Remote control Dual Relay Controller. Two commercially available proximity sensors (DC 3 Wire 6-36V PNP IR Photoelectric Sensor Switch; E18-B03P1) are interfaced to the sense inputs of the X-301 and are used to sense both open and closed positions of the shutter curtain. The X-301 provides a simple web interface for operation of the Simu shutter motor controller over the web, as well as a method of reading the status of the shutter position (open or closed).

A waterproof tarp cover for the front of the camera shutter was constructed for an extra measure of water protection for the camera. The waterproof camera shutter tarp mounts on Velcro strips directly onto the front shutter frame. The camera shutter tarp can be quickly installed or removed ( $<1$  min once the operator is in front of the camera).

### 2.4 Cooling System

The camera cooling system is comprised of a chiller (detailed in Fig. 7), which chills and circulates coolant, and a set of fans coupled to a heat exchanger, which blow cooled air through the camera. The primary purpose of this cooling system is to remove the excess heat that is generated by the camera and module electronics during data taking. The cooling system cannot hold the



Chiller system loop

**Fig. 7** The pSCT chiller block diagram. The chiller unit cools a mixture of water and propylene glycol, which is then pumped into the camera through a feed valve. The chilled coolant mixture is circulated through the right side of the camera. Fans blow across the chilled pipes, blowing this cold air through the camera electronics. The coolant is then returned to the chiller unit to be chilled again.

camera at a predetermined temperature. Individual modules contain a separate cooling system for their SiPMs. Modules are equipped with a Peltier controller that can be used to further stabilize the temperature of the focal plane.

The camera cooling system was designed to provide sufficient cooling capability for a fully populated focal plane, but during the prototype phase, the heat exchangers and cooling fans within the camera were sized to accommodate only the partially filled focal plane. The remainder of the cooling system was constructed to accommodate the cooling requirements of the full focal plane installation.

The cooling system uses a Dimplex SVO-5001M 60000 BTU/hour (17.6 kW) modified for delivery of 40 U.S. gallons per minute (151 lpm) at 45 psi (310 kPa), filled with coolant that is a 50–50 mixture of propylene glycol and water. The Dimplex chiller is permanently mounted on a separate concrete pad from the SCT telescope. Chilled coolant and return lines run underground between the chiller unit and the telescope through insulated rubber hoses [1" (2.54 cm) inner diameter, Parker 7092 hose wrapped in 1/2" (1.27 cm)-thick Buna-N/PVC closed cell insulation]. A series of manual valves and check valves, located near the chiller unit, allow the chiller unit to be emptied or run in a local test loop to bypass the telescope.

The insulated chiller lines run vertically through the telescope pedestal axis and connect to a two-port rotary union (Duff-Norton 750780C), which is located on the azimuthal axis and is directly driven by the azimuthal telescope head through a connecting rod with a pair of U-joints. The rotary union provides a rotating joint for the chilled coolant and return feed, thereby eliminating twisting of the chiller lines under telescope azimuthal rotation. The chiller lines continue up through a flexible hose/cable manager (IGUS R18840 energy chain) that bridges the variable gap between telescope positioner and the primary mirror. The chiller coolant feed and return lines run along the telescope tower arms. The chilled coolant feed line passes through a manifold mounted midway between the primary mirror and the secondary mirror, bolted to a tower strut. The chilled coolant manifold provides a shutoff valve, check valve, and pressure regulator to

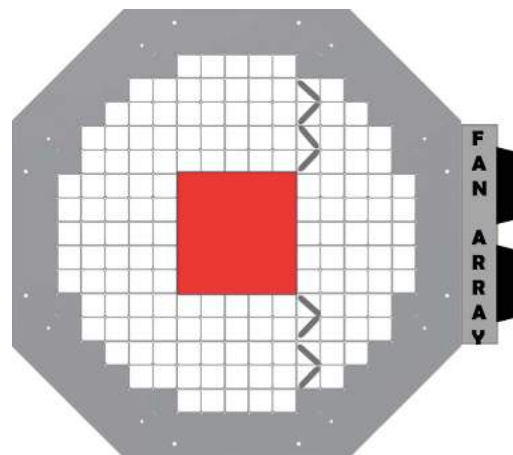
reduce the chilled coolant from the unregulated pressure of 40 to 45 psi (275 to 310 kPa) to a regulated pressure of  $\sim 3$  psi (20 kPa). The pressure regulator is needed to compensate for the varying coolant pressure in the chiller lines caused by different elevation pointings of the telescope. The pressure regulator ensures that the pressure to the heat exchangers in the camera remains constant, regardless of camera elevation.

The chiller manifold also provides a parallel (shunt) coolant flow to supply chilled coolant to a pair of heat exchangers located in the power supply cabinets located behind the SCT camera. Separate pressure regulators are used to adjust the relative chilled coolant flow between the various chilled coolant loops; pressure and temperature sensors are also located in the chilled coolant manifold, allowing for measurement of the coolant pressure before and after the pressure regulator, as well as the coolant temperature and temperature of the power supply cabinets. The pressure and temperature sensors are read out by a ControlByWeb X-320 temperature/analog logging controller, which provides a web interface for remote monitoring. The return coolant manifold is also located on the tower mid-way between the primary and secondary struts, but on a diagonally opposite strut.

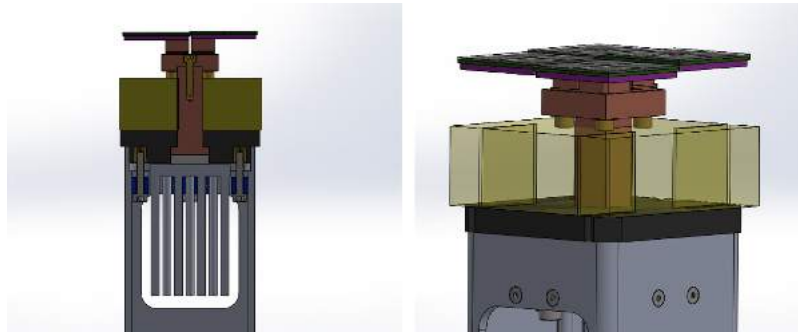
The prototype SCT camera uses eight Pabst EBM 6314 fans coupled to a Super Radiator Coils Model 38 ST WC heat exchanger to cool the camera. The heat exchanger is rated at 7000 BTU/h (2 kW), which is more than sufficient to cool the 25 camera modules, as each module dissipates less than 20 W each when observing.

The camera power supplies, including the FEE power, the SiPM power, the fan power supply, and the power supply for the camera alignment system (see Sec. 2.2), are physically located in two independent, weather-tight power supply cabinets located  $\sim 1$  m behind the back of the SCT camera. The two sealed power supply cabinets each contain one 19-in. rack. The racks are used to hold the rack-mounted power supplies, as well as other rack mounted equipment, such as a managed ethernet switch for communications and control of various camera and telescope sub-systems. Each power supply cabinet is cooled by the chilled coolant feed using a Lytron 6220G1SB heat exchanger and fanpack. Each Lytron 6220G1SB heat exchanger is capable of handling 6832 BTU/h (2 kW) with 2 U.S. gallons per minute (7.5 lpm) coolant flow at 1 psi (6.9 kPa).

Because the camera is not fully populated at this time, a series of baffles is used to force air through just the sector currently containing modules (see Fig. 8). The first baffle is a single, large sheet and fits onto the front of the camera. It blocks the unused module holes in the front of the camera while leaving the central sector open, so modules can be inserted. This keeps cooled air from escaping out of the front of the camera. The other baffles are small rectangular pieces that are inserted at a 45-deg angle into unused module slots. They are secured in a way similar to the



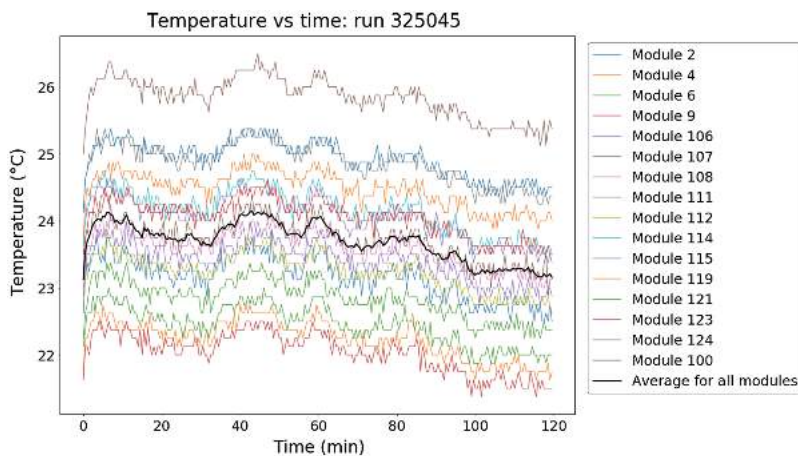
**Fig. 8** Air baffle orientation diagram. Baffles are long, rectangular aluminum pieces that are inserted into unused module slots at a 45-deg angle. The baffles are arranged in such a way that air from the fans is directed through the modules in the camera. These baffles will be removed for the camera upgrade to make room for the modules of the fully populated focal plane. The camera upgrade will also include additional fans to cool the increased number of modules.



**Fig. 9** Two perspectives of an FPM. Each FPM is divided into four quadrants. Each quadrant is composed of 16 image pixels and has a z position achieved by placing shims between the copper post and the copper block on the bottom of the PCB for each quadrant. Yellow insulating foam surrounds the copper post, which attaches the light sensors to a Peltier element. On the opposite side of the Peltier element is a heat sink.

camera modules, with a screw through the back plate of the camera. The baffles are designed to direct air from the fans through the inserted modules. Figure 8 shows the orientation of the baffles currently being used in the camera.

The focal plane photon sensors and the module electronics are thermally isolated from one another. This is achieved by inserting insulating foam between each FPM and its FEE. A thermoelectric (Peltier) element transfers heat from the FPM connected to its cold side to a heat sink connected to its hot side. This is shown in Fig. 9. The heat sink is cooled by the air flow of the chilled coolant cooling system, alongside the module electronics. A Peltier controller will be used to stabilize the temperature of the focal plane. Each module's electronics are stable to within 1°C when using the chiller system (see Fig. 10). Using the Peltier controller, the focal plane temperature stability was measured in the lab to be within 0.1°C, but the Peltier controller has not yet been tested onsite. As a result, the *in situ* focal plane temperature stability is unknown.



**Fig. 10** Temperature versus time for a 2-h run taken onsite during the summer of 2018 (prior to installation of the Peltier coolers and control). The ambient temperature over the course of the run was 22.8°C to 23.9°C. The module temperature is recorded on the module's FEE. The temperature of each individual FEE is constant to within 1-deg over the full 2-h period. Typical data runs last one hour, meaning that individual modules do not experience significant changes in temperature within a single run. The spread of temperatures across modules is due to their physical position in the camera and is consistent over time. In addition, each module has an independent lookup table for temperature-dependent variables to account for the 4-deg spread between modules.

### 3 Modules

The camera is capable of housing 177 modules (see Fig. 2). Each module consists of the FEE, which are housed inside an aluminum module cage, and an FPM, which mates to the FEE. The modules are inserted into the front aluminum lattice until the focal plane module fiducial surface is flush with the lattice. To fit the modules into the camera's back aluminum plate, modules in the same row have alternating orientations (they are rotated 180 deg from their neighbor), whereas those in the same column have the same orientation.

#### 3.1 FPM Design

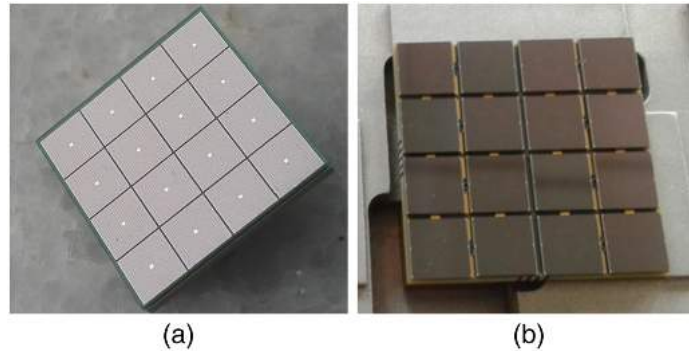
The pSCT focal plane is made up of two types of photosensors. The locations of these photosensors in the focal plane are shown in Fig. 11. Sixteen modules are equipped with Hamamatsu photon detectors S12642-0404PA-50(X). One Hamamatsu tile is shown in Fig. 12. One tile consists of 16 SiPMs in a square grid configuration, each with dimensions  $3 \times 3 \text{ mm}^2$ . One FPM is equipped with 16 Hamamatsu tiles, and each tile corresponds to one trigger pixel.

Nine modules are equipped with third-generation near-ultraviolet high-density SiPMs (NUV-HD3) that were produced by Fondazione Bruno Kessler (FBK) in collaboration with Istituto Nazionale di Fisica Nucleare (INFN). One FBK unit consists of 16 SiPMs in a square grid configuration, each with dimensions  $6 \times 6 \text{ mm}^2$ .<sup>11</sup> One camera module is equipped with four FBK units with each unit containing four trigger pixels.

For either type of photosensor, a single FPM contains 64 image pixels. One square group of four image pixels makes up one trigger pixel. Thus, one FPM contains 16 trigger pixels. One square group of four trigger pixels makes up one quadrant of the FPM. Figure 13 shows how quadrants, trigger pixels, and image pixels are laid out in a single FPM. Quadrants are mounted onto a printed circuit board (PCB) that has a tapped copper block on the other side. These quadrants are bolted onto the top of a copper post. This is shown in Fig. 9. The copper post passes through a layer of insulating foam and is secured at its base by a plastic base plate.

FPM 4-24 FEE 2	FPM 4-23 FEE 3	FPM 4-22 FEE 1	FPM 4-21 FEE 5	FPM 4-20 FEE 4
FPM 4-19 FEE 9	FPM 4-18 FEE 106	FPM 4-17 FEE 126	FPM 4-16 FEE 125	FPM 4-15 FEE 103
FPM 4-14 FEE 8	FPM 4-13 FEE 121	FPM 4-12 FEE 110	FPM 4-11 FEE 108	FPM 4-10 FEE 119
FPM 4-9 FEE 7	FPM 4-8 FEE 112	FPM 4-7 FEE 124	FPM 4-6 FEE 123	FPM 4-5 FEE 115
FPM 4-4 FEE 6	FPM 4-3 FEE 107	FPM 4-2 FEE 114	FPM 4-1 FEE 111	FPM 4-0 FEE 100

**Fig. 11** The pSCT focal plane is currently equipped with 25 modules in a square grid configuration. Sixteen of the modules are equipped with Hamamatsu photon detectors S12642-0404PA-50(X) (see Fig. 12). The remaining nine modules are equipped with the NUV-HD3 sensors produced by FBK. The locations of these modules are shown as viewed facing toward the sky, with blue indicating Hamamatsu sensors and red indicating FBK sensors. For each slot, the FPM number is listed along with the FEE number for the module in that slot.



**Fig. 12** (a) A photo of a Hamamatsu MPPC S12642-0404PA-50(X) sensor used in the pSCT camera. Shown is a single tile as delivered by the manufacturer. Each tile has 16  $3 \times 3$  mm SiPMs that are grouped into four  $6 \times 6$  mm image pixels. Each tile corresponds to one trigger pixel, and a single FPM uses 16 of these tiles.<sup>10</sup> A single Hamamatsu tile measures  $13 \times 13$  mm. (b) A photo of an FBK sensor used in the pSCT camera. Shown is a single tile. Each tile has 16  $6 \times 6$  mm SiPMs, each of which corresponds to a single image pixel. Each tile corresponds to four trigger pixels, and a single FPM uses four of these tiles. A single FPM tile measures  $26 \times 26$  mm.

Module

42	43	46	47	58	59	62	63
10	41	11	45	14	57	15	61
34	35	2	38	39	50	51	3
8	33	9	36	37	12	49	13
32	33	36	37	48	49	52	53
10	11	14	15	26	27	30	31
2	9	12	13	24	25	28	29
8	9	12	13	24	25	28	29
2	3	6	7	18	19	22	23
0	1	4	5	16	17	20	21
Image pixel		Trigger pixel		Quadrant			

**Fig. 13** One module contains 64 image pixels (black) numbered 0 to 63. A square group of four image pixels makes up one trigger pixel (red). Thus, one module contains 16 trigger pixels. A square group of four trigger pixels makes up one quadrant (blue). Thus, one quadrant contains 16 image pixels, and there are four quadrants in a module. Image pixels are associated with channels, trigger pixels with trigger groups, and quadrants with ASICs in the software.

When installed, the base plate mates securely into a slot in the front camera lattice and is pulled flush to the front surface of the lattice by springs in the module housing, positioning the photosensors precisely in the desired position in the focal-plane surface.

Trigger pixels are placed at unique  $z$  positions in relation to the quadrant they are in to produce a smoothly varying convex focal plane required by SC optics.<sup>5</sup> The final  $z$  positions of the quadrants are determined by the height of the copper post and the thickness of shims between the post and each of the four PCBs. The bottom of the copper post is connected to the cool side of a Peltier thermoelectric element (TE) and acts as a thermal conductor between the sensors and the TE. On the warm side of the TE, a heat sink is connected. A thermistor is mounted to the back of each quadrant and is capable of providing temperature feedback.

The sides of the quadrants are aligned to the edge of the plastic base plate. This base plate is then pushed onto the FEE aluminum module cage and secured with screws. The pitch between

modules is 54 mm. The optimal sag of the focal plane,  $z_f$ , is derived through simulations and is given as

$$\frac{1}{F}z_f(v) = k_1v + k_2v^2, \quad (1)$$

where  $v$  [given in Eq. (2)] is related to the cylindrical coordinate  $r_f$  of the surface of the focal plane:

$$v = \left(\frac{r_f}{F}\right)^2. \quad (2)$$

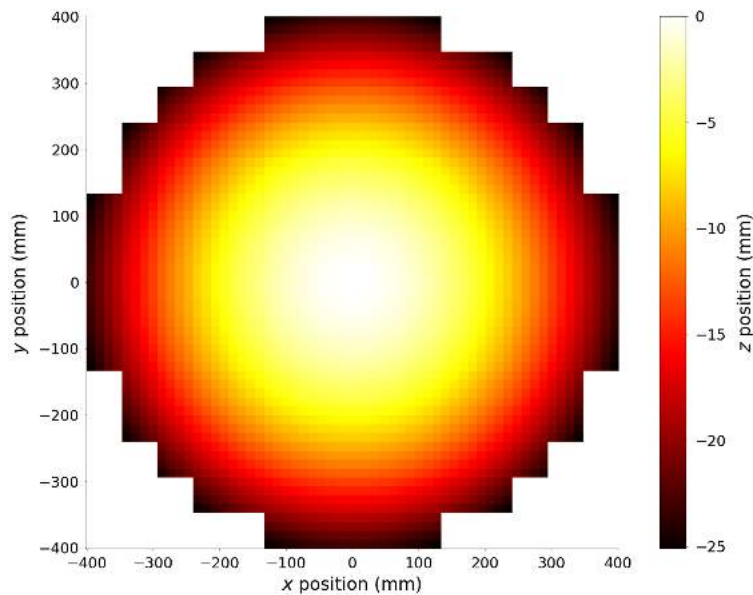
The constants  $k_1$  and  $k_2$  in Eqs. (1) and (2) have values  $k_1 = 0.8327$  and  $k_2 = 4.9950$ .

This results in a focal plane that is nearly parabolic. If the curved focal plane is assembled from photon detectors of size  $\Delta$  in the tiled arrangement with the center of the detector placed exactly at the optimal coordinates  $(r_f, z_f)$ , then the edges of the detector will be misplaced from their optimal location by  $\Delta Z_f$  [given in Eq. (3)]:

$$\Delta Z_f = \pm k_1 \left(\frac{r_f}{F}\right) \Delta = \pm 3.023 \text{ mm} \left(\frac{\Theta}{4 \text{ deg}}\right) \left(\frac{\Delta}{52 \text{ mm}}\right). \quad (3)$$

SC optics require positional uncertainties along the optical axis of  $<1.2$  mm and uncertainties perpendicular to the optical axis of  $<0.27$  mm.<sup>12</sup> The precision of the placement of the center of each image pixel is better than  $100 \mu\text{m}$  in the  $z$  direction (parallel to the optical axis). In the  $X$ - $Y$  plane (perpendicular to the optical axis), the precision is better than  $200 \mu\text{m}$ . The positions of each pixel are shown in Fig. 14. The on-axis PSF of the current pSCT camera was measured to be 2.8 arcmin. The off-axis PSF has not yet been measured.<sup>9</sup>

Each quadrant is connected to the FEE with a microcoaxial ribbon cable with  $50 \Omega$  impedance. These cables provide power to the SiPMs and send the SiPM signals to ASICs located on the FEE. Each image pixel is connected to an ASIC channel of the same number. In addition, the ribbon cables provide connectivity between each quadrant's thermistor and a microcontroller,



**Fig. 14** Camera focal plane. Colormap of the position of each trigger pixel in the camera. This plot is from the front perspective of the camera with the positive  $z$  axis toward the secondary mirror. The  $z$  position of each quadrant is determined by shims placed between the SiPMs and the copper post. Trigger pixels within a quadrant are fixed at unique  $z$  positions in relation to the quadrant. The final product is an approximation of a smoothly varying convex surface.

located on the FEE, which is responsible for temperature stabilization (see Sec. 3.2). Temperature stabilization is required because the SiPM gain is temperature dependent. Currently, temperature stabilization is achieved only through the chiller system. Stabilization including the thermistor is currently underway and is expected to be achieved during the camera upgrade.

The FEE also provides power to the TE. Further temperature stabilization of the focal plane is achieved through insulation of the sides of the camera walls and airflow cooling the module heatsinks (see Sec. 2.4).

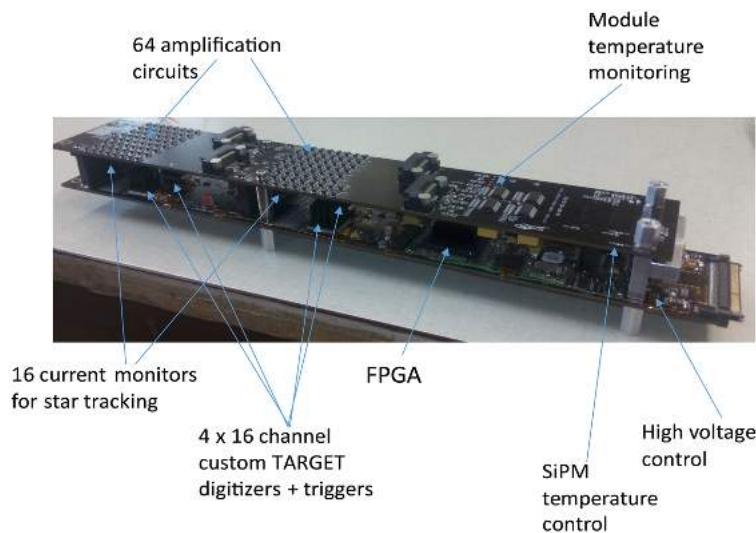
The breakdown voltage of the Hamamatsu sensors has a median of 64 V.<sup>13</sup> The breakdown voltage of the FBK sensors is  $\sim 27$  V. Every SiPM will be operated at  $\sim 3$  V above breakdown (this corresponds to a gain of  $\sim 1.6 \times 10^6$  for Hamamatsu sensors and  $\sim 2 \times 10^6$  for FBK sensors at a temperature of 20°C). To achieve this bias voltage for each SiPM, a uniform 70 V (which is applied to all pixels in a sector) is combined with a trim voltage (adjustable for individual pixels). The 70 V and trim voltage both come from the module FEE (see Sec. 3.2).

### 3.2 FEE Design

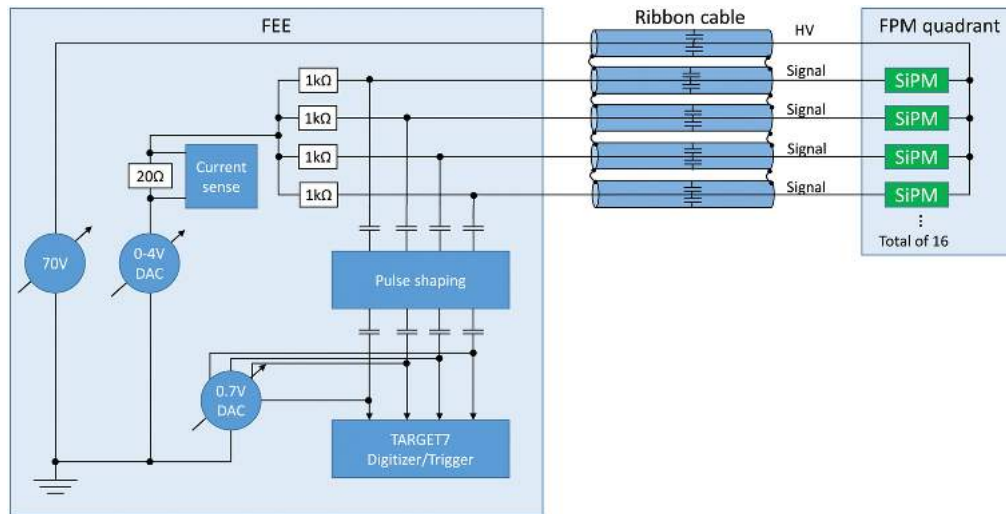
The FEE part of the camera module generally handles the readout and control of the FPM. The main functionalities it combines are

- amplification and digitization of FPM signals,
- control of SiPM bias voltage,
- temperature monitoring and control of FPM,
- low-level trigger generation, and
- waveform data packaging and transfer to storage.

The electronics of the FEEs are distributed over two circuit boards: the primary and the auxiliary boards. Their dimensions are  $\sim 5$  cm  $\times$  28 cm, and they are stacked, the auxiliary board on top of the primary board, to fit a 5 cm  $\times$  5 cm  $\times$  45 cm aluminum housing. A photograph of the stacked boards is shown in Fig. 15. The boards are interconnected through Samtec QTH series high-speed board-to-board connectors. The primary board connects directly to the backplane, when mounted in the camera. The FPM connects to the auxiliary board through four ribbon cables, one per quadrant. These cables carry ground, a 70-V supply to the cathode of the SiPMs, the SiPM anode output signals, and the connection to thermistors on the FPM quadrant.



**Fig. 15** The pSCT FEE. The auxiliary board is stacked on top of the primary board, and they are connected with high-speed connectors. The primary board connector on the right side connects the module to a backplane when it is mounted in the camera.



**Fig. 16** A block diagram of the signal chain between SiPM sensors of one FPM quadrant and a single TARGET7 readout chip (of four in one module). The 0–4 V DAC adjusts the bias voltage across groups of four SiPMs for differences in their breakdown voltage. The 0.7 V DAC provides a pedestal offset to the signals entering the digitizer chip.

The auxiliary board contains most of the analog processing for the incoming 64 FPM signals. This includes a pulse-shaping circuit for each channel that shortens the SiPM pulses through a high pass filter and 16 current sensors that read the combined current through groups of four SiPM pixels.

The current pSCT has only one sector populated with modules with a bias voltage of 70 V. Modules that include FBK sensors have an extra voltage regulator located on the FEE, which converts this bias voltage from 70 to 35 V. The trim voltage across the SiPMs can be regulated for groups of four image pixels using digital-to-analog converters (DACs) that can set the SiPM anode voltage between 0 and 4 V in steps of 1 mV. The cathode voltage is fixed to the bias voltage; this feature is used to compensate for production variances of the SiPMs, which affect the breakdown voltages of the sensors. The groups were chosen such that SiPMs with similar breakdown voltages are part of the same bias regulation group. The DAC can sink a maximum current of 50 mA from the four SiPM pixels. The maximum SiPM current is limited to 128 mA for each module. If this limit is reached, the module will be shut off, and all trim voltages will be set to zero. A block diagram that illustrates the signal processing, current readout, and biasing of a group of four SiPMs is shown in Fig. 16.

The auxiliary board also manages the FPM temperature readout and control through a microcontroller to achieve stable SiPM temperatures. For this purpose, a full PID regulation scheme is implemented in the microcontroller. The microcontroller will monitor the temperature of the four quadrants by measuring the resistance of the thermistors inside the FPM and will regulate the current through the Peltier element to supply the necessary cooling.

The primary board contains most of the digital control of the FEE as well as readout and triggering circuits for the SiPM signals. The communication with and control of all devices within the FEE, as well as connection to the backplane and data acquisition (DAQ) boards, is established using a field programmable gate array (FPGA). It uses I2C, SPI, and custom protocols to configure and read FEE components. Digitized data are managed within the FPGA and transferred to the DAQ boards via gigabit Ethernet links, if requested by an incoming trigger signal.

### 3.2.1 Module sampling and trigger system

The primary board contains four TARGET7 chips (the seventh generation “TeV Array Readout with GSa/s sampling and Event Trigger”). This chip was designed to sample, digitize, and trigger on 16 incoming channels.<sup>14–16</sup> It has a dynamic range of  $\sim 2$  V and samples the input waveform’s

charges every nanosecond, so at a speed of 1 GSa/s (see [Appendix A](#) for a full description of this sampling system). The charge samples are held in an analog storage buffer within the chip, which can hold up to 16  $\mu$ s of samples before having to overwrite. Inside the buffer, samples are grouped into 512 blocks of 32. These blocks can be randomly accessed and transferred to the Wilkinson digitizer of the chip using an individual block address.

At the same time, a trigger system inside the chip monitors groups of four channels for a threshold crossing of their analog sum. If the threshold is crossed, a module trigger (roughly 10 ns long trigger pulse) is sent directly to the backplane. Module triggers are evaluated by the backplane to produce backplane triggers (see [Sec. 4.1](#) for a description of the backplane trigger system). In case of a trigger request from the backplane, the FEE gets a time stamp of the data to be read out. The time stamp can be translated into the appropriate address within the analog buffer, and data can be digitized and sent to the FPGA for transfer to storage. Currently, the typical length of a readout is four blocks of 32 samples. This highly integrated circuit allows us to implement a trigger system, sampling and readout of 64 high-speed channels within the given tight space at a reasonable power consumption of  $\sim$ 13 W per module.

The input signals to the TARGET7 chip are AC coupled to the SIPM output, and an offset of 0.7 V is applied to them by DAC to optimize the usage of the dynamic range of the digitizer. For calibration, this pedestal offset can be varied through the entire voltage range of the digitizer.

## 4 Backend Electronics

The focal plane of the pSCT is divided into nine sectors, each of which will have its own backplane PCB and two DACQ boards. Each sector can hold a maximum of 25 modules. Corner sectors only hold 13 modules. All nine backplanes will connect with a single telescope-wide trigger system (see [Sec. 7.2](#)) and a single housekeeping/command computer (currently, a Raspberry Pi with Ethernet interface).

Currently, only one sector of the pSCT is populated with modules, requiring only one backplane and two DACQ boards for full operation. An upgrade of the camera that will fully populate it is currently in progress.

### 4.1 Backplane

The current pSCT camera contains one backplane mounted to the back bulkhead. When modules are inserted into the camera (see [Sec. 2.1](#)), they are connected to the backplane via a backplane connector. The modules are held in place via a screw that holds the backplane, module, and back bulkhead together.

The high-speed serial data from the camera modules are routed through impedance matched low voltage differential signal (LVDS) lines to the backplane via a single connector. The same connector includes the trigger signals from each module and the trigger acknowledge (TACK) messages needed to localize the triggering data in the analog pipeline. This connector also carries the 12 V DC power for the module, which is distributed by the backplane.

The backplane also provides housekeeping and power supply management functionality. Each backplane has a single 70 V input DC converter board that produces the 12 V DC input to the backplane. A second mezzanine power supply module is used to derive all of the other voltage levels needed by the backplane. Putting these power supply components on mezzanine cards allows the relatively low-lifetime components (e.g., electrolytic capacitors) to be replaced without pulling the main backplane motherboard. A housekeeping FPGA (HKFPGA) is used to control critical power-up sequencing of the various voltage levels required by the FPGAs and FEEs and to reduce the current inrush. Current shunts and ADCs are used to monitor voltages and currents. Power field effect transistors are used to control power to individual FEE modules and the DACQ boards. The HKFPGA also communicates with the trigger FPGA (TFPGA), allowing slow-control (SC) commands for configuring and monitoring the trigger logic. A single SPI link to each BP HKFPGA allows for communication through a small housekeeping/command computer (currently, a Raspberry Pi with Ethernet interface, see [Sec. 4.3](#)).

An upgrade to the pSCT is currently underway and will increase the number of backplanes from one to nine, one for each sector of the focal plane. Each backplane will connect to two DACQ boards (see Sec. 4.2). Backplanes in the same row will have alternating orientations (they are flipped 180 deg with respect to their neighbor), whereas backplanes in the same column will have the same orientation.

#### 4.1.1 Backplane triggers

One of the principal responsibilities of the backplane is to provide the camera trigger logic and time synchronization functions (working with the telescope's time-tagging system; see Sec. 4.4). Each camera module covers 64 SiPM image pixels and provides 16 trigger signals to the backplane, each coming from one trigger pixel (called module triggers; see Sec. 3.2.1). The programmable pulse width set by the FEE electronics directly determines the coincidence resolving time of the pattern trigger. The pulse width of the module trigger is currently set to  $\sim 10$  ns, and no additional discriminator or one-shot components intervene to modify the pulse width. A minimal overlap of  $\sim 1.5$  ns of these FEE trigger pulses in the TFPGA is sufficient to generate a coincidence.

The backplane forms backplane triggers using a single TFPGA to form coincidences from the 400 module trigger inputs for the 25 modules in each backplane. A backplane trigger is only produced when three adjacent trigger pixels produce a module trigger at the same time. A pixel is considered adjacent if it is orthogonally adjacent or diagonally adjacent (i.e., a pixel can have up to eight adjacent pixels).

The TFPGA runs on an external 125 MHz clock, from which one derives an internal 250 MHz clock for the synchronous logic. However, the TFPGA logic actually allows one to further interpolate this 4 ns time resolution, giving coincidence resolving times (minimum trigger pulse overlap) down to 1.5 ns and time stamping of triggers to 1 ns. This time precision is achieved by dividing each trigger input into four pipelines (A, B, C, and D) with phase offsets of 0, 1, 2, and 3 ns, respectively, with respect to the 250-MHz clock. The 400 inputs are latched on each of the four phase offsets and then delivered to the coincidence logic. The coincidence logic (e.g., to derive three adjacent hits) is exactly duplicated for each pipeline and implemented as synchronous logic running at the four different clock phases.

If any of the coincidence logic pipelines give a high value, a backplane trigger is generated. We note that the distributed intelligent array trigger (DIAT) communication protocol (not used in the prototype) includes synchronization words to ensure that the phase of the 8-ns clock is common between the FEE modules and TFPGA. In the pSCT camera, the TFPGA provides a similar mechanism to send sync messages to the FEEs. This 1-ns time is latched by the first pipeline to trigger, time-tagging the coincidence to a similar precision. The hit pattern is also latched on a trigger, and the time and hit pattern are sent to the DIAT interface board on the backplane, which serializes the data to forward through a high-speed serial link to the DIAT.

## 4.2 DACQ Boards

Data acquisition is accomplished with two custom DACQ boards. Each board hosts a 16-channel 1-Gbit Ethernet switch implemented in an FPGA. The boards are based on the commercial White Rabbit design by Seven Solutions but were modified to provide electrical and mechanical interfaces needed for compatibility with the backplane motherboard. For the pSCT application, a number of features of these boards are not used, and they function as simple network switches to route the data from the FEE modules to a single 1-GigE network connection. These boards were originally designed for the CHEC/GCT camera, which used an identical backplane design but was populated with 32 camera modules (see Ref. 2 for a more detailed description). Commands to and data from the FEEs are sent in UDP packets managed by the switch. The LVDS data lines between the FEEs and DACQ boards are aggregated into two connectors on the backplane and delivered via a ribbon cable to the DACQ boards. The power to the DACQ boards can be controlled via the HKFPGA to allow for remote rebooting. The 125-MHz backplane clock is also distributed to the DACQ boards.

### 4.3 Raspberry Pi

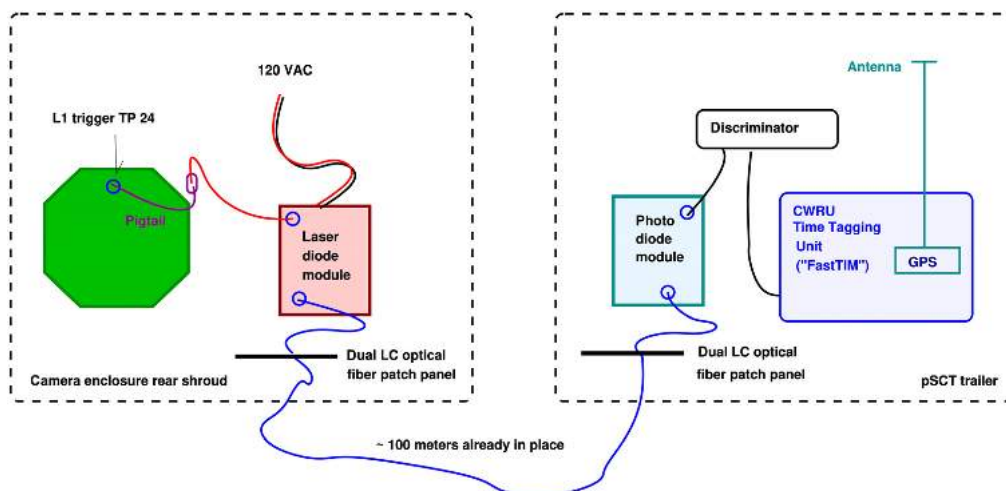
The purpose of the Raspberry Pi is to establish communications to the backplane HKFPGA, the TFPGA, and the flasher modules (see Sec. 5.1), none of which can be accessed via the available Ethernet connections to the camera (see Fig. 3). A backplane control program establishes an SPI link to the HKFPGA of the backplane and, among other things, allows the user to

- switch and monitor supply voltages for camera modules and measure their individual power consumption,
- send synchronization messages to the camera modules,
- enable and monitor trigger channels from the camera modules,
- control the DACQ board power, and
- monitor backplane power voltages, currents, and temperatures.

The Raspberry Pi also contains software to configure the three flashers as well as their trigger system via a serial interface over USB. The trigger system allows the user to choose a rate and time frame for triggers to be sent to the flashers.

### 4.4 Camera Trigger Time-Tagging

In the final SCT, the DIAT board will provide essential GPS time-tagging and a synchronized 62.5-MHz clock to each backplane and FEE module. The DIAT will be installed during the camera upgrade (see Sec. 7). In lieu of a DIAT board, we installed a standalone backplane event time-tagging system that will operate on the pSCT independent of the backplane. Figure 17 shows a conceptual schematic of how the time-tagging system operates. The system is divided into two modules: the laser-diode module, which is located in the camera rear shroud, and a photodetector/GPS module, which is located in the telescope trailer. The two modules are connected by about one hundred meters of fiber optic communications cable. We use a laser-diode (850 nm, q-switch) to generate fast pulses at up to 5 kHz from camera backplane triggers. The output is fed to a discriminator, and then the logic pulse is generated. We latch a GPS time-stamp to each pulse using custom-developed software/firmware 2-in-1 programmable logic device implemented on the Xilinx 7200-based Zedboard. The system provides stable time stamps for every camera event trigger to a GPS accuracy of better than 5 ns as measured on the laboratory test bench.



**Fig. 17** Conceptual schematic of the standalone camera event trigger time-tagging system for the pSCT. The level-1 backplane trigger output is used to trigger a pulsed laser diode located at the back of the telescope. The laser pulse propagates via fiber optic cable to a photodiode detector, which generates a GPS time-stamp accurate to better than 5 ns.

## 5 Additional Systems

### 5.1 Flashers

A photograph of the LED flashers as they are currently installed on the optical table of the pSCT is shown in Fig. 18. This LED flasher system is based on the calibration system of the CHEC-M camera<sup>17</sup> and on the design for the VERITAS LED flasher system.<sup>18</sup> The pSCT primarily uses these flashers to provide consistent triggers at a known rate to the camera. A variety of waveform amplitudes can be achieved by adjusting which LEDs in the flasher are used during data taking.

The LED flasher consists of two PCB boards stacked together, linked with a 14-way Samtec SFMC connector. The two boards are the programmable system-on-chip “PSoC board” and the “LED board.”

The LED board is the upper board and hosts ten 3-mm LEDs providing light in the UV range ( $400 \pm 2.5$  nm). Each LED has a viewing angle of 15 deg. The light from the LEDs in each flasher unit passes through a 20-deg circle pattern diffuser.

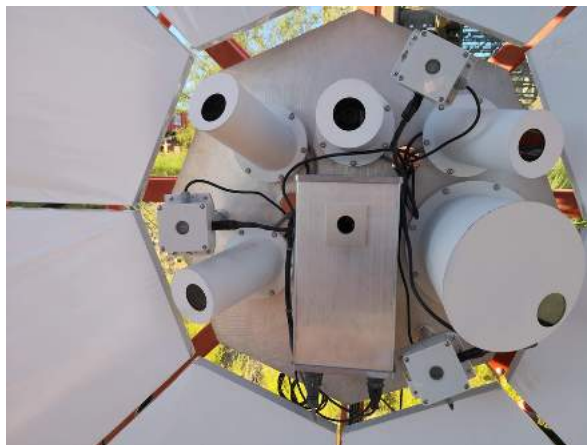
Three entire assemblies of the flasher are mounted on the optical table at the center of the secondary reflector, as shown in Fig. 18. Each flasher is powered through a USB serial connector connection to the Raspberry Pi (via a USB hub) located in the camera enclosure. Using the Raspberry Pi, these USB connections can be used to turn individual LEDs on and off to produce a variety of LED patterns.

The flasher receives a TTL trigger pulse through an LEMO connector. After the rising edge of the TTL trigger is received at the PSoC board, an active-high LED pulse is generated by a NOT gate, two AND gates, a potentiometer, and a 1 pF capacitor, with the pulse width determined by the setting of a potentiometer.

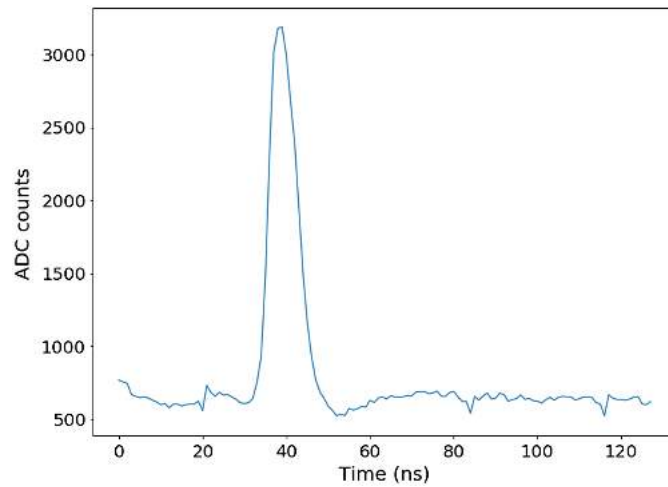
Currently, triggers to the flashers are provided by an Arduino seated in the back of the camera. The rate and duration of the trigger signal are communicated to the Arduino from the Raspberry Pi.

The current through an individual LED within a flasher is controlled by a resistance in series with the LED. Each flasher on the pSCT has five “bright” LEDs (L1, L3, L4, L6, and L8), each of which is connected in series with a corresponding resistor of 80  $\Omega$ . The other five LEDs are dimmer than these “bright” LEDs, but each has a unique resistor value. The LEDs L2, L5, L7, L9, and L10 are connected in series with resistors of 100  $\Omega$ , 110  $\Omega$ , 120  $\Omega$ , 140  $\Omega$ , and 130  $\Omega$ , respectively. These higher resistor values lead to a lower current.

The output light level of an LED depends on the total charge from an active-high LED pulse, which is controlled by both the current (set by the resistance in series) and the pulse width (set by the potentiometer resistance). After an LED flasher unit is assembled, only the pulse width is



**Fig. 18** Optical table located at the center of the secondary reflector. The flashers are the square objects mounted along the exterior. From top to bottom, the flashers have potentiometer settings 2.5 k $\Omega$ , 1.8 k $\Omega$ , and 4 k $\Omega$ . The flasher set to 4 k $\Omega$  is also equipped with a 10% neutral density filter.

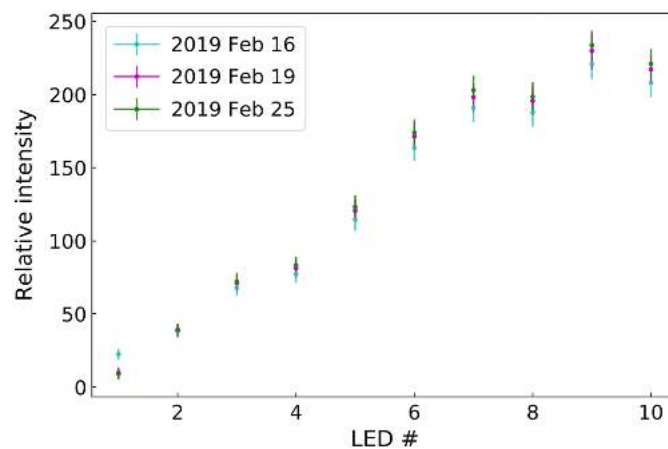


**Fig. 19** Flasher pulse taken onsite using a flasher on the optical table with the potentiometer set at 6 k $\Omega$ . No pedestal or baseline subtraction was applied.

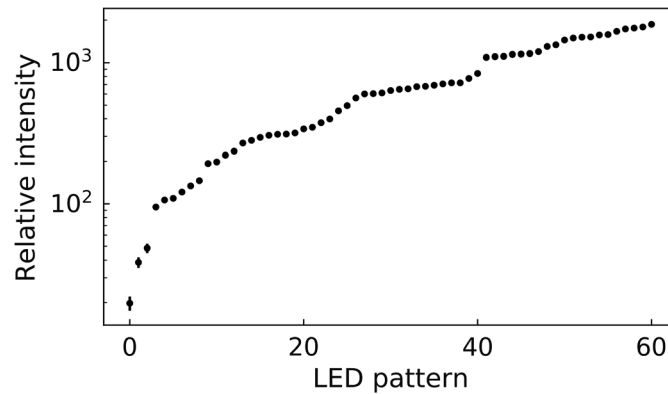
adjustable through the potentiometer. A higher potentiometer resistance leads to a wider pulse and therefore a higher output light level. In the current design, the potentiometer can be set only when the flasher is disassembled and uninstalled from the optical table shown in Fig. 18. The current potentiometer values for each flasher on the pSCT are noted in the caption. An example raw waveform, from a channel of pSCT from a flasher pulse generated with a 6-k $\Omega$  potentiometer setting, is shown in Fig. 19.

The relative output light levels for each LED are fixed as the resistance in series is constant. We performed three measurements of the light output of each individual LED on different dates in a similar, controlled environment in the lab, as shown in Fig. 20. The results show good agreement between different measurements for the brighter LEDs. The fluctuation in the LED with the lowest intensity may be attributed to the PMT used in the test.

When a combination of different LEDs is turned on, the total output light level is not equal to the simple sum of those from individual LEDs when they are turned on by themselves. Small



**Fig. 20** Relative intensity levels for individual flasher LEDs measured in the laboratory. The absolute scale of the relative intensity corresponds to the approximate number of photoelectrons per pixel expected in the camera running on the telescope, accounting for pixel geometry and estimated photon detection efficiency. Each individual LED was flashed independently, and the intensity was measured on three different dates. The LEDs in a single flasher each have a different relative output. Here, the LEDs are numbered according to this output, with 1 being the lowest and 10 the highest.



**Fig. 21** Relative intensity levels for several combinations of flasher LEDs measured in the laboratory. The absolute scale of the relative intensity corresponds to the approximate number of photoelectrons per pixel expected in the camera running on the telescope, accounting for pixel geometry and estimated photon detection efficiency. A selection of patterns was chosen, combining one or more flasher LEDs. The intensity of these patterns was measured. Here, the patterns were ordered according to their intensity, with 1 being the lowest and 60 being the highest.

changes in the circuit performance when multiple LEDs are used impact the behavior of the flasher.

We show an example of the relative light levels from one flasher unit with the potentiometer set to 2.5 k $\Omega$  in Fig. 21. More combinations of LED on/off patterns can be used to achieve finer increments in light levels. The LED patterns shown are sorted by the light output. The light level is scaled so that it approximately corresponds to the number of photoelectrons (PE value) that a pSCT image pixel detects if the flasher is mounted on the pSCT (at a distance of  $\sim 1.86$  m). Note that the lowest order of magnitude of the output light levels (in this case, roughly between 8 and 80 PEs) is only covered by a few of the weakest patterns, whereas higher output levels are densely sampled.

The relative dynamic range covered by one flasher is slightly over two orders of magnitude. The full-width at half-maximum of the trace measured with the test PMT from all flasher pulses (with a 2.5-k $\Omega$  potentiometer setting) is well under 10 ns. The pulses have a rise time of under 4 ns and a somewhat slower decay (under 6 ns).

## 5.2 Camera Power Supply

Two NEMA weatherproof enclosures mounted in the telescope behind the camera contain rack-mounted power supplies and switches for the camera. The devices in the enclosures receive 120 V, 60 Hz power. One Acopian power supply provides power to the camera fans. Another power supply (Wiener PL506 series) provides power for all other camera components, including SiPMs and electronics. This power supply (PBN506 3U RASO) has a height of 3U, a total capacity of 3 kW, and interior space for six power supply modules, each providing an independent power channel. It currently contains three modules (model PBX506-EX), each operated at 70 V with 8 A capacity and  $\sim 90\%$  efficiency. One of the three modules powers all 25 FEE modules. Each module consumes  $\sim 13$  W under normal operation. This channel is isolated from the others for noise reduction.

The other two modules are tied together in parallel and power all other camera components (FEE, backplane, and Peltier system). This module is also operated at 70 V. DC-DC converters on the backplane convert the 70 to 12 V for use within the camera (see Sec. 4.1).

## 5.3 Camera Servers and Software

The event data stream generated by the camera is sent through the DACQ boards to a data server (DS) located in the pSCT server room over two 9/125 single-mode fiber lines (one per board). The connection is carried through a D-Link DGS-1510-28X 10 Gbps network switch.

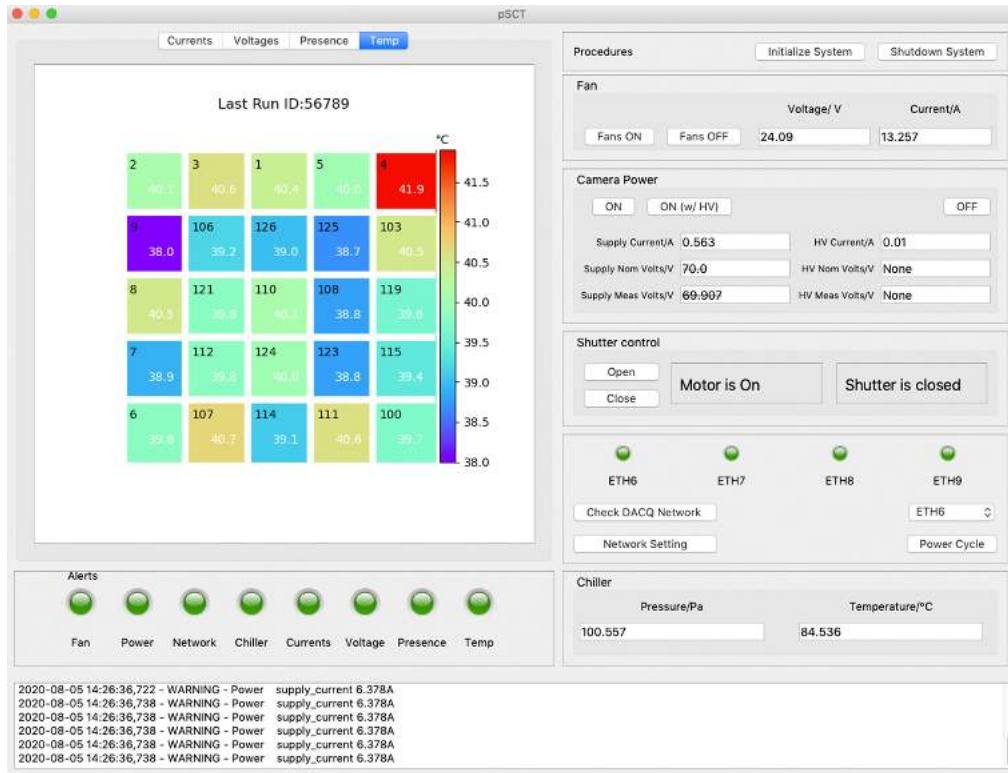
The DS, a rack-mounted 2U custom server from Aberdeen LLC, runs on a 10-core Intel Xeon E5 processor at 2.6 GHz equipped with 64 GB of DDR4 2133 MHz RAM on eight channels. The server, which is responsible for the data taking and general operation of the camera, also acts as a local data repository with 48 TB of storage space in a RAID6 configuration. The DS is equipped with a dual-port, 10 Gbps Intel X520 network interface card.

The main software components running in the DS are the SC and run-control (RC) systems. The slow control system is responsible for powering and monitoring hardware components of the camera, such as the backplane, FEE modules, chiller, fans, and SiPM temperature controllers.

The SC software suite is written in Python following a server-client model. The server runs as a daemon with continuous connection to the hardware components (each with a specific class providing access to its low-level functionality), and a Python client serves as a user interface that can send commands to the server or receive updates from it. High-level commands are defined by combining several low-level functions on multiple components into a single step, allowing for simplicity of control from the client side. The server-client communication uses the Protocol Buffers serialization library,<sup>19</sup> and commands and configuration settings are defined and stored in YAML files.

The SC system allows for the creation of alerts; nominal and alert values for monitored variables (such as currents, voltages, etc.) are defined, so an alert can be issued if a threshold value is crossed. Two implementations of the SC user interface (UI) exist: a command-line UI that provides fast access to the SC functions and is meant mainly for troubleshooting purposes and a basic graphical UI (GUI) meant for standard data-taking operations (see Fig. 22). The GUI is written in python and designed using PyQt5. The SC control server logs its output to a local log file and will also save monitoring variables to a local MySQL database.

The RC system of the pSCT follows a similar design to the SC system. Its main functions are to load the configuration settings of the FEE modules ahead of a data-acquisition run; to start, monitor, and stop runs; and to manage the recording of the physics-level and calibration



**Fig. 22** First version of the slow control GUI. Values are displayed at the FEE module level in this view.

data to disk. The RC system runs on a daemon server written in Python, which connects to the FEE modules using the TargetDriver and TargetIO libraries developed by the CHEC camera group.<sup>2</sup> The TargetDriver library is responsible for control and readout, and TargetIO reads/writes event data from the modules. The RC system is implemented as a state machine, with definitions that follow current CTA requirements on the possible camera states and allowed transitions.

Event data are sent from the camera to the DS as asynchronous UDP packets (two packets per event per module), which are buffered and assembled into full events based on their event trigger ID. Events are subsequently written to disk in FITS<sup>20</sup> files using the TargetIO library.

The data throughput that the DS must handle depends on the length of the readout waveforms, which can be modified, and the trigger rate, which depends on the trigger thresholds. Although first tests (e.g., Fig. 19) were performed using a 128-sample waveform, it is expected that a 64-sample waveform will be used in standard data-taking mode. The waveform digitizer dynamic range requires two bytes per sample for storage, which added to a five-byte header per waveform results in a waveform size of 133 bytes, or 200 kB for a full-camera readout of 1600 imaging pixels. A trigger rate of 1 kHz would result in a throughput of 1.6 Gbps, well suited for the prototype network and computing speeds.

## 6 Performance

pSCT performance testing focused on elements that were relevant to the camera upgrade. This includes software testing, waveform calibration, and trigger performance. Further performance testing is planned after the camera upgrade is completed.

### 6.1 Software Tests

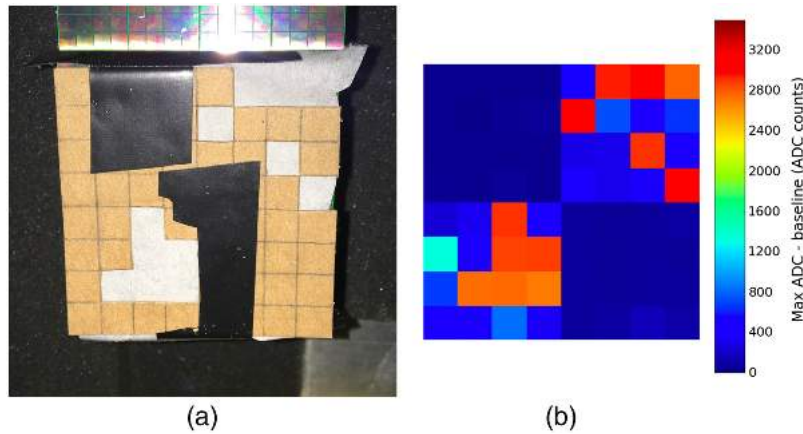
An initial software test checked that the pixels in the software were mapped correctly to their physical location in the camera. The camera can be easily run with a subset of modules. Because of this, we were easily able to identify that the module location in the software matched its physical location. To test the channel locations within a module, a mask test was done. This test consisted of masking off a subset of channels within a module and then flashing the module with an LED. The masked pixels were exposed to significantly less light, allowing us to differentiate between masked and unmasked pixels. A heatmap (shown in Fig. 23) of all of the pixels in the module showed that the pixels' locations in software correctly matched their physical locations.

A second software test checked that the flashers could consistently trigger the camera when used. To test this, a rate scan was run while the flashers were on. The flashers were run at 10 Hz, and the rate scan shows a clear plateau at 10 Hz, indicating that there is a wide range of thresholds over which the flasher will trigger the camera. Results of the flasher test are shown in Fig. 25.

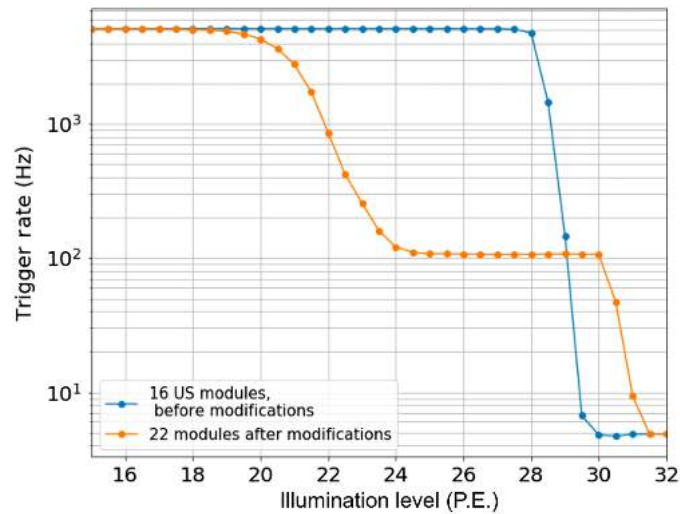
### 6.2 Waveform Calibration

Inside the TARGET7 chip, the data path (the path of the recorded charge from the sampling array through the analog buffer to digitization) is subject to variations in physical routing of the connections and variations in the capacitance of the storage buffer elements (see Appendix A for a more detailed discussion). Therefore, the buffer elements that were used need to be recorded with every waveform, and appropriate voltage to ADC count calibration needs to be applied on a sample by sample basis. The current strategy for calibration includes two steps: pedestal subtraction and ADC-to-voltage conversion via a lookup table.

For pedestal subtraction, a database needs to be created from pure electronic noise data to prevent bias from dark SiPM pulses. This can be achieved using a software trigger to produce waveforms with the SiPM bias voltage disabled. The first digitized block of a waveform shows a



**Fig. 23** The face of a single module FEE was first covered with a tissue (which allows light to pass through) and then with a cardboard mask. The mask was affixed to the FEE with black electrical tape. An LED was flashed on the prepared FEE. The left shows a picture of the physical setup of the module. The right shows the heatmap of average waveform height in different channels. Some cross-talk exists between adjacent pixels in the same quadrant. However, it is clear that the ASIC channels are connected to the correct Pixel IDs as those pixels exposed to LED pulses have significantly larger average waveform heights.



**Fig. 24** Trigger noise reduction. Prior to noise reduction steps, the trigger noise was high enough that it saturated the trigger system. After the noise-reducing modifications, the trigger rate was reduced to 22 PE for a 1-kHz trigger rate.<sup>4</sup>

systematic elevation in ADC counts, which needs to be accounted for when constructing the database and in calibration.

Once the pedestal subtraction is applied, the final step is to convert waveforms from ADC counts to voltage via a lookup table, which needs to be created from waveforms recorded at different input pedestal voltages. In general, for Hamamatsu sensors, the conversion for all cells is close to two counts for every 1 mV or eight ADC counts at the peak of a 1-PE pulse. FBK sensors have double the electronics gain of Hamamatsu sensors, and therefore the conversion is close to 16 ADC counts per 1 PE pulse. Once the ADC conversion is calibrated, the charge can be found by integrating over the waveform.

### 6.3 Noise and Trigger Performance

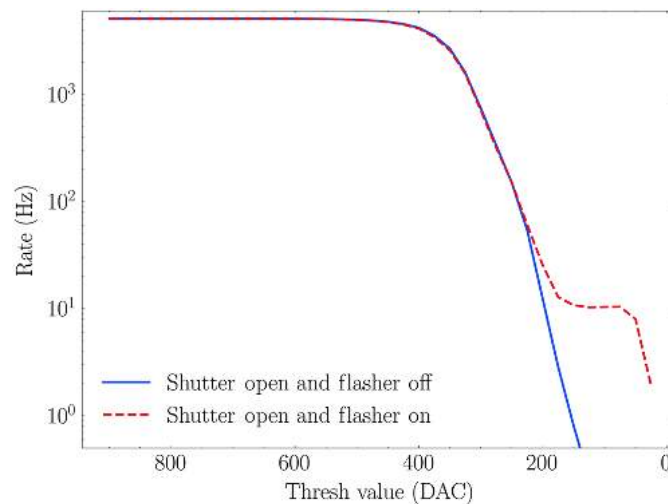
The trigger path of the camera is responsible for processing incoming signals quickly using higher-level logic to determine if the charges should be digitized and read out. On the module level, this is done with two inverting amplifiers per pixel and an inverting summing amplifier per trigger pixel. These are used to amplify and take the analog sum of a group of four pixels (called a trigger pixel). If this sum surpasses a selected threshold, then the module produces a trigger that is sent to the backplane.

Rate scans are one way to measure the effect of changing this threshold. A trigger is generated when the input signal crosses the specified threshold. A rate scan consists of systematically changing this threshold (starting at a high value and decreasing in regular steps) and measuring the trigger rate at each threshold. The trigger rate is measured by recording the TACK rate. When the threshold reaches the amplitude of an incoming signal, the rate rapidly increases. As the threshold is decreased further, the rate will increase again as the system begins to trigger on noise. Currently, the rate saturates at  $\sim 5$  kHz due to an enforced 200  $\mu$ s dead time. This dead time was implemented to ensure that modules would not trigger on noise produced by the module's own TACK signal.

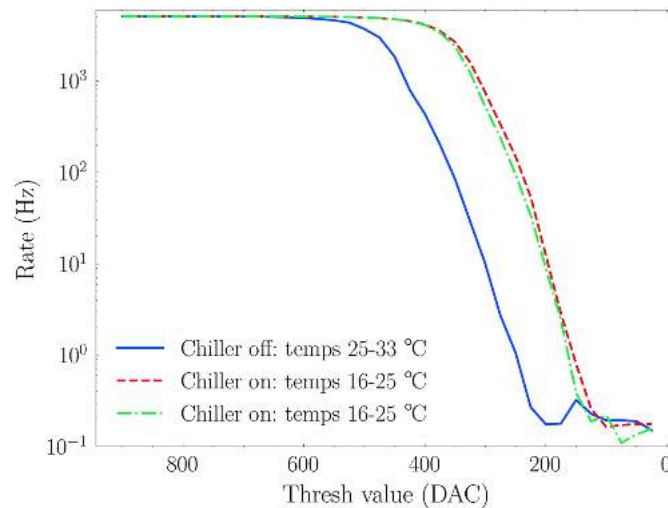
Because the incoming signal travels through three inverting amplifiers before being compared with this threshold, the way in which the threshold is specified is unintuitive. The threshold level is set by the Thresh parameter. A low Thresh value corresponds to a physically high threshold, whereas a high Thresh value corresponds to a physically low threshold.<sup>4</sup> US and INFN SiPMS have different gains (190 and 300 ADC ns, respectively), which means that the conversion between Thresh value and photoelectrons for both modules is different. For rate scans that include only one type of module (Fig. 24), it is straightforward to make this conversion; however, for rate scans that include a mix of modules (Figs. 25 and 26), it is impractical to make this conversion.

Noise in the trigger path can cause the module to trigger even when there is no signal present. Such noise was found to be caused by radiative coupling with the voltage regulators present on the module FEEs and with the aluminum housing within which the FEEs are fixed. The voltage regulators were redesigned, and the aluminum housing was replaced with a fiberglass alternative in all modules, significantly reducing the noise on the trigger path.<sup>4</sup> Figure 24 shows this reduction.

The nominal maximum rate at which the camera can be operated is 1000 Hz. The nominal maximum throughput that can be sustained is  $4 \times 1$  Gbps. (This corresponds to four 1 Gbps lines, two in each DACQ board.) The real maximum rate and maximum throughput have not yet been measured.



**Fig. 25** Rate scans with flasher on and off. Rate scans included all modules and were taken under typical operating conditions in the same night. The rate scan taken with the flasher on shows a clear plateau at 10 Hz (the same rate at which the flasher was run).



**Fig. 26** Rate scans included all modules and were taken with the shutter open on the same night so that ambient conditions were the same. One rate scan was taken with the chiller off, resulting in warmer average module temperatures. Two rate scans were taken with the chiller on, resulting in colder temperatures. Rate scans with a lower temperature are shifted to lower Thresh values (corresponding to a higher physical threshold).

Once installed in the telescope, further rate scans were taken to determine how the night sky background rate and inherent trigger noise rate compare. This was achieved by taking rate scans with the shutter closed (no night sky photons) and with the shutter open under similar circumstances. Figure 25 shows these rate scans.

It was also found that the temperature of the camera has a strong effect on the rate at a given Thresh value. The colder the temperature is, the higher the trigger rate for a given Thresh is. This is either due to an increase in noise or a change in the threshold with temperature. Figure 26 shows two rate scans taken at different temperature ranges to illustrate this effect.

## 6.4 Camera Images

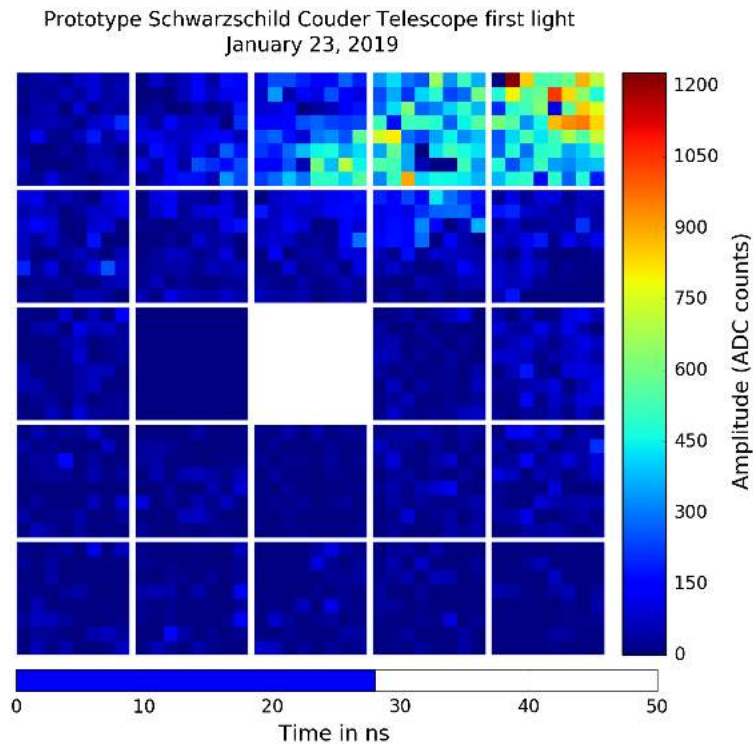
On January 23, 2019, the pSCT camera and optics were simultaneously uncovered for the first time. First light and first shower candidates were achieved on this date. Two runs were taken, one with and one without simultaneous flashers. One event is shown in Fig. 27.

At this time, the optics were not fully aligned, leaving some trace optical effects in the first light data. The optical alignment was completed in December 2019, and observations of the Crab Nebula began at that time. In January 2020, the pSCT recorded its first gamma-ray-like shower. This event is shown in Fig. 28. Observations in January 2020 led to a detection of the Crab Nebula at a significance of 8.6 sigma.<sup>21</sup>

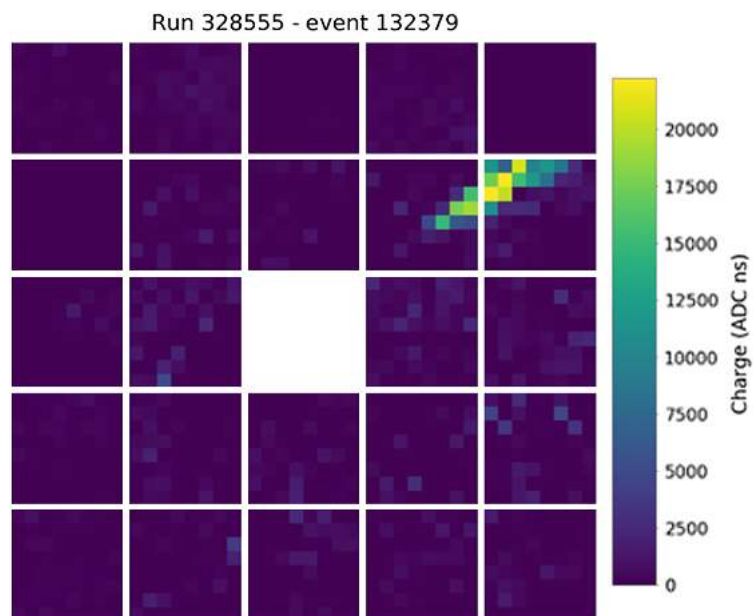
## 7 Camera Upgrade

### 7.1 Upgrade Outlook

The camera is scheduled to be upgraded by December 2022. The upgraded camera will have a fully populated focal plane, increasing the number of pixels from 1600 to 11,328, and will increase the FoV from 2.7 deg to 8.0 deg. This will require a total of nine backplanes (each with two DACQ boards), which will require synchronized timing between them. A DIAT system (See Sec. 7.2) will be used to achieve this and will ensure camera-wide triggers between backplanes (see Sec. 7.2). The backplane PCB will also be redesigned as its current form factor was intended to accommodate 32 modules as opposed to the 25 modules per sector required for the pSCT. Each backplane will control up to 25 FEE modules (corner backplanes control only 13



**Fig. 27** First light from the pSCT. First light and first shower candidates were achieved on January 23, 2019. This is a snapshot of a single event. The center module is blank because that position is temporarily occupied by an alignment calibration module. The module in the center left is dark because it failed to connect on this run.



**Fig. 28** First confirmed gamma-ray-like event recorded by the pSCT. This event was taken on January 17, 2020, with simultaneous observation with VERITAS. This event was confirmed as a gamma-ray via timing coincidence with simultaneous VERITAS observation.

modules; see Fig. 2). The nine backplanes will be mounted to the back bulkhead of the camera with their associated DACQ boards mounted on top of them.

The camera upgrade will represent a substantial reconfiguration in terms of the electronics components utilized. Instead of a mixture of FBK NUV-HD and Hamamatsu SiPMs, the entire camera will use the third-generation FBK NUV-HD SiPMs. These sensors demonstrate substantial improvements over those currently installed, including improved photon detection, lower temperature dependence, and lower breakdown voltage. The FEE modules will use a new design that incorporates next-generation TARGETC ASICs for digitization and sampling and a separate TARGET 5 Trigger Extension ASIC (T5TEA) for triggering. This new design is expected to significantly reduce trigger noise.<sup>16</sup> The PCBs for the new FEE modules are also improved over older designs.

Another new custom ASIC called the SMART chip is being developed to connect the SiPMs to the FEE modules. This chip will allow for improved control over SiPM bias voltages as well as pulse shaping and amplification directly at the SiPM sensors.

Auxiliary systems such as the heat management system and the camera shutter will also be improved during the upgrade. The heat management system, which currently accommodates 25 modules, will be improved to accommodate the 177 modules of the full pSCT camera. The LED flashers will also be upgraded to improve the performance and trigger synchronously with the backplanes.<sup>22</sup>

## 7.2 DIAT Board

The DIAT is a custom-designed board module for GPS time-tagging, timing synchronization, hit pattern preprocessing, and distributed trigger formation.<sup>23</sup> The DIAT was specifically designed to optimize the performance of the SCT and will replace the current time-tagging system (see Sec. 4.4).

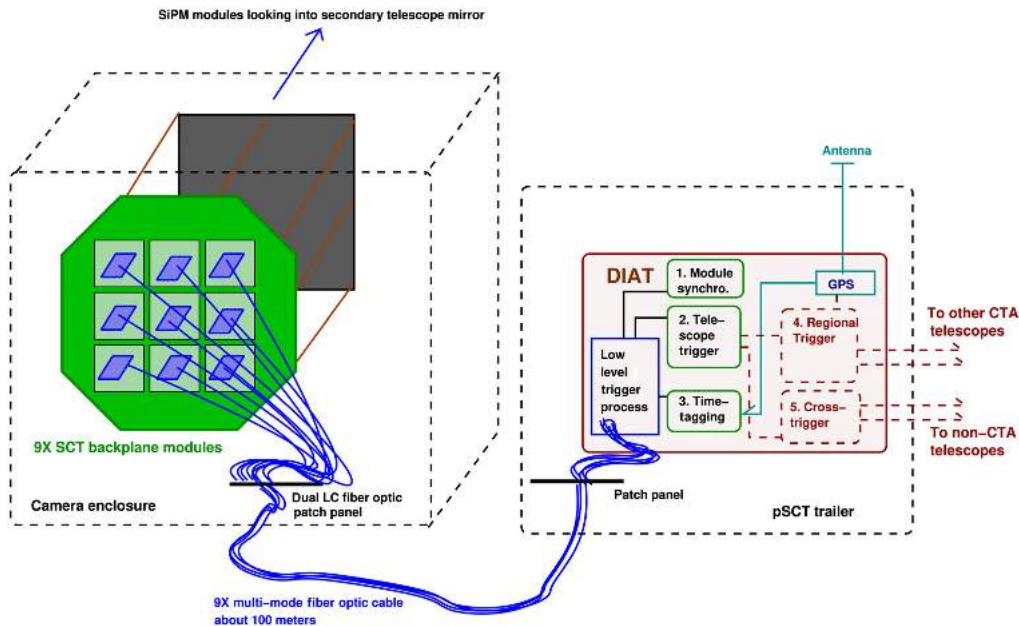
By design, the DIAT provides five key features to the operation of the SCT camera and telescope:

1. It provides a GPS-disciplined 62.5-MHz clock signal to each of nine backplanes, actively synchronizing the internal 125 MHz clock signals distributed to every FEE detector module within the camera.
2. It collects low-level trigger data from each of up to nine backplane modules within the camera to form a telescope trigger.
3. It provides nanosecond accuracy GPS time-tagging for all telescope trigger events.
4. It provides rapid, intelligent preprocessing of all low-level trigger information, resulting in a digital hit-pattern to indicate trigger pixels above the threshold. The DIAT uses these patterns to calculate lower order moments, which can then be shared with neighboring telescopes to form regional triggers, thus reducing the rate of spurious telescope camera triggers. These moments are also sufficient to veto cosmic-ray-induced air showers, which can further reduce triggers.<sup>23</sup>
5. Finally, it can also be programmed to enable synchronized timing and cross-triggers with any neighboring telescopes.

For the pSCT, a first “demonstrator” version of the DIAT is interfaced to the nine backplanes that will be present in the fully upgraded camera. The DIAT demonstrator provides functionality associated with features (1)–(3) listed above. In the pSCT, the DIAT will be installed within the data collection trailer and connected to the camera backplane via fiber optic cable and custom designed interface boards.

The critical role of the DIAT demonstrator for the pSCT is camera synchronization. Synchronization of the backend electronics and FEE is achieved by DIAT calibration of delays and by setting local clocks to the GPS disciplined clock of the DIAT. The messages between the DIAT and the backplane tell the backplane to set the 1-ns clock to some value on the next clock edge.

The FEE module does not inherently have true 1 ns precision. Instead it synchronizes with the 8-ns clock provided by the backplane. The module then reads the 64-bit 1-ns time



**Fig. 29** Conceptual schematic of the operation of the DIAT module (right) in relation to the full SCT camera with nine backplanes (left). Low-level trigger and timing messages from individual detector modules (FEE) are collected and relayed with timing information by each of nine backplane modules via fiber optic lines. The DIAT module (located within the telescope trailer) has five functions: (1) synchronization of detector modules, (2) telescope triggers, (3) GPS time-tagging, (4) regional triggers (via shared hit-patterns), and (5) cross-triggers with other telescopes in CTA. For the pSCT, the DIAT demonstrator module provides functions (1) to (3) as required for a single backplane.

and uses this to address the analog memory. The module resets the counter to the next 8 ns clock edge using SYNC messages generated by the DIAT, which are also passed through the backplane. The backplane in turn ensures that the 125-MHz clock is aligned to better than 80 ps.

The DIAT will provide functionality for synchronization for up to nine backplanes within the SCT camera and across multiple telescopes. Figure 29 shows a conceptual schematic of the DIAT in relation to the full SCT camera. The DIAT is designed to act as an intelligent trigger for both a single SCT telescope (generating telescope triggers based on information relayed from each backplane module). In principle, the DIAT can also provide functionality for cross-triggers with neighboring SCT telescopes within the larger CTA array.

The DIAT interface uses a SerDes device and SFP Gbit fiber connection to send the trigger time and hit pattern to a single DIAT module in the telescope operating trailer. If there are multiple backplanes or multiple telescopes, the DIAT derives a coincidence trigger and sends a message (a TACK command) back to each backplane in the camera. The 125-MHz backplane clock can be derived from a free-running oscillator (as it is for the prototype) or from a phase-locked clock derived by the DIAT interface board from the fiber-optic data connection. The DIAT uses time-of-flight message delays to synchronize the time on each backplane, ensuring that all backplanes and camera modules have a common absolute 1 ns time for time-tagging triggers and localizing the region of interest around each trigger in the analog pipeline.<sup>24</sup>

## 8 Appendix A: TARGET 7 ASIC Sampling Optimization

The TARGET 7 ASIC Sampler is comprised of two main parts: the sampling array and the storage array. The sampling array is designed to correctly sample the value of an incoming signal once per nanosecond. Then, these values are transferred from the sampling array to the storage

array. Finally, the data are stored in the storage array in a known order, so they can be reconstructed at a later time. The timing of this process is determined by six ASIC signals: SSTin, SSPin, STRB1, STRB2, Incr1, and Incr2.

## **8.1 ASIC Parameters and Definitions**

### **8.1.1 Sampling array**

The sampling array consists of 64 capacitors that record incoming signals. It is broken up into group 1 (capacitors 0 to 31) and group 2 (capacitors 32 to 63).

### **8.1.2 Tracking mode**

In tracking mode, a capacitor in the sampling array is allowed to take on the value of the incoming signal. (The SSTin/SSpin switch is closed.)

### **8.1.3 Holding mode**

In holding mode, a capacitor in the sampling array is held at some fixed value. (The SSTin/SSpin switch is open.)

### **8.1.4 SSTin (sample Start input)**

SSTin is the main clock in the ASIC. Its leading edge is defined to be 0 ns, and its trailing edge occurs at 32 ns. All other initialization parameters are measured from the SSTin leading edge. The leading edge switches the capacitors from tracking mode to holding mode.

### **8.1.5 SSPin (sample Stop input)**

The SSPin leading edge switches the capacitors from holding mode back to tracking mode.

### **8.1.6 Storage array**

The storage array has 512 blocks (8 rows  $\times$  64 columns) with each block containing 32 capacitors. The data taken by each group in the sampling array are transferred to the storage array for long-term storage.

### **8.1.7 STRB (write strobe)**

The STRB leading edge closes the switch between the sampling array and the storage array. The trailing edge opens this switch. Together the leading and trailing edges dictate both the time and the duration that the sampling array capacitors are connected to the storage array capacitors. There are two STRB parameters: one for sampling array group 1 (STRB1) and one for Sampling array group 2 (STRB2). The switch between the sampling array group and storage array must be closed after the signal is already stored and all of the capacitors in the group are converted to holding mode.

### **8.1.8 Write address**

The write address is also known as the block ID. It is the location within the storage array to which values from a sampling array group will be transferred. Each of the 512 locations in the storage array has a unique block ID between 0 and 511.

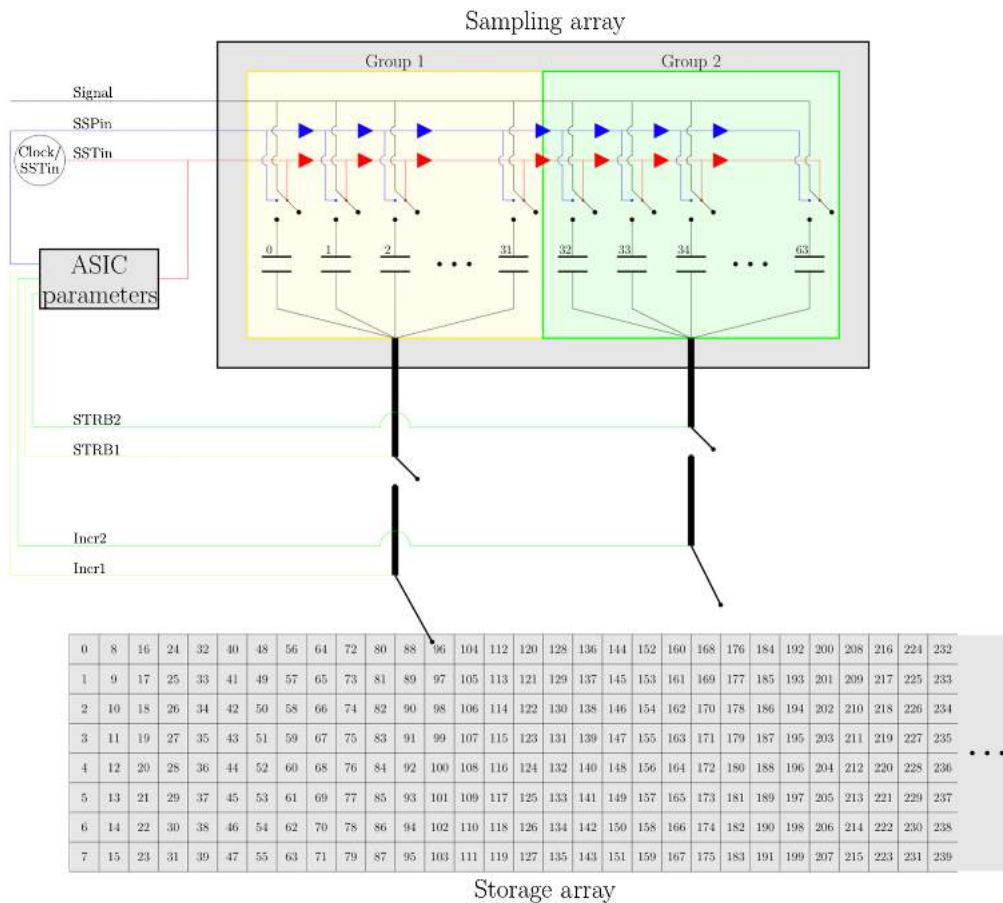
### 8.1.9 Incr (Increment)

The Incr leading edge increments the write address of the storage array by 2 (that is, it tells the STRB command the next place to connect the sampling array). This must occur before the sampling and storage arrays are connected with the STRB command (otherwise part or all of the data will be transferred to the wrong location). Incr1 increments the write address for group 1, and Incr2 increments the write address for group 2. Incr1 only writes to even blocks, and Incr2 only writes to odd blocks.

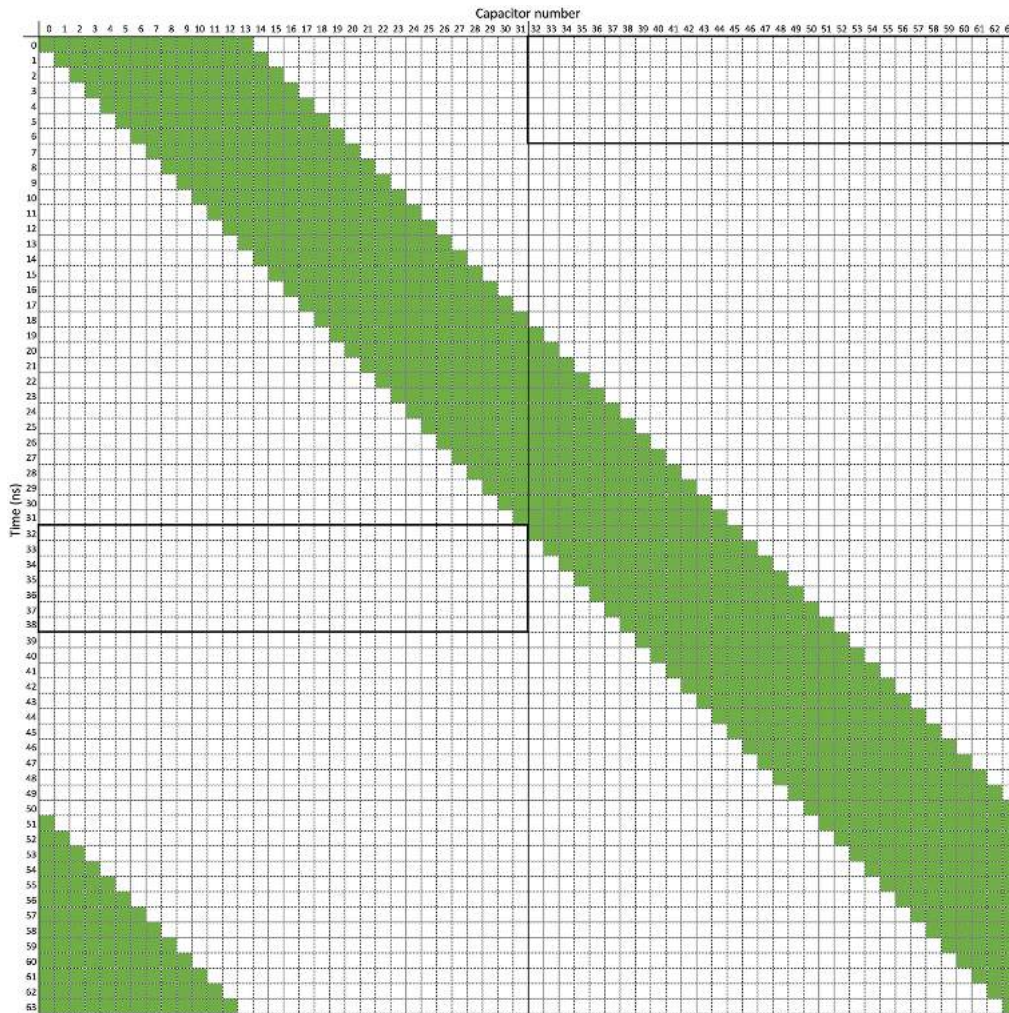
## 8.2 ASIC Functions

The sampling array is designed to correctly sample the value of the incoming signal once per nanosecond and then store these values long enough that they can be transferred to long-term storage. This is achieved by switching each sampling array capacitor between holding mode and tracking mode at the appropriate time. This is achieved through the SSTin and SSPin leading edges.

Both the SSTin and SSPin parameters must go through 1 ns delays after each capacitor (see Fig. 30). The SSTin leading edge is defined to be at 0 ns; thus at 0 ns, capacitor 0 switches from tracking to holding mode. However, the SSTin leading edge is delayed by 1 ns before it can reach capacitor 1. Thus, capacitor 1 switches from tracking to holding mode at 1 ns. This continues for



**Fig. 30** ASIC diagram including ASIC inputs, sampling array, and storage array and how they connect. The triangles on the SSTin and SSPin lines are 1 ns delay elements. When a signal hits a delay element, it is delayed by 1 ns for each element. Notice there are no delay elements on the signal line. The incoming signal hits all of the capacitors simultaneously. The Incr1 and Incr2 switches can connect to any storage array block, though the mechanism is more complicated than depicted here.

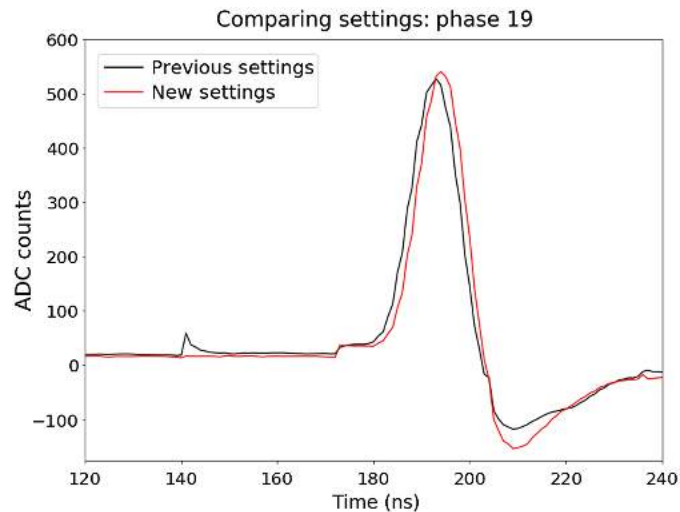


**Fig. 31** Holding/tracking diagram for the optimized ASIC settings. Capacitors are labeled on the top of the diagram, and as we move down the figure time progresses in steps of 1 ns. The state of each capacitor is given by the color. Green means the capacitor is in tracking mode, and white means it is in holding mode. The thick black boxes indicate the duration of the STRB for each group of capacitors.

subsequent capacitors, each with an additional 1 ns delay before it is affected by the SSTin leading edge.

Similarly, the SSPin leading edge hits capacitor 0 at 50 ns. However, capacitor 1 is not affected until 51 ns due to the delay. This, combined with the SSTin signal, produces a moving subsection of capacitors that are in holding mode as shown in the holding/tracking diagram (Fig. 31). Each individual capacitor is in holding mode for 50 ns, whereas each group has all capacitors simultaneously in holding mode for only 18 ns. Thus, there is an 18-ns window during which one group of the sampling array is storing 32 ns of signal.

Once values are properly stored short-term in the sampling array, the next step is to transfer those values into the storage array. This transfer process depends on both the Incr and STRB parameters for each group. The STRB parameter connects the sampling and storage arrays, allowing the stored data from one group on the sampling array to be transferred to one block on the storage array. Thus, the STRB parameter must begin and end within the 18-ns window during which the sampling array is in holding mode. After the values are transferred using STRB, the write address of the storage array must be incremented. This is achieved using the Incr parameter. It is important that the write address is incremented fully before the corresponding STRB leading edge occurs. Otherwise, current values will overwrite the values from the last transfer.



**Fig. 32** To compare the original ASIC settings (shown in black) with the optimized settings (shown in red and listed in Table 1), data were taken using an LED flasher with an asynchronous trigger provided by an external signal generator. The data were pedestal subtracted and averaged, once for the previous settings and once for the new settings. Because the location of the pulse in relation to the block boundary (called the “phase”) determines where the prepulse is located in the waveform, the two settings were compared individually for every phase. The figure on the right shows the difference between the previous and new settings for a single phase. It is clear that the new ASIC settings reduce the prepulse. Similar results are found for all phases.

To ensure that the values from each group do not interfere with one another, the following increment procedure is used. Group 1 only writes to even numbered storage array blocks, whereas group 2 only writes to odd numbered storage array blocks. Each group’s Incr parameter increments the storage array location by two. This produces a “ping-pong” effect in which one group is transferring data to the storage array while the other is taking data and incrementing its write address. After 32 ns, the two groups switch. Storing data in this way reduce the chance of error but also mean that the signals are not stored in order in the storage array. Individual waveforms that are longer than 32 ns are comprised of several storage array blocks. The write addresses of these blocks will have a  $+3/-1$  pattern, e.g., 0,3,2,5,4,7,6,9,8,11,...

Incorrect ASIC settings can produce waveforms in which part of the signal is located in the incorrect portion of the readout. This often looks like a “prepulse” occurring before the bulk of the signal. To reduce this effect, the ASIC settings were optimized. A comparison of the settings pre- and postoptimization is shown in Fig. 32. Optimized ASIC settings are shown in Fig. 31 and in Table 1.

## 9 Appendix B: Component Photos

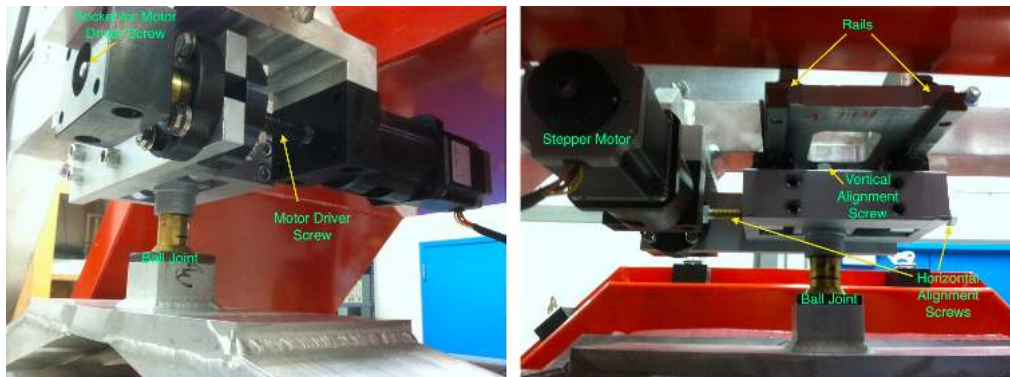
Figures 33–38 show photos of several pSCT components.

## Acknowledgments

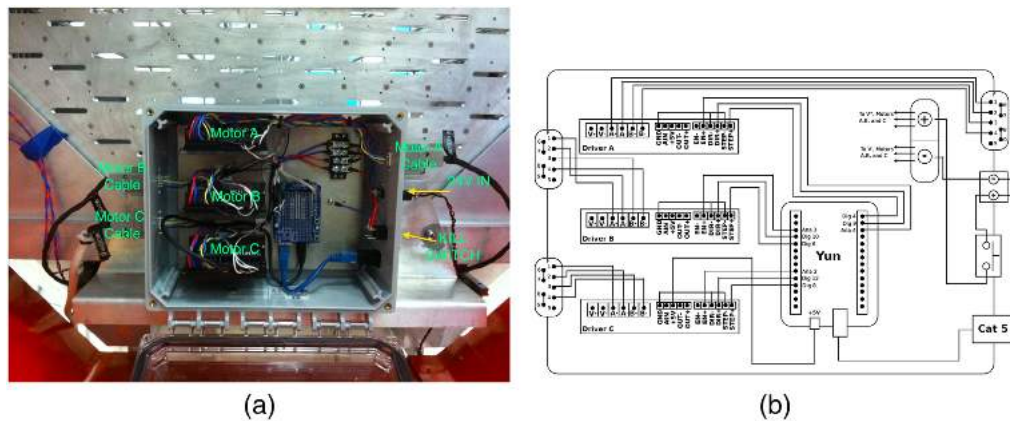
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**Table 1** Optimized ASIC initialization parameters.

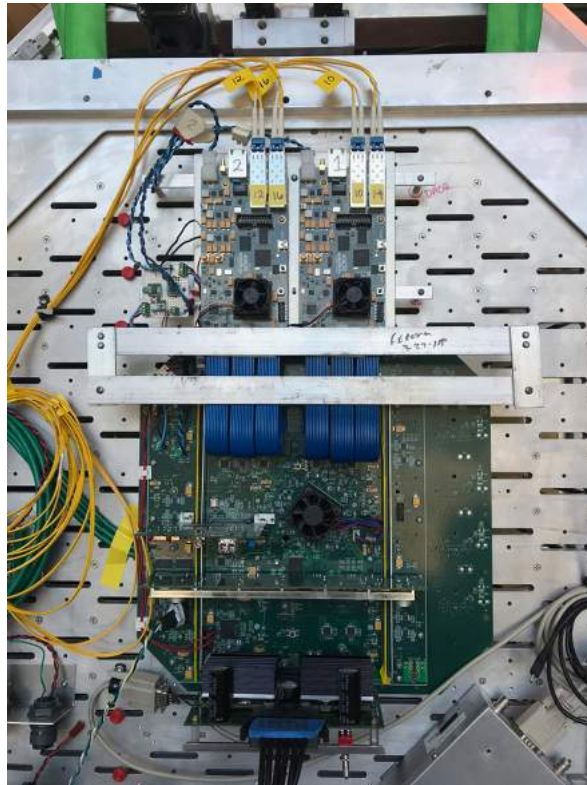
Parameter	Setting
SSTin_LE	0 ns
SSTin_TE	32 ns
SSPin_LE	50 ns
SSPin_TE	3 ns
Incr1_LE	3 ns
Incr1_TE	18 ns
STRB1_LE	32 ns
STRB1_TE	39 ns
Incr2_LE	35 ns
Incr2_TE	50 ns
STRB2_LE	0 ns
STRB2_TE	7 ns



**Fig. 33** Photo of motor assembly C, located at the top of the camera. Labeled are the ball joint, the motor driver screw, rails, vertical and horizontal alignment screws, and the stepper motor.



**Fig. 34** (a) Photo and (b) circuit diagram of the motor electronics box located in the back of the camera. This box includes an Arduino and three motors that control the movement of each stepper motor.



**Fig. 35** Photo of the backplane. The back bulkhead has two holes per module: one long slit for the module backplane connector and one for the module securing screw. The backplane is mounted onto this back bulkhead. Each module connects to the backplane through a backplane connector and is secured with a screw running through the backplane, bulkhead, and module. On top of the backplane are mounted two DACQ boards (top), one power board (middle), and two power connectors (bottom). The DACQ boards have two fiber cables (yellow), each leading to the network switch. The green cables allow a central alignment device, which can be installed instead of the central module, to connect to a positioner. This device is used to align the camera and optics. The Raspberry Pi is in an aluminum box in the lower right corner and is connected to the backplane via an SPI link through a D-shell connector. The fans are connected to the backplane via a small board in the upper left corner.



**Fig. 36** Photo of the demonstrator DIAT on a laboratory test stand, connected to the pSCT camera backplane. The DIAT is a single-board custom-designed module for time-tagging, timing synchronization, hit pattern processing, and cross-triggering. Fiber optic ports on the front panel connect to up to nine SCT backplanes for the full-sized camera.



**Fig. 37** Photos showing main components of the standalone timing system: (a) the laser-diode module, which is installed near the telescope camera backplane, and (b) the photo-diode and GPS timing module, which is installed in the pSCT trailer.



**Fig. 38** Photograph of one of three LED flashers currently installed in the pSCT. The cover containing the diffuser is open to expose the LEDs and circuit inside the module. The flasher enclosure is 8 cm × 8 cm × 5.5 cm, and the diffuser lens has a diameter of 2.5 cm.

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Biographies of the authors are not available.