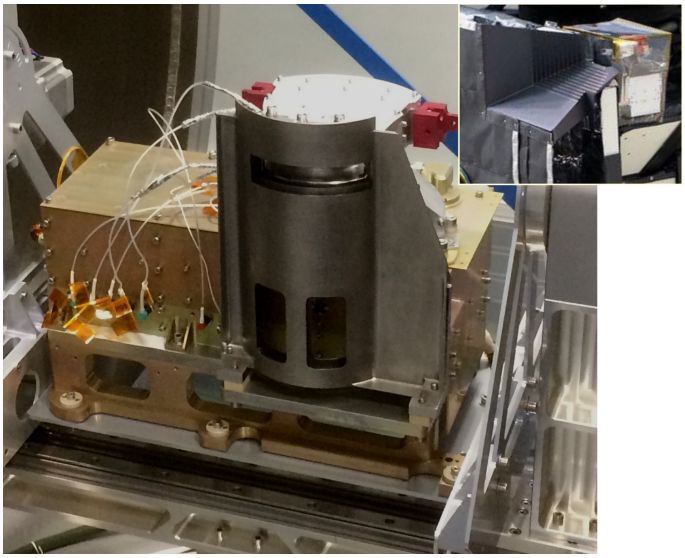

Fig. 18. Flight model of the SWA-PAS unit in the vacuum chamber during its calibration. The white analyser head is mounted on the top of the electronics box. Both are located behind the SWA-PAS-specific heat shield. Inset to the top right shows the sensor mounted behind its scalloped cut-out in the main spacecraft heatshield.

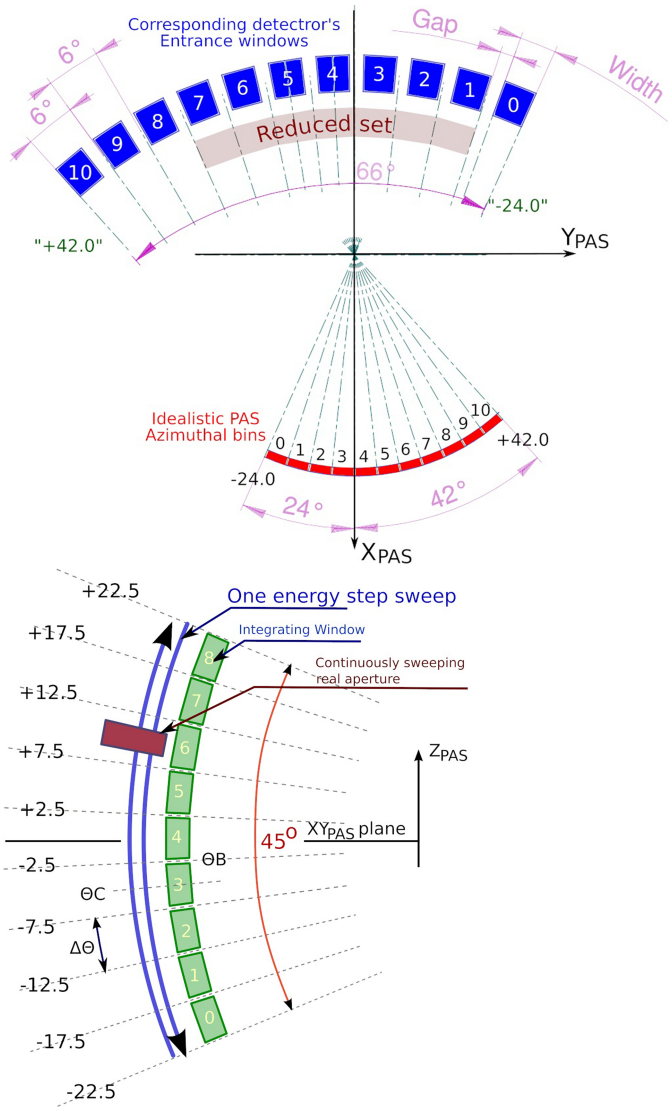

Fig. 19. SWA-PAS detector angular bins defined by the sensor geometry for the azimuth bins (*top panel*) and by deflector sweep for the elevation bins (*bottom panel*).

elevation and energy bins, SWA-PAS performs elevation sweeping and energy stepping (see Figs. 19 and 20). For a given energy, SWA-PAS makes a continuous sweep over the elevation range. The width of the instant elevation response is ~3°. To fill one bin, SWA-PAS opens the corresponding counter when the elevation scan enters the corresponding elevation bin, and stops the counter when the scan leaves the bin. As soon as one full elevation sweep is completed, SWA-PAS transfers to another energy step (Fig. 20). The transition time, ~2 ms, is that needed to stabilise the deflector HVPS. SWA-PAS transmits the data from the eleven CEMs to the SWA-DPU as soon as counts from one elevation bin are accumulated.

The duration of the full 3D sampling period consisting of (96, 9, 11) elements is exactly 1 s. The SWA-PAS design allows for the reduction of the number of energy steps and elevation angles, and also the use of seven rather than eleven channeltrons. Reduced VDFs are then obtained: for example, samples of (48, 9, 7) or (24, 3, 7), etc. Importantly, in these cases the reduced set of the energies is a subset of the energies of the full 3D sampling. The same is true for the elevation subsets. This allows placement of the 2D energy-elevation sub-window of the reduced sample in any position inside the full sampling window. If the duration of the reduced sample accumulation is less than the full sampling duration, SWA-PAS can perform several samplings per second. This fundamental advantage of the SWA-PAS operation allows the sensor to capture short-duration, high-cadence snapshots. The full set of the constants defining the SWA-PAS instant energy-elevation window is shown in Table 5.

In nominal operation, one VDF (one 1 s 3D VDF sample) will be measured each 4 s, with 3 s idle time between samples. This provides the basis to determine the density, velocity, and pressure of the solar wind at the required 4 s cadence.

3.3.4. SWA-PAS design details

From the functional point of view, SWA-PAS can be divided into five subsystems (see Fig. 21) as follows: (1) the electrostatic analyser, (2) the CEM board with the detectors, (3) the HVPS board providing HVs for the sensor head optical surfaces, (4) the FPGA board hosting the necessary digital data processing, and (5) the DC-DC converter providing the corresponding LV power. All electronics boards are located the SWA-PAS electronics box. It is not expected that the electronics box will need to be heated when the spacecraft is far from the Sun. However, for safety reasons, an operational heater is located on the side of the electronics box. The heater is powered via the same primary power line as SWA-PAS itself. The FPGA provides very simple open-loop heater control.

The SWA-PAS electrostatic analyser has no direct heritage in past space plasma instruments. Since corresponding instruments flown on HELIOS and on Bepi-Colombo are, or were, on spinning spacecraft, their plasma instrument designs did not need to include elevation steering. The Parker Solar Probe ion instrument is completely protected by the spacecraft heat shield and does not need special design to accomodate direct exposure to sunlight. However, the SWA-PAS sensor head must look directly at the Sun, which has driven the need to design the SWA-PAS analyser from the scratch. No existing coating can survive in such conditions, thus the entrance collimator and the

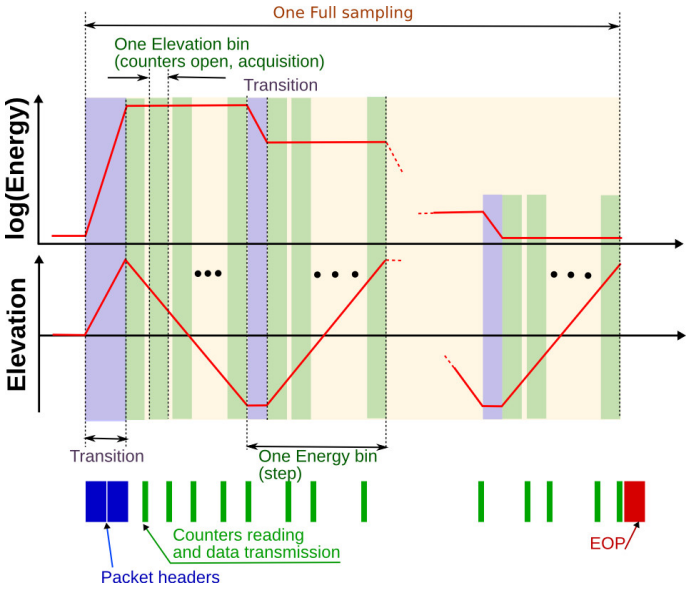

Fig. 20. SWA-PAS Energy – Elevation sampling waveform. The transition time, 2 ms, is needed to stabilise the deflector HVPS. Without this delay, the slope on the HV is perturbed at higher elevations.

Table 5. Constants controlling the SWA-PAS reduced energy-elevation window.

Parameter	Description	Possible values
Ne	Number of energy bins	2, 4, 6, ... 92
Se	Start position of the energy window	Any if the window does not exceed 0 or 95
Nel	Number of elevation bins	1, 3, ... 9
Sel	Start position of the elevation window	Any if the window does not exceed 0 or 8

deflector plates exposed to sunlight are made of polished aluminium. The electrostatic analyser spheres, less impacted by thermal flux, are scalloped and coated by Ebonol "C" UV absorbing film. The insulation of the deflector plates must be maintained up to 10 keV, since the steering of 20 keV charged particles requires at least 5.5 keV sweeping voltage. We describe the analyser properties in more detail in Sect. 3.3.5.

The CEM board is the uppermost board in the SWA-PAS electronics box. It serves as a base-plate for eleven ceramic CEMs mounted via two semi-metallised Ultem holders (Fig. 22). A corresponding set of eleven anodes lies under the CEM assembly, surrounded with a grounded guard fencing, made as a part of the outer golden metallisation layer. The anodes are internally routed and capacitively coupled to the hybrid charge-sensitive pre-amplifier-discriminators. The pre-amplifier digital output signals exit the board via logical buffers and level shifters and are passed to the FPGA board where the detected particles are counted. Each pre-amplifier-discriminator can register 6×10^6 Poisson-distributed pulses per second and their thresholds are set by fixed resistors to $\sim1.5\times10^5$ e^-. In order to save electrical power, the pre-amplifiers are switched off during the idle phases of the measurement (independently for the central and lateral sections).

The channeltron exits are kept at a potential ~-100 V, while the CEM entrance grids are biased to the CEM bias (-3900 V maximum). Two CEM variants with different resistances are used in the SWA-PAS detector to decrease the total power consumption. CEMs with nominal resistance of 80 MΩ, allowing maximum count rate 10^7 s^{-1}, are used for the azimuthal sectors 2−6. Sectors 0, 1, 7−10 utilise CEMs with nominal resistance of 200 MΩ (maximum count rate 10^6 s^{-1}) (see Fig. 19 and Table 6). Two independent HV converters (HVC) provide CEM bias for the central CEMs (sectors 1−7) and the lateral CEMs (sectors 0, 8−10). The count versus HV bias profile of both types of central CEMs are very similar, so it is unnecessary to provide separate voltages on them. Both HV converters work at 25 kHz, synchronised by a phase-locked loop (PLL) circuit to the 5 kHz clock signal provided by the FPGA board. When working with the reduced set of azimuthal sectors, the lateral pre-amplifiers and the lateral CEM HVC are always off. To minimise electromagnetic emissions and channeltron noise, the CEM board provides a single point connection between the SWA-PAS internal electrical and mechanical (chassis) grounds.

Table 6. SWA-PAS CEM properties.

CEM #	0	1	2−6	7	8−10
Resistivity, MOhm	200	200	80	200	200
Central or lateral	L	C	C	C	L

Two temperature sensors are glued near the two outermost channeltrons to monitor their operational temperatures. The CEM operational temperatures are a critical factor for detector lifetime and the SWA-DPU continuously monitors the corresponding HK values. If the temperature becomes too high, the CEMs are switched off immediately.

The SWA-PAS HVPS board provides four very fast varying HV voltages for the electrostatic analyser optical surfaces. Figure 23 shows the wave-forms of HVPS outputs. The deflector voltage linearly sweeps from -2000 V up to 5500 V over 10 ms. To provide the necessary waveform, the HVPS switches the output voltage sign and changes the internal gain of the source to transfer from the highest voltages to the lower voltage range needed for the low energy measurements.

The SWA-PAS HVPS provides a static voltage source, ±6500 V, which powers four opto-coupler-based fast HV drivers. The design includes dedicated opto-couplers, maintaining 12 keV bias, for the HVPS. The HPVS instant output is controlled by FPGA via a very fast LVDS data line.

As shown in Fig. 21, the FPGA code functionality is divided into several subsystems: (1) SpW interface; (2) SWA-DPU command decoder; (3) operational heater control; (4) HVPS control; (5) CEM HV control; (6) 11 fast counters; (7) HK acquisition unit; and (8) sequencer. The HV control system is a fast multi-channel LVDS control of the DACs integrated with the dedicated boards. The HK control is a multiplexing multi-channel analogue-to-digital converter control. Several channels needed for critical control, such as the operational heater, can be measured and transmitted to SWA-DPU at a factor of 20 times faster than other HK parameters. The counters can count up to 10^7 events per second.

The main FPGA subsystem is the sequencer, which gives significant flexibility to the system. The sequencer is an embedded programmable controller which allows simple mathematical operations, performs simple execution control loops, and "if-else" switching. The sequencer calculates HV values for the next substep using appropriate constants held in a small look-up table (LUT), and sends the commands to the HVPS board. It opens and closes the counters at the required times and forms

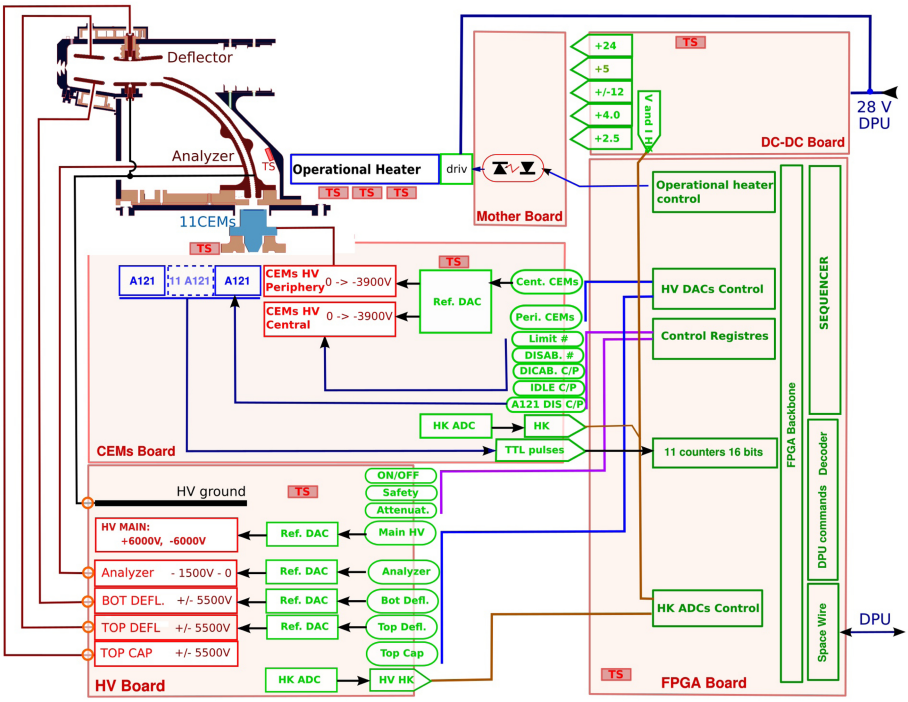

Fig. 21. Block diagram of the SWA-PAS system.

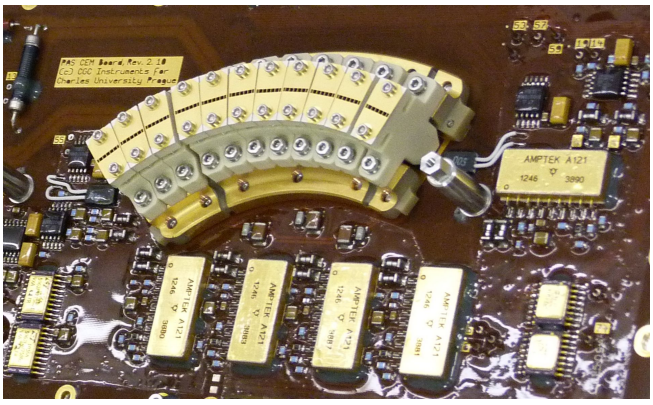

Fig. 22. Detail of the SWA-PAS CEM board depicting the assembly of the eleven ceramic channel electron multipliers. Two HV isolation gaps between the seven central CEMs and one + three lateral CEMs allow their independent operation. Hybrid charge sensitive pre-amplifiers-discriminators are placed on both the top and the bottom sides of the PCB near the lower voltage side of the channeltrons. Two temperature sensors are glued left and right of the channeltron set to monitor the temperatures of the CEM board.

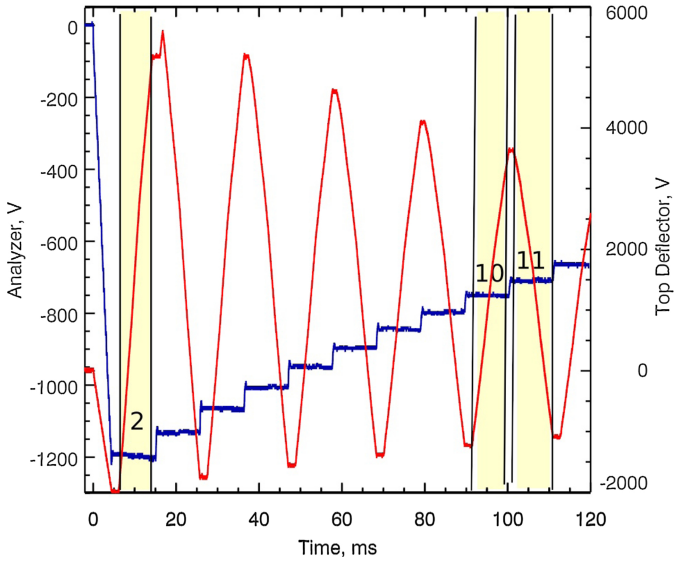

Fig. 23. SWA-PAS HVPS waveforms taken at the beginning of a sampling period. Blue trace: energy analyser voltage; red trace: top deflector voltage. The yellow bars show the time intervals for count accumulations.

the data packet. The sequencer controls the HK acquisition and performs all other actions needed to control the sensor.

3.3.5. SWA-PAS characterisation and calibration

A summary of the steps in the characterisation and calibration of SWA-PAS elements and the whole sensor is shown in Table 7.

As shown in Fig. 24 the "top-cap" voltage can be varied over a relatively large range for a given elevation bin. The analyser properties vary significantly with the "top-cap" polarisation. A trade-off is thus required between the bin geometrical factor, the energy, and the angular resolutions, in order to establish the optimised combination of parameters for operation. The FPGA sequencer can be programmed with the optimal values, as shown in Fig. 25.

Once SWA-PAS optical surface voltages are optimised and SWA-PAS FPGA tables are uploaded in flight, we can perform a full SWA-PAS calibration procedure, measuring the energy-angular-response of each angular bin. The integration of these responses provides the full matrix of SWA-PAS geometrical factors. An example of such responses are shown in Fig. 26.

3.3.6. Summary of SWA-PAS specifications at delivery

A summary of the design goals versus the obtained SWA-PAS properties is given in Table 8. The performance is close to that expected on the basis of numerical simulations of the design, with minor exceptions. The energy resolution varies between 3%