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Authors	FOCARDI, MAURO, Pace, E., FARINA, Maria, DI GIORGIO, Anna Maria, Sierra-Roig, C., Colome, J., Ribas, I., Gesa Bote, L., MORGANTE, GIANLUCA, TERENCE, LUCA, Da Deppo, V., PEZZUTO, Stefano, Ottensamer, R., Noce, V., PANCRAZZI, Maurizio, Malaguti, G., MICELA, Giuseppina, Pascale, E., Eccleston, P., Amiaux, J., Cara, C., Tommasi, E.
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M. Focardi^a, E. Pace^b, M. Farina^c, A. M. Di Giorgio^c, C. Sierra-Roig^{d, e}, J. Colome^{d, e}, I. Ribas^{d, e}, L. Gesa Bote^{d, e}, G. Morgante^f, L. Terenzi^f, V. Da Deppo^g, S. Pezzuto^c, R. Ottensamer^h, V. Noce^a, M. Pancrazzi^b, G. Malaguti^f, G. Micelaⁱ, E. Pascale^{l, m}, P. Ecclestonⁿ, J. Amiaux^o, C. Cara^o, E. Tommasi^p, and the ARIEL System Team^{*}

^aINAF-OAA, Arcetri Astrophysical Observatory, Largo E. Fermi 5, 50125 Firenze - Italy

^bUniversity of Florence - Department of Physics and Astronomy, Largo E. Fermi 2, 50125 Firenze - Italy

^cINAF-IAPS, Institute of Space Astrophysics and Planetology, Via del Fosso del Cavaliere 100, 00133 Roma - Italy

^dICE-CSIC, Institute of Space Sciences, Carrer de Can Magrans, Cerdanyola del Vallès, 08193 Barcelona - Spain

^eIEEC, Institute of Space Studies of Catalonia, Despatx 201, Edifici Nexus Gran Capità, 08034 Barcelona - Spain

^fINAF-OAS, Astrophysics and Space Science Observatory, Via P. Gobetti 101, 40129 Bologna - Italy

^gCNR-IFN, Institute for Photonics and Nanotechnologies, Via Trasea 7, 35131 Padova - Italy

^hUniversity of Vienna - Institute of Astronomy, Türkenschanzstraße 17, 1180 Vienna - Austria

ⁱINAF-OAPa, Astronomical Observatory of Palermo, Piazza del Parlamento 1, 90134 Palermo - Italy

^lUniversity of Rome - "La Sapienza", Piazzale Aldo Moro 5, 00185 Roma - Italy

^mUniversity of Cardiff, School of Physics and Astronomy, The Parade CF24 3AA, Cardiff - UK

ⁿSTFC-RAL Space, Rutherford Appleton Laboratory, OX11 0QX Harwell Oxford - UK

^oCEA-Irfu, Department of Astrophysics, 91191 Gif-sur-Yvette - France

^pASI - Italian Space Agency, Via del Politecnico, 00133 Roma - Italy

^{*}refer to the ARIEL Mission Consortium

ABSTRACT

The Atmospheric Remote-sensing Infrared Exoplanets Large-survey (ARIEL)¹ Mission has been recently selected by ESA as the fourth medium-class Mission (M4) in the framework of the Cosmic Vision Program. The goal of ARIEL is to investigate, thanks to VIS photometry and IR spectroscopy, the atmospheres of several hundreds of planets orbiting nearby stars in order to address the fundamental questions on how planetary systems form and evolve.²

During its four-years mission, ARIEL will observe several hundreds of exoplanets ranging from Jupiter- and Neptune-size down to super-Earth and Earth-size with its 1 meter-class telescope.³ The analysis of spectra and photometric data will allow to extract the chemical fingerprints of gases and condensates in the planets atmospheres, including the elemental composition for the most favorable targets. It will also enable the study of thermal and scattering properties of the atmosphere as the planet orbits around its parent star.

Send correspondence to: Mauro Focardi

E-mail: mauro.focardi@inaf.it, Telephone: +39 055 275 5213

The ARIEL telescope will feed, by means of a collimated beam, two separated modules hosted in the Payload⁴ (P/L); the main instrument, i.e. the IR Spectrometer (AIRS), providing variable spectral resolutions in the range 30-180 for a waveband between 1.95-7.8 μm and a combined Fine Guidance System (FGS) VIS-Photometer/NIR-Spectrometer module hosting 3 photometric channels in the range between 0.50-1.2 μm to monitor the photometric stability of the targets. Two of these channels, commonly referred as the FGS, will also be exploited by the S/C as a prime/redundant system for fine guidance and closed-loop control. Integrated in this combined module is a further low-resolution ($R \simeq 10$) spectrometer in the 1.2-1.95 μm waveband.

The Payload is passively cooled to ~ 55 K by isolation from the Service Vehicle Module (SVM) via a series of V-Groove radiators and, to constrain the thermo-mechanically induced optical aberrations, the temperature of the primary mirror will be monitored and finely tuned thanks to an active thermal control system based on thermistors and heaters. They will be switched on and off to maintain the M1 temperature within ± 1 K thanks to a proportional-integral-derivative (PID) controller implemented within the Telescope Control Unit (TCU), an electronics subsystem in charge of the active thermal stabilization of the detectors assemblies belonging to AIRS and FGS, besides M1.

TCU, as baseline, shall also control the on-board IR calibrator by means of an accurate feedback-loop system, the M2 secondary mirror refocusing mechanism and will collect the housekeeping of the managed subsystems, forwarding them to the Instrument Control Unit (ICU), the main electrical I/F to the Spacecraft (S/C).

The ICU processor will run the Application SW⁵ in charge of instrument management and data processing and it will feed and control the TCU, collecting all the needed housekeeping for the management of the monitored subsystems.

ARIEL is highly complementary to other on-ground and space observatories (such as Kepler, TESS and PLATO) and will take advantage on the success of previous already flown missions, which will provide an optimized list of targets (~ 500 planets at least).

This paper will focus on the P/L warm electronics, on ICU and TCU architectures in particular.

Keywords: Exoplanets atmospheres, transit spectroscopy, payload electronics, Instrument and Telescope Control Units, Application SW.

1. INTRODUCTION

The ARIEL Payload (refer to Fig. 1) is conceived to seamlessly perform variable low-resolution spectro-photometry in the band [1.20-7.80] μm and to monitor the stellar activity in the visible and NIR range. It is based on a modular architecture, including both cold and warm electronics subsystems.

The Focal Plane Assemblies (FPAs) host the detectors and their Cold Front End Electronics (CFEes), interfaced to the warm electronics side (WFEes), working at ambient temperature, by means of a dedicated harness, composed by different parts each one linked to heat sinks and radiators. The AIRS and FGS (Fig. 2) warm electronics are called, for historical reasons and heritage, Detectors Control Units (DCUs) and are located on the warm part of the Service Vehicle Module (SVM). DCUs are interfaced to the FPA CFEes and their detectors in order to control the detection process, and to the ICU to transfer the Science Data Packet towards the Spacecraft. A dedicated unit for temperature monitoring and fine regulation (TCU) completes the warm electronics subsystems suite.

The Cold Electronics subsystems (SS), detectors and their control electronics, are located on the cold side of the Payload to limit noise and efficiently detect the IR spectroscopic signatures of the selected exoplanetary atmospheres and targets. AIRS detectors shall work down-to ~ 42 K, while their CFEes will be operated at a higher temperature.

Some European options are under study at CEA (F) for what concern the AIRS IR sensors selection, but the baseline design foresees the adoption of the HIRG-type detectors from Teledyne.

As well as for the detectors case, a European ASIC, designed to drive and readout the IR sensors, is under development at SRON (The Netherlands Institute for Space Research) but the baseline solution adopts the

Teledyne SIDECAR ASIC, already developed to drive efficiently the H*RG detectors and tested in relevant space environments.

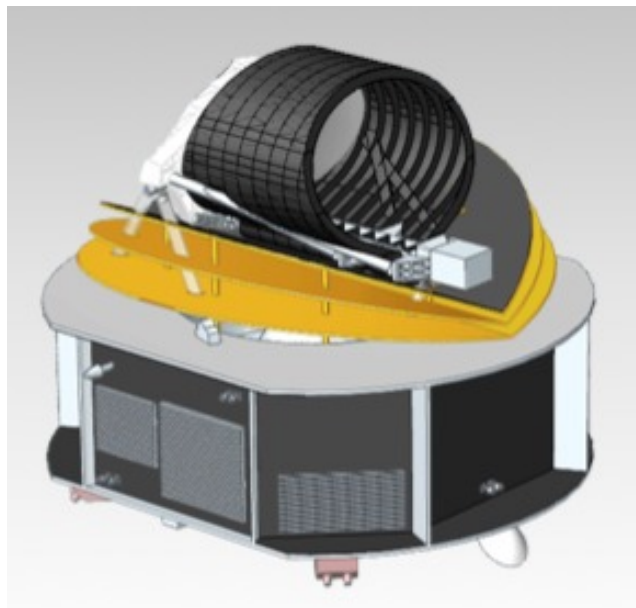


Figure 1. ARIEL cold (top) and warm (bottom) Payload. The telescope and optical bench hosting the suite of instruments are decoupled by the Service Module, working at ambient temperature, by means of bipods and three V-grooves (in yellow).

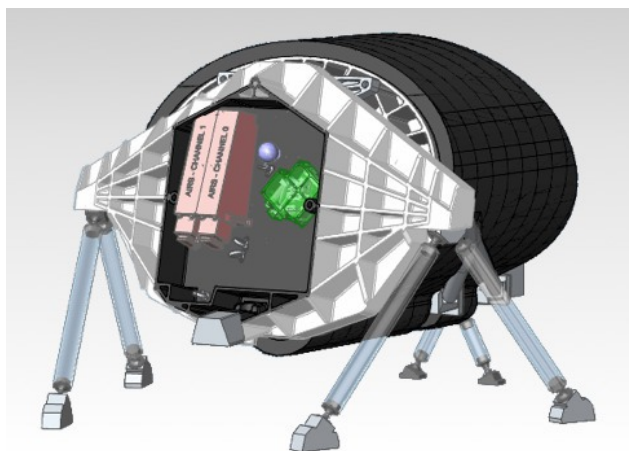


Figure 2. Back-side of the ARIEL telescope with the optical bench hosting AIRS (in pink) and the FGS (in green). The blue sphere represent the IR calibrator unit.

2. WARM ELECTRONICS DESIGN

The warm electronics units DCUs (for AIRS and FGS), ICU^{6,7} and TCU^{8,9} (refer to Fig. 3 for the mechanical design and to to Fig. 4 for the electrical configuration) are located on the warm part of the P/L, the SVM, maintained at ambient temperature ($\sim 270\text{-}300\text{ K}$). These units host analog and digital electronics, whose aim is to drive and control the overall data acquisition chain (scientific data and instrument housekeeping, HK), monitoring the telescope and the payload subsystems temperatures, commanding the AIRS instrument and provide the SVM with the scientific telemetries and the P/L health status.

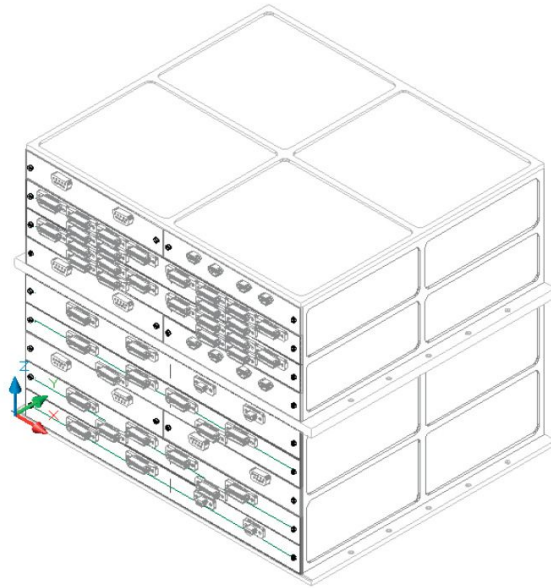


Figure 3. The stacked drawers configuration for the overall assembly including ICU, TCU and the two DCUs for the AIRS spectrometer (Channel-0 and Channel-1), as designed during the Assessment Phase of the ARIEL Mission.

Presently, along with the baseline design here described, an alternative configuration for the P/L warm electronics part is under study, in order to exploit a common solution for the implementation of an HW synchronization module as well as for scientific data routing and HW compression, if actually needed.

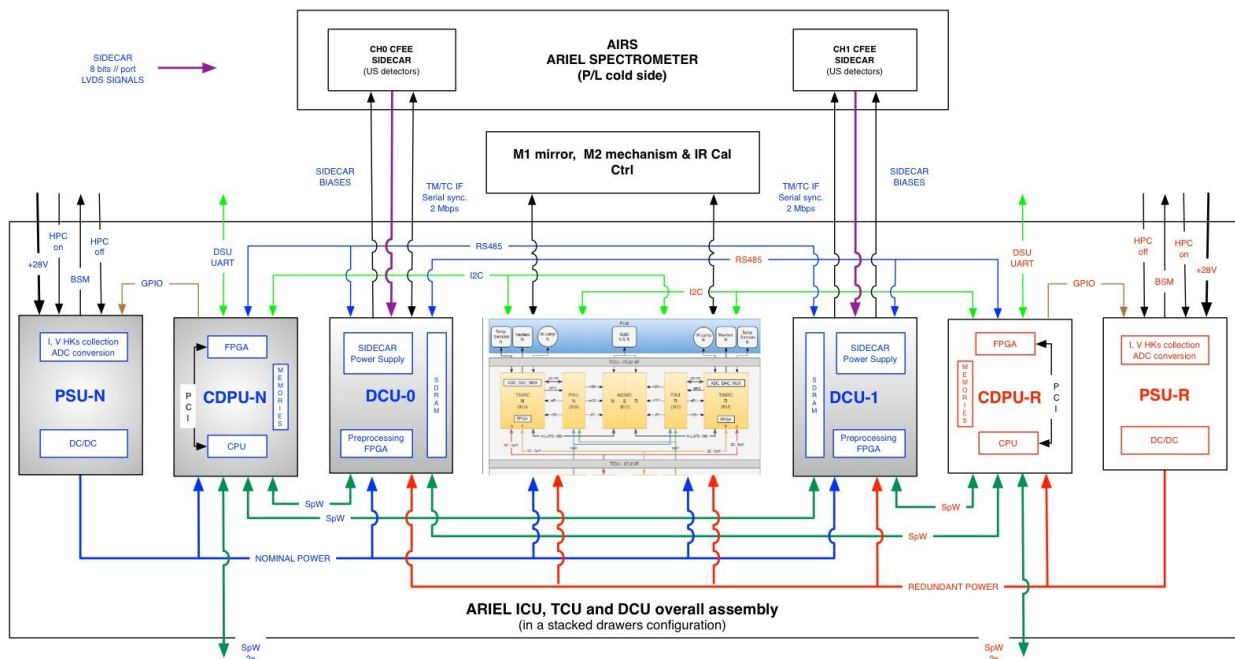


Figure 4. Electrical configuration of the overall assembly hosting ICU, TCU and DCU. Blue labels are used for ICU and DCU Nominal boards while, in red are represented Redundant boards. The central part of the block diagram shows an embedded electrical scheme for the TCU's 3N and 3R boards, as described in the text.

The alternative design would take advantage from a consolidated configuration already developed for the NISP Instrument on-board EUCLID, for what concern DCUs and HW synchronization, and from a design under development and validation for the PLATO ICU¹⁰ Routing and HW Data Compression board.

While the design requirements and common architecture of the AIRS and FGS DCUs are still to be defined, as their actual characteristics will be bounded to the final detectors choice, the ICU and TCU units relies on more consolidated architectures,¹¹ as described in the following.

2.1 DCU design

The Detector Control Unit(s), as baseline, adopt the same design for both AIRS and FGS. They interface directly the CFEEs and the detectors to manage the detection process and the ICU to transfer the Science Data Packets. Their main functions are:

- control the scientific data acquisition at detector level, through the CFEE;
- process the data from the detector prior the formatting of the Science Data Packet done by ICU;
- ensure the proper interface with the ICU for TC reception, HK and Science Data Packet transmission.

DCUs for both AIRS and FGS could be based on a different design only in case AIRS will benefit of the implementation of European detectors; in that case an ASIC or a mixed-signal CFEE, based on discrete components, could be adopted as its executive design will start early this summer at SRON.

2.2 ICU design

The ICU baseline design relies on two Nominal plus two Redundant boards, in a cold-redundant scheme, able to support the cross-strapping configuration of the the TCU Units (N and R):

- 2 (N + R) Power Supply Units (PSU);
- 2 (N + R) Commanding and Data Processing Units (CDPU).

Their design and development are under the Italian responsibility, as well as the Application SW (ASW), running on the ICU processor.

2.2.1 Power Supply Unit

PSU hosts DC/DC converters with a number of secondary sections needed to support the adopted cross-strapped and partially redundant configuration as DCUs, as baseline, are not redundant because their reliability, as achieved for the NISP data acquisition chain design, is very high ($\geq 98\%$).

It is in charge of collecting currents, voltages on secondary outputs and temperatures HK (A/D converted internally to the Unit, exploiting the serial HK I/F for signals and control lines to/from the ADCs).

The ICU consumption monitoring is in charge of the Platform as well as the Instrument switching on/off by means of HPC commands (both PSU and CDPU boards are switched on at the same time, thanks to a sequencing logic owing to PSU, after whose activation the booting sequence take place).

2.2.2 Commanding and Data Processing Unit

The CDPU is based on a CPU (the UT699E Processor from Cobham Gaisler, as baseline) and a co-processing FPGA (Microsemi RTAX type), hosting some peripherals.

Memories for:

- booting (PROM),
- storing the ASW (E2PROM and/or non-volatile memory (NVM) e.g. MRAM),
- data buffering (e.g. SDRAM),
- data processing support (e.g. SRAM, SDRAM),

are included in the design as well. The two main blocks, i.e. the UT699E CPU and the RTAX FPGA are connected through an on-board cPCI bus.

The selected enhanced UT699E CPU is a 32 bits fault tolerant LEON3FT SPARC V8 microprocessor supporting up to 100 MHz clock rate and allowing up to 140 DMIPS. The processor includes an on-chip Integer Unit (IU), a Floating Point Unit (FPU), a Memory Controller with a DMA Arbiter and an UART-based Debugging Support Unit (DSU) I/F. It is interfaced to the on board FPGA by means of a 32 bit wide, 33 MHz, cPCI bus supporting DMA (Direct Memory Access).

One of the main characteristics of the adopted UT699E CPU is the on-board availability of 4 embedded SpW links (2 supporting the Remote Memory Access Protocol -RMAP- protocol) allowing to be directly interfaced to the SVM (Data Management Subsystem -DMS-, composed by the On Board Computer -OBC- and the Solid State Mass Memory -SSMM- Units) and to the DCU SpW I/F.

The RMAP protocol could be exploited to read from and write directly to the DCU FPGA registers as the CDPU FPGA, along with the processor, is in charge of the DCU board management and of the data acquisition and pre-processing tasks, e.g. implementation of the HW compression core.

CDPU FPGA is also interfaced to the TCU Thermal Stabilizer and IR Calibrator (TSIRC) board by means of an I²C bus or SpW I/F (for parameters configuration, telescope mirrors temperatures and mechanisms HK telemetries acquisition).

An embedded Finite State Machine (FSM), in charge of controlling and scheduling the FPGA tasks, is foreseen along with an AMBA AHB/APB bridged bus to connect and control all the internal peripherals thanks to an AHB arbiter.

Finally, an on-board Point of Load (PoL) is included in the CDPU design, with the aim of providing all the needed fine-regulated voltage levels to feed properly the processor and the FPGA (IC core voltages).

As alternative to the adoption of the UT699E as main processor, the Cobham/GR UT700 or the GR712RC dual-core LEON3FT CPU could be selected. The latter results to be one of the eligible on-board CPU for implementing both instrument control and data acquisition and processing functionalities (e.g. for SW data compression), exploiting properly its dual-core-based nature, as in this configuration, two instances of the RTEMS OS can be executed.

The GR712RC can exploits up to 6 embedded SpW I/F if no SDRAM-type memory is directly interfaced to the processor, otherwise only 4 links are available, as in case of the UT699E CPU.

The final and proper selection of the processor to be adopted for the management of the AIRS Spectrometer and the P/L subsystems will be done during the present phase of the Project (B1), once the overall requirements on instrument management and data processing will be available. Indeed, the choice of a dual-core architecture, should be really justified by the actual need in terms of CPU resources (mainly peripherals, as the GR712RC too guarantees up to 140 DMIPS when running at 100 MHz).

2.2.3 CDPU on-board SW

The CDPU science data handling functionalities include the AIRS spectrometer digital data acquisition, buffering, pre-processing and lossless compression.

Both scientific and HK data are packetized according to the CCSDS/PUS (Packet Utilization Standard) protocol format and sent to the S/C DMS for storing and later downloading to Ground. Preprocessing and compression tasks can be disabled in case of raw data request from the Spacecraft/Ground (mandatory requirement).

The science data handling functionalities will be implemented by the ICU Application Software, as baseline the only high-level SW running on the AIRS warm side. It handles all the ICU/Spectrometer and ICU/TCU digital interfaces and implements the following Instrument monitoring and control functionalities: verifying and executing the telecommands received from the S/C, handling the switching on/off of the ICU and TCU subsystems, configuring and commanding the spectrometer sub-units, monitoring the ICU and AIRS units, reporting housekeepings and events, supporting the payload Fault Detection, Isolation and Recovery (FDIR) procedures and the operational modes, managing the on-board time and the Instrument synchronization.

These functionalities will be implemented by means of the CCSDS PUS services, as all the mandatory PUS services, requested to properly manage the P/L, will be guaranteed along with a set of services specific to the ARIEL Mission and its Payload.

2.3 TCU design

The Telescope Control Unit is in charge of the following tasks:

- Monitor the temperatures of the P/L elements reading several thermistors;
- Control the thermal stability of the Thermal Control Systems (TCS) of the AIRS and FGS detectors and M1 mirror);
- Drive the M2 refocusing mechanism;
- Drive the IR calibration lamp.

TCU is composed of three boards, as described in the following paragraphs.

2.3.1 Power Supply Unit

A dedicated Power Supply Unit (TCU-PSU) is foreseen for TCU, which will generate (from the main power line of +28 V coming from ICU) all the voltage levels required by the M2 mechanism driver (M2MD) and TSIRC boards. The system will be based on a full cold redundancy, with all the needed boards resting inside dedicated drawers on top of the ICU Units, as represented in Fig. 3.

2.3.2 Thermal Stabilizer and IR Calibrator

The TSIRC board will hosts the P/L thermal monitoring and control HW, the IR calibration lamp driver and their multiplexing stages.

The digital system of TSIRC will be based on a FPGA only hosting an internal logic to control all the TCU boards as a slave system of ICU, in order to simplify the overall SW architecture of the ICU and TCU assembly. The FPGA will host two Digital Signal Processing Modules (DSPM, one for the thermal monitoring subsystem and the other one for the IR calibration lamp driver), five PID controllers, GPIO interface management to generate multiplexers addresses and select the proper voltage and gain for a given thermistor, as well as to control Output Power Controllers (OPCs) of TCU-PSU.

It will also include a memory bank, two I²C (or SpW) links to communicate with CDPU and one MIL-STD-1553 (or SpW as well) link to communicate with the M2M Driver.

The telescope thermal monitoring will be performed by means of two types of sensors: Cernox thermistors for precise readings (detectors, M1, optical elements, etc.) and DT-670 diodes for housekeeping TM of other

elements of the PLM (V-grooves, OB, baffle, etc.). These sensors will be driven and read-back thanks to the TSIRC electronics.

The thermal stabilization of the TCS (which are placed between critical detectors/mirrors and their thermal sinks) will be carried out by monitoring the relevant temperatures and activating their heaters once the correction has been calculated by a PID control loop.

Detectors will have a single heater to stabilize their temperature, but M1 requires several (3 to 5) heaters to help an effective distribution of the heat. Survival heaters and thermistors might be installed in each TCS as well, but these are assumed to be completely in charge of the S/C.

The IR calibration lamp, located on the optical path between AIRS and FGS, will be based on a thermal source to generate the proper light spectrum for the detectors. The thermal source consists, as baseline, of a 4-wires tungsten filaments in order to power and read its voltage at the same time.

ARIEL requirements foresee an high-resolution DAC to control the filament current once ground test has found the proper current to achieve the required temperature (~ 1100 K) at the tungsten filament. The proposed architecture foresees a 24-bit (equivalent resolution) PID feedback loop in order to control the calibration lamp power with a better resolution than one part over a million.

2.3.3 M2M Driver Unit

For the driver electronics of the M2 mechanism, it is foreseen an upgraded version of the GAIA and EUCLID M2M, with the same driver, which will require a separated board for both nominal and redundant systems (M2MD).

The mechanism will have three degrees of freedom (tip/tilt and piston) controlled by a dedicated driver hosted inside TCU box. The system will rely on a board with an embedded cold redundancy configuration, where nominal coils of the stepper motors are connected to the nominal section of the driver, and backup coils are connected to the redundant section.

2.4 Conclusion

In this paper we have provided an overview of the current design of the ARIEL warm electronic subsystems, ICU and TCU in particular, at the beginning of the Phase B1 of the Project. The present architecture is still under consolidation as it will undergo two following reviews by ESA during the next two years, the P/L Preliminary Design Consolidation Review (PDCR) and the System Requirements Review (SRR).

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