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EChO Payload electronics architecture and SW design

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Abstract EChO is a three-modules (VNIR, SWIR, MWIR), highly integrated spectrometer, covering the wavelength range from 0.55 μm , to 11.0 μm . The baseline design includes the goal wavelength extension to 0.4 μm while an optional LWIR module extends the range to the goal wavelength of 16.0 μm .

An Instrument Control Unit (ICU) is foreseen as the main electronic subsystem interfacing the spacecraft and collecting data from all the payload spectrometers modules. ICU is in charge of two main tasks: the overall payload control (Instrument Control Function) and the housekeeping and scientific data digital processing (Data Processing Function), including the lossless compression prior to store the science data to the Solid State Mass Memory of the Spacecraft. These two main tasks are accomplished thanks to the Payload On Board Software (P-OBSW) running on the ICU CPUs.

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1 Introduction

The Exoplanets Characterisation Observatory [1] is designed as a dedicated survey mission for the study of the atmospheres of a selected sample of extra-solar planets. This main scientific goal can be achieved by using the transit and eclipse spectroscopy method, to observe exoplanets for which the contrast between planet and host star can be as low as 10^{-5} , and will be typically of the order of 10^{-4} . As a consequence, the main aim of the EChOs payload instrumentation will be to perform time-resolved spectro-photometry (no angular resolution is required as no imaging is foreseen on FPAs) exploiting the temporal and spectral variations of the signal due to the primary and secondary occultations occurring between the exoplanet and its parent star. Moreover, in order to extract the planet spectral signature and probe the thermal structure and the physical and chemical properties of its atmosphere [2], it will also be necessary to have a large and simultaneous wavelength coverage to detect as many molecular species as possible and to correct for the contaminating effects due to the stellar photosphere at the same time.

To fulfil all these requirements, the EChO scientific payload [3] has been conceived as a multi-modules highly integrated spectrometer covering the baseline wavelength range from $0.55 \mu\text{m}$ to $11.0 \mu\text{m}$. An optional long wavelength channel extends the range to the goal wavelength of $16.0 \mu\text{m}$, while the baseline design of the visible and near infrared channel [4], [5] includes the goal wavelength extension to $0.4 \mu\text{m}$. A Fine Guidance Sensor (FGS), necessary to provide closed-loop feedback to the high stability spacecraft pointing system (AOCS, Attitude and Orbit Control System), is also included in the EChO payload instrumentation (see Fig. 1).

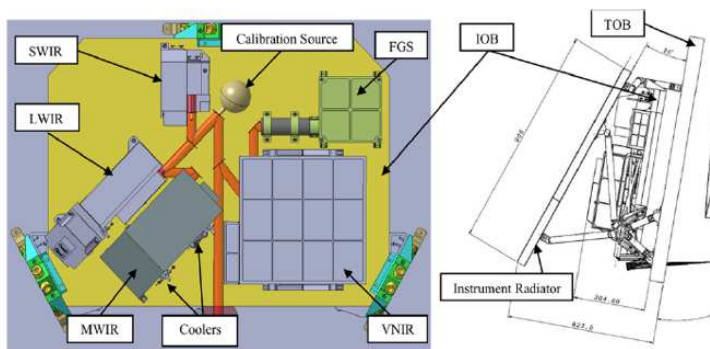


Fig. 1 EChO Payload optical bench hosting the Science Modules.

The spectrometer modules share a common field of view, with the spectral division achieved using a dichroic chain operating in long-pass mode. The five core sci-

ence channels include a cross-dispersed spectrometer (Visible/Near Infrared channel, VNIR) operating in the range from 0.4 to $\sim 2.5 \mu\text{m}$, a grism spectrometer (Short Wave InfraRed channel, SWIR) operating between 2.5 and $5.3 \mu\text{m}$, a prism spectrometer (2 Mid Wave InfraRed channels, MWIR) covering the long wavelength range from 5.3 up to $11 \mu\text{m}$, and a long (optional) wavelength spectrometer operating between 11 and $16 \mu\text{m}$ (Long Wave InfraRed channel, LWIR). All science modules and the FGS are accommodated on a common Instrument Optical Bench. The payload instrumentation and the detectors proximity electronics are passively cooled at $\sim 45\text{K}$ with a dedicated instrument radiator for cooling the FGS, VNIR and SWIR detectors to 40 K. An Active Cooler System based on a Neon Joule-Thomson Cooler provides the additional cooling to $\sim 28 \text{K}$ which is required for the longer wavelengths channels (MWIR, LWIR).

The overall EChO payload design, as well as its electrical architecture, has been conceived to maintain a high degree of modularity. This approach helps both technically and programmatically in allowing for independent development of the different modules.

In this paper we provide an overview of the EChO payload electronics and on-board software. The presented architectures are a result of the trade-off processes driven by the mission science requirements, aimed at satisfying both the need to minimize the overall system complexity and the requirements on the overall system budgets.

2 Payload electrical architecture overview

The EChO electrical architecture [6], [7] has been logically divided into two main segments: spectrometers detectors and proximity (cold) electronics on one side, and a spectrometers data handling warm electronics on the other side.

The cold segment hosts the Focal Plane Arrays (FPAs), the ROICs (Read Out Integrated Circuits), the active thermal stabilisation electronics and the cold front-end electronics (CFEEs). The warm electronics contain the warm front-end electronics (FEEs) and implements the unique payload instruments interface to the spacecraft On-Board Computer, hosting nominal and redundant connections for all the digital data links (telemetry, telecommands and housekeeping). The unit implementing these functionalities is called Instrument Control Unit (ICU).

The baseline scientific focal plane arrays are MCT (Mercury-Cadmium-Telluride) detectors for the short wavelengths channels and Si:As for the (optional) longest wavelengths channel. A block diagram of a spectrometer module electrical architecture (e.g. VNIR channel) is shown in Fig. 2. The detectors signals are readout by the Analog/Digital CFEEs ASICs, operating at a temperature of $\sim 50 \div 55\text{K}$ and located at a distance $\leq 0.5 \text{m}$ from the focal plane arrays. The digital signals are then handled by the warm front end electronics (WFEEs), which are located at a $\sim 2.5 \div 3.5 \text{m}$ distance from the FPA, and sent to the Instrument Control Unit.

The ICU provides the main functionalities to manage all the instrument subsystems implementing detectors commanding, science and housekeeping data acquisition, calibration sources and mechanisms handling and the overall on-board com-

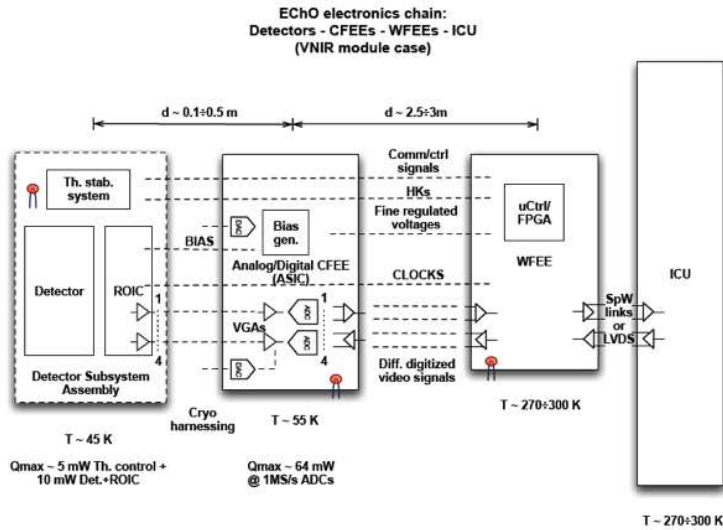


Fig. 2 EChO VNIR module electrical architecture.

munications management. In the present baseline design WFEEs support the ICU in performing the distributed digital pre-processing of data coming from the CFEEs and in generating their control digital signals. ICU and WFEEs, being warm electronics units operating at $\sim 273 \div 300 \text{ K}$, shall be located inside the SVM (Service Vehicle Module), a module thermally decoupled from the telescope optical bench.

The ICU electronics will rely on a cold-strapped redundant architecture with some trade-off solutions removing or mitigating any electronics single-point failure. Presently the full cold redundancy is foreseen at board level exploiting the ICU passive back plane as the main support for the cross strap routing. This baseline solution will be studied in more detail in the following phase taking into account FMECA (Failure Mode, Effects, and Criticality Analysis) and FDIR (Fault Detection Isolation and Recovery) studies at electronics subsystems level. As alternative solution the full cold redundancy could be implemented duplicating all the electronic boards in a cold-spare cross-strapped configuration.

2.1 Detectors

Within the Consortium, detectors development and testing activities are presently aimed at increasing the technology readiness level of the European candidate MCT detectors operating in the IR range (e.g. arrays of 512×512 pixels with $15 \mu\text{m}$ pixel pitch coupled to an ASIC for CFEEs from the Dutch SRON) and at developing MWIR new devices. In the present baseline, however, the detectors for the VNIR, SWIR and FGS modules will be Teledyne HgCdTe arrays with $512 \times 512 - 18 \mu\text{m}$ pixel pitch (H2RG devices [8], [9], [10], [11]). These arrays are produced in US and are presently

the only ones at the required TRL level with an expected noise well within the EChO requirements.

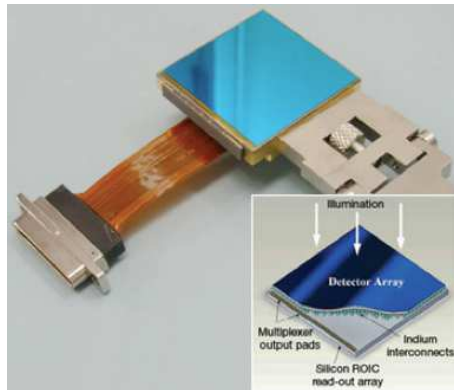


Fig. 3 An example of a MCT detector from Teledyne: a H2RG hybrid array with $18 \mu\text{m}$ pixel pitch. Courtesy Teledyne.

One key outcome during the Assessment Phase was the identification of an MCT detector with TRL approaching 5 that worked up to $11 \mu\text{m}$ at an operating temperature of $\sim 40 \text{ K}$. Due to the lack of a MCT European solution for the MWIR channel, the Teledyne NEOCam device was selected as the baseline. This led to a change in the instrument baseline with the expectation that we could have an all-MCT solution with operating temperatures no lower than 28 K (a constraint due to the desired lower dark current at longest wavelengths). The advantage of this solution is the simplification of the payload cooler by avoiding the use of an active two-stage cooler otherwise required to operate the currently foreseen Raytheon Si:As detectors down to 7 K .

Following these considerations, in the baseline payload design, all spectrometer modules will host MCT-type detectors (Fig. 3) from Teledyne electrically and mechanically bonded with their ROICs.

All ROICs will have at least four or more analogue outputs, amplified and interfaced with their own CFEE (i.e. the SIDECAR ASIC [12], [13]) where analogue to digital conversion will take place.

2.2 Cold Front End Electronics (CFEES)

Baseline configuration. As described above, the foreseen baseline solution adopts SIDECAR ASICs from Teledyne as CFEEs for the VNIR, SWIR, MWIR and FGS modules. This solution is the best one to drive properly the US MCT detectors and to save mass, volume and power at the same time. To greatly improve Sensor Chip Arrays (SCAs) integration by reducing size, overall system performance, Teledyne developed the SIDECAR (System for Image Digitisation, Enhancement, Control And Retrieval) ASIC [14], [15]. SIDECAR is a SCA interface chip that provides clocks

and biases to the SCA, and performs amplification and analog-to-digital conversion of the SCA analog outputs. It can run with up to 36 ADC with a maximum sampling frequency of 500 kHz. In Fig. 4 the ICU is interfaced to the SIDECAR ASICs by means of WFEEs, one per each scientific focal plane array (spectrometer), which is connected to the CFEEs and detectors modules by means of suitable cryo-harness as described in the harnessing section of this paper.

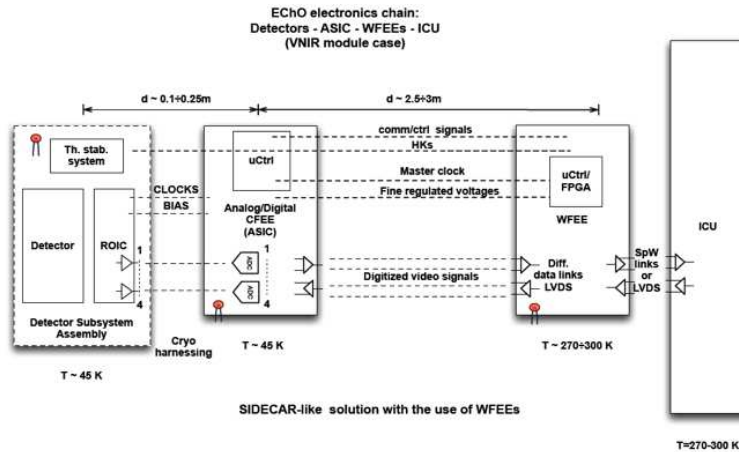


Fig. 4 EChO payload overall electrical architecture (baseline solution with SIDECAR ASIC and WFEE).

SIDECAR standard version has 36 analog input channels, and digitisation can be done with 12 or 16 bit resolution. SIDECAR presents all-digital interface to the external world, providing the following advantages to system design:

- Simplifies the overall system architecture and reduces the number of wires within the system;
- Eliminates the risks and problems of transmitting low-noise analog signals over long distances;
- Offers high flexibility and redundancy due to broad programmability;
- Digitises 16-bit data at 500 kHz (per port) or 12-bit data at up to 10 MHz (per port) for a maximum total of 12-bit pixel rate at 160 MHz.

Fig. 5 shows a schematic electrical diagram of the SIDECAR ASIC and its interfaces with the H2RG detector (i.e. ROIC multiplexer) and the host (external) electronics. A new version of SIDECAR ASIC has been recently designed by Teledyne [16]. The EChO Consortium will evaluate this new product during Phase B in both its I/F configurations with 37 pins microD connector and 91 pins nanoD Airborn connector, if available.

The overall power consumption of a system composed by a H2RG detector read-out by a SIDECAR ASIC by means of four 16 bit ADCs (4 channels) at a frequency of 100 kHz is measured to be less than 10 mW [17], [18]. The detectors FPAs +

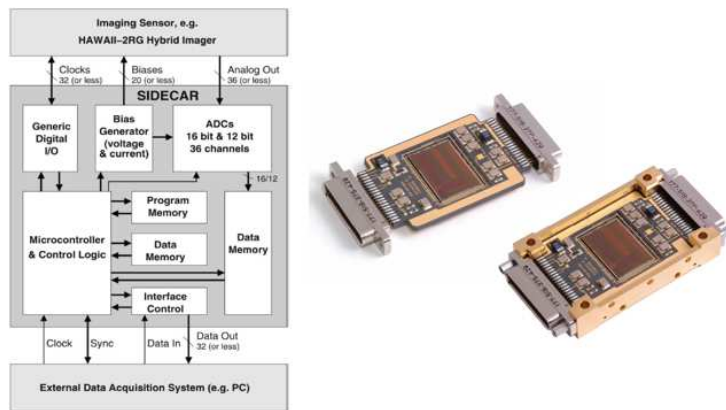


Fig. 5 Left: SIDECAR electronics block diagram. Right: JWST flight package: ceramic circuit board with ASIC die and passive components, shown without and with metal housing. The dimensions are about $74 \times 38 \times 10.4 \text{ mm}^3$. Courtesy Teledyne.

CFEES overall power dissipation allocation is a function of wavelength in order to limit the total thermal load from cold module to $< 75 \div 80 \text{ mW}$ for the VNIR, $< 25 \div 30 \text{ mW}$ for the SWIR and $< 15 \div 20 \text{ mW}$ for the MWIR one. These values will include dissipation from the single detector and its thermal stabilisation electronics, CFEE, parasitic loads (conductive and radiative) and all other loads caused directly by the cold-part modules. An alternative design for the payload electronics has been proposed in which the SIDECAR ASICs are directly interfaced the ICU, negating the need for the WFEEs. This architectural change will be studied in more detail in EChO project Definition Phase (Phase B) and finalised before the SRR (System Requirements Review).

Alternative configuration. The CFEEs alternative solution adopts the SRON CFEE ASIC (Fig. 6). It hosts up to 4 A/D converters at 16 bits outputs with input VGA (Variable Gain Amplifiers) able to perform offset and gain corrections on the video input signal and at least an externally DAC-controlled fine bias generator, as baseline, to feed the detectors ROICs. A/D converters outputs are differentially interfaced (LVDS) to WFEEs to remove the common mode residual noise.

In order to prevent from and minimising all the likely conductive thermal leakages between the detectors and the CFEEs stages operating at a ΔT of about $10 \div 15 \text{ K}$, the FPAs and the CFEEs shall be electrically connected by harnessing ranging from few cm to about 50 cm. The increasing distance between units could represent a potential issue for pixels clocking and video signal driving from the detectors outputs to the CFEEs, likely requiring an intermediate current buffering stage between the two units, especially when operating the detector at high readout frequencies. This solution would also increment the overall module electrical and electronics complexity leading to a revised basic solution adopting more than two outputs to operate the detectors (e.g. the VNIR channel one) in a low speed mode (below 500 kpx/s

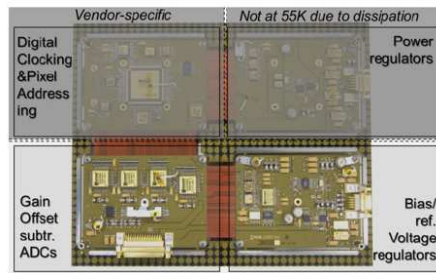


Fig. 6 Functions implemented in the SRON ASIC are Gain offset subtraction and A/D conversion as well as bias and voltage regulation. Clocking, addressing and power regulation will not be done by this unit but inside the WFEE FPGA (courtesy SRON).

@ 16 bits/px) to limit power consumption/dissipation and electrical noise. The final adopted solution with the SRON ASIC should be a compromise between available budgets and the chosen sampling frequency to meet the scientific requirements.

2.3 Fine Guidance System (FGS)

The main task of the FGS is to ensure the centering, focusing and guiding of the satellite, but it will also provide high precision astrometry and photometry of the target for complementary science. In particular, the data from the FGS will be used for de-trending to aid in the data analysis on ground [19].

The FGS optical module is designed for a 20 arcsec square field of view using 50% of the flux of the target star below $1.0 \mu\text{m}$ wavelength. The optical module provides for internal cold redundancy of the detector chain through the use of an internal 50%/50% beam-splitter and two independent detector channels with their own cold and warm drive electronics.

A consortium designed FGS Control Electronics (FCE) unit provides the control and processing of the FGS data and deliver centroid information to the S/C AOCS. The assessment of the FGS accuracy for the faintest target goal star defined for EChO (considering the effective collecting area of the telescope, efficiency parameters of optical elements, beam splitter and QE of the detector) lead to a photoelectrons count of more than 10^4 per second. Combined with a pixel scale of 0.1 arcsec and an FWHM of $2 \div 3$ pixels, the centroiding accuracy will be less than 0.1 pixel or better than 10 milliarcsecs, well in line with the required precision (PDE - Pointing Drift Error of 20 milliarcsecs -1σ - over a period of 90 s to 10 hours).

2.4 Warm Front End Electronics (WFEEs)

WFEEs are equipped with digital LVDS transceivers to communicate with CFEEs (to send/receive digital commands and collect digitised data) and host a digital logic (mainly an FPGA and/or a microcontroller) to produce command and control signals

and digital clocks to manage the detectors ROICs and CFEEs (mainly the Master Clock and Sync signals for the SIDECAR ASICs).

In the baseline design A/D conversion will be performed on board the CFEEs ASIC as well as detector clocking, wave shaping and filtering. The acquired spectra pre-processing (e.g. digital masking and image cropping) will be implemented on board the WFEEs by means of a suitable FPGA (Fig. 7), as a support to the ICU processing.

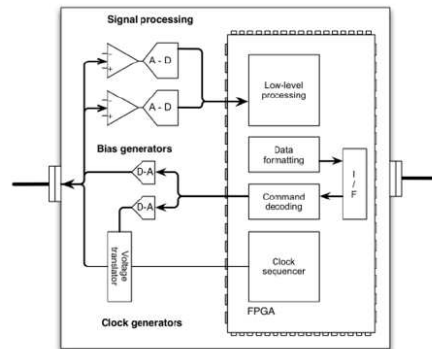


Fig. 7 Warm Front End electronics block diagram. The scheme is referred to one channel only.

WFEEs also generate precise secondary voltage levels to feed the CFEEs electronics, which, in turn, produce fine-regulated biases for the detectors FPA assemblies. Also analog housekeeping A/D conversion is performed on board WFEEs before sending digitised values to the ICU, where monitoring and packetisation will take place.

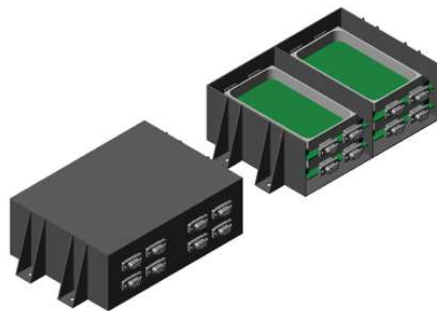


Fig. 8 WFEEs mechanical design (the number of connectors and their location are only indicative and will be better defined and fixed in the next mission phases).

Description	Basic	Nominal (20% cont.)	Margin
Power	< 18 W	< 21.6 W	< 2.4 W
Mass	3.5 kg	4.2 kg	Tot. electr. < 25 kg
Volume	224 x 164 x 80 mm ³	-	26 x 76 x 100 mm ³

Fig. 9 WFEEs box mass and volume budgets (for four WFEEs units) with an estimate of the power consumption.

WFEEs shall be connected to the ICU by means of a nominal plus a redundant SpW link or a LVDS I/F. These interfaces will be implemented by means of IP cores inside the FPGA (e.g. RTAX1000 rad-tolerant device from Actel). The preliminary design for the WFEE electronics boards (FGS excluded) mechanical accommodation is represented in Fig. 8. The aluminium alloy box dimensions are 224x164x80 mm³.

The preliminary WFEEs box mass and volume budgets (for four WFEEs units) are reported in Fig. 9 with an estimate of the power consumption. The provided overall dimensions are not taking into account the box mounting feet.

3 The Instrument Control Unit

The EChO payload electrical architecture is designed to simplify the interfaces between the integrated spectrometer and the spacecraft and to suitably perform the required on-board scientific-data digital processing and proper instrument management. As described in the previous section, a single Instrument Control Unit is foreseen, implementing all payload instruments control functions and all detectors digital signals acquisition and processing.

3.1 ICU architecture

In the EChO ICU block diagram reported in Fig. 10 the main ICU functional blocks and their interfaces are shown.

The cold proximity electronics are interfaced to the detectors ROICs bonded to the MCT sensors arrays in the VNIR, SWIR, MWIR and LWIR modules (the latter hosts a Si:As detector as baseline). These proximities and the detectors thermal control modules shall provide the buffered analogue HKs (temperatures, voltages and currents) to the warm front-end electronics and ICU, where multiplexing and HKs analogue to digital conversion will take place.

The proposed payload architecture has been designed to minimise and simplify the number of interfaces. In particular, the ICU will be the main payload interface with the spacecraft Power Conditioning and Distribution Unit (PCDU) and the On-Board Computer (OBC) and Solid State Mass Memory (SSMM) (ref. EChO EID-A ESA document).

ICU is mainly a digital unit with processing and data buffering capabilities interfacing both the spacecraft electronics and the digital section of the payload warm

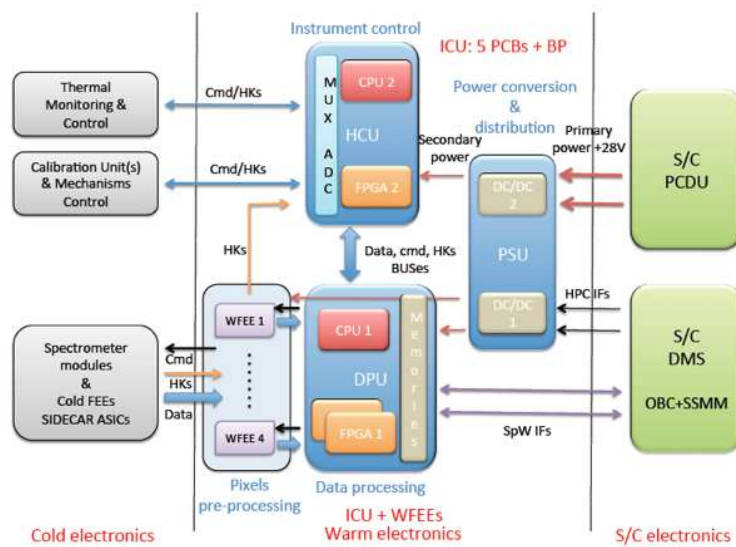


Fig. 10 EChO ICU architecture block diagram (baseline solution).

front-end electronics for commanding, data and housekeepings (HKs) acquisition, A/D conversion and dispatching, data packetisation and spectra pre-processing, as well as providing finely regulated voltage levels to all its subsystems and FEEs.

Cold front-end electronics ASICs send digitised data and analog HKs to WFEEs for packetisation in CCSDS format before sending them to the ICU by means of N+R Spacewire (SpW) or, alternatively, LVDS links. A Data Processing Unit (DPU), a HK and Calibration source management Unit (HCU) and a Power Supply Unit (PSU) are the main blocks of the ICU. The currently adopted ICU architecture interfaces 3+1 warm front-end electronics (1 optional module for LWIR) communicating with an on-board ICU digital subsystem with processing capabilities, the Data Processing Unit (DPU) and the Housekeeping and Calibration source management Unit (HCU) both based (as baseline) on a rad-hard space qualified processor and devoted, respectively, to the Data Processing Function and to the Instrument Control Function. Both processors (CPUs) run the main Application SW suitably designed to perform separately the two functions, to manage the payload operating modes (instrument managing) and the overall data acquisition procedures and processing. The modularity of this design, in which the data processing and instrument control sub-units are well separated will allow for the possibility to have different providers for the sub-units and will ease the integration and test activities at ICU level.

DPU and HCU. The data processing function at pixel level is supported by two rad-hard FPGAs working @ 80 MHz (assumed frequency for the processing resources evaluation) acting as co-processors to perform on-board (HW implemented functions) pixel-based data processing procedures.

The DPU will implement the digital data processing, the data storage and packetisation, the telemetry and telecommand packets handling and the clock/synchronisation capability to temporally correlate the scientific data coming from the different spectrometer channels.

As baseline, DPU is composed by a processing board hosting the scientific digital data processing CPU and the two ancillary FPGAs working as a co-processors and a memory board (or section) hosting all the memories needed to load and run the Application SW (PROMs, EEPROMs and SRAMs) and buffer the incoming scientific data (SDRAMs or FLASH memories) prior digital processing and data formatting. Memories addressing functions are performed by one of the two FPGAs that also act as a memory controller for data buffering.

DPU and HCU will host and share an internal PCI interface to the PCI bus including data, address and control buses. Alternatively an AMBA bus could be used. The PCI bus is connected to the rad-hard processors (an ITAR-free LEON2 AT697F and a LEON3 from ATMEL running at 60 MHz were considered, as baseline, to evaluate the processing and instrument control power needs) and to the main digital logics hosting a PCI I/F (AMBA I/F).

ICU manages both processors and logics to perform all the required tasks as digital processing (pixels sum, average, digital binning, windowing, spectra cropping and masking, pixels deglitching -if needed-, data and HKs compression) and memory management.

PSU. A Power Supply Unit (PSU) distributes the secondary voltages to the instrument subsystems by means of rad-hard DC/DC converters whereas the HCU will provide instrument/channel thermal control, calibration sources (the common Calibration Unit represented by the integrating sphere on the IOB and the calibration source owing to the VNIR module), mechanisms (the refocusing mirror and the steering mirror if included) and HKs management.

PSU will be feed by two (N+R) +28V power interfaces and will be equipped with two (N+R) BSMs (Bi-Levels Switch Monitors) to report to the S/C the unit status (switched ON/OFF) as defined by two Main (ON/OFF) plus two Redundant (ON/OFF) High Voltage - High Power Pulse Commands (HV-HPC) with interface characteristics as defined by ECSS standards.

DC/DC converters are hosted by two boards of the PSU in order to feed all the ICU subsystems and provide the basic voltage levels to the WFEEs, so the present ICU design foresees as baseline 5 Extended Double Eurocard (233.4 mm x 220 mm) electronic boards in a fully redundant architecture aboard the same PCBs in a cold strapped configuration exploiting the ICU back panel board interfacing all the electronics subsystems.

The ICU redundancy policy is based on a trade-off solution removing or reducing to an allowed level the impact of any single-point failure thanks to its cross-strapped fully cold-redundant architecture. The two DC/DC boards, as baseline, are separately used in a cold-spare redundancy scheme.

The ICU power, mass and volume budgets are reported in Fig. 11. The presented overall dimensions are not considering the box mounting feet.

Description	Basic	Nominal (20% cont.)	Margin
Power	20 W	24 W	0
Mass	7.5 kg	9 kg	Tot. electr. < 25 kg
Volume	250 x 240 x 150 mm ³	-	0 x 0 x 30 mm ³

Fig. 11 ICU power, mass and volume budgets.

3.2 Electrical IFs to the Spacecraft

The ICU is interfaced to the SVM OBC and SSMM through a +28V power line (Nominal + Redundant), two discrete high voltage - high-power command lines HV-HPC (N+R) for switching on/off the unit and a (N+R) SpaceWire (SpW) interface for commanding, HKs and data transfer to the OBC, configured to work at 10 Mbps (see Figs. 12 and 13). The SpW interfaces are implemented inside the DPU service logic FPGA as an IP core that, in turn, is bridged to the PCI bus or the AMBA bus. The same FPGA or a dedicated FPGA controls also the Buffer Memory section used to store data for digital processing and as a temporarily buffer before sending them to the OBC.

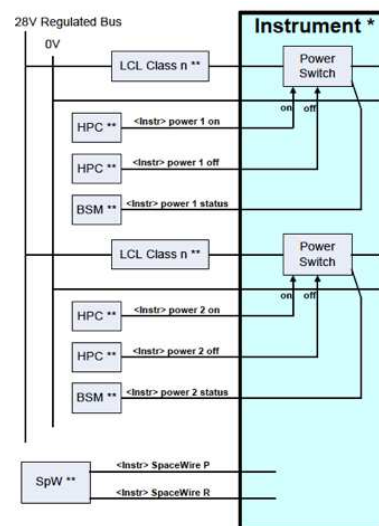


Fig. 12 Electrical IFs between SVM and the instrument.

In Table 1 the power supply and control lines presently assumed for the EChO payload electronics are indicated.

Finally, an additional MIL1553 BUS use is under evaluation and could be exploited at payload level e.g. to interface the Fine Guidance System to the S/C.

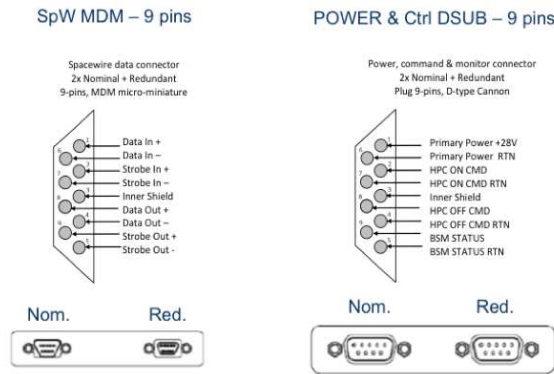


Fig. 13 TM/TC communications IFs and Power IFs.

Table 1 ICU Power supply and control lines (a cold redundancy is assumed).

Line type	From/To	Nom. and/or Red.
Power line: 28V + RTN	(From S/C PCDU to ICU)	N+R
Switch On HPC (Signal + RTN)	(From S/C DMS to ICU)	N+R
Switch Off HPC (Signal + RTN)	(From S/C DMS to ICU)	N+R
Switch Status BSM (Signal + RTN)	(From S/C DMS to ICU)	N+R

3.3 Electrical IFs to WFEEs

Electrical IFs to the WFEEs are implemented by a nominal and a redundant SpW link (or an alternative LVDS serial link) for every module in order to transmit digital data and HKs telemetry and telecommands. The possibility to use additional analog links to transmit to ICU analog HKs to be multiplexed and digitised by the HCU unit is currently being taken into consideration. Their implementation is subordinated to the final design of the WFEEs and to the final definition of their monitoring needs.

3.4 Grounding, Isolation, Bonding and Charging Control

The present EChO ICU grounding concept is a Distributed Single Point Grounding (DSPG), see Fig. 14, involving all the 5 ICU electronics boards.

The principle is to realise a single point ground for each independent power network and provide isolation between those networks. In order to match this goal, any primary power and return input lead of equipment shall have a DC isolation of at least 1 MOhm (shunted by no more than 50 nF) to equipment chassis and between power input lead and secondary power leads. In order to avoid grounding loops, secondary power distributed inside the equipment shall be galvanically insulated and decoupled by DC/DC converters.

The ICU box will be bonded to the platform bench via its mounting feet. In addition, the unit shall provide a bonding stud/hole for bonding via a bond strap. All

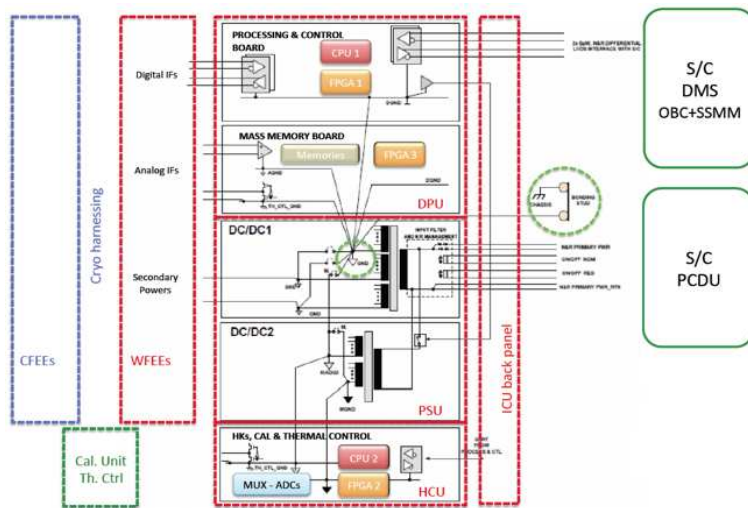


Fig. 14 ICU grounding concept.

sensible surfaces will be treated to be electrically conductive, in order to mitigate and control charge accumulation phenomena.

This concept will be revised to guarantee the compatibility with the overall spacecraft grounding scheme, as soon as the spacecraft SVM design will be finalised by the prime contractor.

3.5 Mechanical design

The ICU preliminary mechanical design is presented in Fig. 15. The ICU box dimensions are $250 \times 240 \times 150 \text{ mm}^3$, mounting brackets and feet excluded. All the electronics boards are fixed by means of space qualified card lock retainers and are reinforced by an aluminium structure hosting the connectors as depicted in the figure.

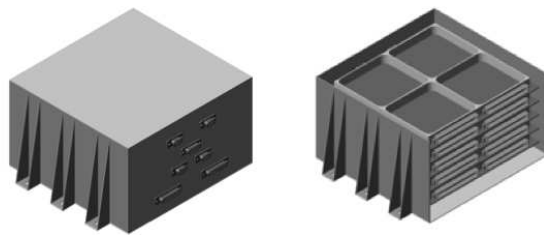


Fig. 15 ICU mechanical design (the number of connectors and their location are only indicative and will be better defined and fixed in the next mission phases).

The ICU box, made by aluminium alloy, will have an external bonding stud to connect analog and digital grounds to the unit chassis, in order to implement an alternative configuration for testing and external noise shielding.

3.6 Thermal design

The present ICU thermal design is based on a simple radiative and conductive heat transfer analysis performed on similar units, that lead to the overall thermal load dissipation to maintain all the electrical components in their operational and survival ranges and will be refined during the Definition Study (Phase B) of the project. Thermal straps could be foreseen inside the unit to manage properly heat flows between the hottest components and the ICU chassis.

3.7 Harnessing

ICU IFs harnesses will be divided into EMC classes. All cabling will have an overall screen to provide an EMC shield against radiated emissions and susceptibility and to avoid charging of the cabling dielectric materials. No flying harness is foreseen -as baseline- inside the ICU. No harness dielectric will be directly exposed to space plasma environment.

Cryogenic harnessing from WFEEs to CFEEs is presently under study and its definition requires a close collaboration between the System Team and the Science Team as the speed of acquisition and detectors driving signals have an important impact on the cable design in terms of wire size, electrical properties, shielding configuration etc. All these requirements will then be evaluated in terms of heat leak between thermal stages and, if needed, the design tuned to meet heat load allocations and electrical requirements. At this stage of the study the analysis can be based only on a series of assumptions that shall be reviewed in the next phases of the project [20].

It is clear from a first quick evaluation that typical standard flat cables or flexi-harness used in such applications (AWG26 37 pins or AWG30 91 pins) based purely on Cu are not a viable solution due to the high parasitic loads that they induce on the stages w.r.t. the allocations on the S/C. Custom made harness in terms of materials, AWG, and shielding, based on standard connectors, shall be required for EChO.

At this stage of analysis the material combination that best suits the EChO set of requirements from both the electrical and thermal point of view are the following:

- CuZn (Brass) for bias control and power supply (the expected voltages/currents should be low enough to avoid, for the moment, Cu wires);
- PCuSn (Phosphorous Bronze) and/or stainless steel (SS) for analog and digital I/O and all other signals;
- SS (Stainless Steel) braid for cable shielding.

The baseline harnessing between cold and warm electronics is presently considered as a standard round bundle cable configuration (flat cable is assumed only for the connection between Sidecars and detectors and vendor-provided).

4 Electronics simulators

The experience gained during the preparation of the Herschel [21] and Euclid [22] satellites instruments has shown the great importance of having subsystem simulators as soon as possible during SW development. The electronics simulators are intended to provide an independent functional platform for testing and simulations. They allow to test the communication protocols, data packetisation, implementation of autonomy functions; without good simulators, all these test activities have to be postponed after the AIV phase with high risk of delay due to the need to correct bugs found in the SW. They can also provide useful data and metrics to analyse and monitor sensors, FEEs electronics and ICU performance.

The present simulator, used as an early testing environment, provides TM and HKs acquisition and is virtually controlling two emulated devices retrieving randomly generated data.

The development of the simulator is based on a FPGA, which manages all house-keepings, telecommands and telemetry data. All the acquired information is sent to a computer via Ethernet connection for further analysis. The board containing the core of the simulator is GR-XC6S, manufactured by Pender Electronics. The FPGA model is a Xilinx Spartan-6 XC6SLX75.

ICU simulator consists of four modules: one for H/W interfaces and the three remaining ones make up the S/W architecture (simulation, control and monitoring and user interfacing). From this point of view, the system simulation is running the ICU components loaded and provided by the control module, which is also in charge of stand-alone monitoring of every parameter of the system and its operated through the user interface, providing the user with the whole needed functionality for practical operation, configuration and inspection of the simulation system.

The FPGA integrates an IP core of LEON3 processor. The simulator application running on the development board is coded in C++ and controlled by RTEMS, a fully featured and open-source real-time operating system widely used in embedded platforms.

The software architecture is based on two main components, Device Manager and HK Manager, controlling Device data acquisition and HKs sensor sampling, respectively. Everything is coordinated by a Core component, in charge of TC reception and TM retrieving, and responsible for communication between managers and users.

For the following Definition phase the use of a TSIM LEON3 SW simulator from Aeroflex Gaisler is also foreseen, in order to simulate the main processing tasks of the ICU. This will allow to split the SW and HW functionalities simulations and to cross-check all the results from simulations.

5 ICU software

The EChO Payload instruments On Board Software (P-OBS) running on the ICU will be composed by the following main blocks:

- *Boot Software*: it is installed in the PROMs of ICU boards and allows for loading the ICU application software (ASW) from EEPROM to RAM at boot. It contains all the low level drivers for the CPU board and its related interfaces.
- *Instrument Control Software*: it refers to the software performing the operations of the EChO scientific payload. It implements the data-handling functions of the payload and calibration sources and mechanisms (if present), manages the spectrometers operating modes and runs autonomous function. It implements the interface layer between the S/C and the instruments operation.
- *Data processing Software*: implements the ICU science data on-board processing and lossless compression (i.e. RICE). It also implements the data packetisation for the transmission to the S/C Solid State Mass Memory (SSMM).

5.1 EChO On-Board Software functional analysis

The ICU is responsible for the following main activities:

1. Telemetry and Telecommand exchange with the S/C CDMU;
2. Instrument Commanding, based on the received and interpreted TCs;
3. Instrument monitoring and control, based on the Housekeeping data (HKs) acquired from the focal plane instrument units;
4. Synchronisation of all the scientific payload activities;
5. Detectors readout data acquisition, pre-processing and formatting according to the selected Telemetry protocol;
6. Science Data download towards the S/C Mass Memory.

These activities can be grouped into the Instrument Control and Data Processing software: these two SWs will constitute the On Board Software (OBS) of the EChO science payload (P-OBS). The On Board Software will be implemented as a real-time multitask application. The Block Diagram reported in Fig. 16 is a general purpose functional diagram which is applicable to a generic space instrument control and processing software and therefore well represents the main ICU functional architecture. The two different colours indicate the different groups of functionalities of the Instrument Control and the Data Processing software.

5.2 Software layers

The EChO Payload instruments On Board Software layers structure is presented in Fig. 17. The boot software component refers to the start up software described in the previous section: it is installed in the PROMs of the ICU boards and allows for the application software loading. It contains all the low level drivers for the CPU and its related interfaces.

The physical layer includes all ICU HW components with a direct level of interaction with the on board software.

The Runtime environment includes the Real Time Operating System (RTOS) layer, necessary to provide multi-tasking support. In case the baseline architecture

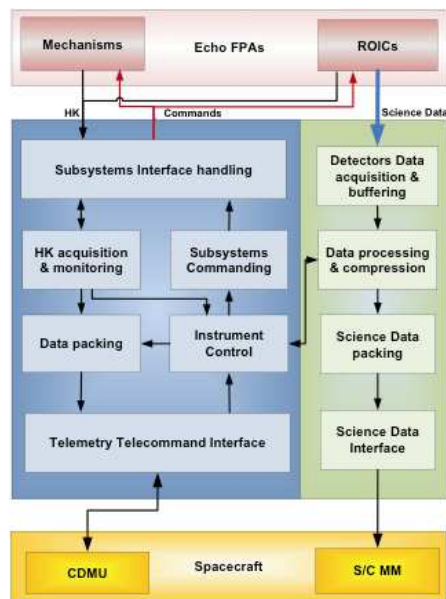


Fig. 16 ICU OBS functional components block diagram.

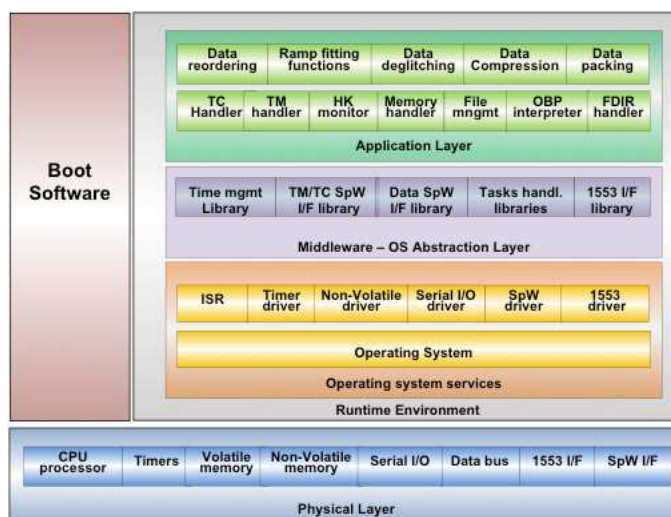


Fig. 17 SW layers structure of the EChO Payload instruments On Board Software.

based on the LEON processor will be confirmed, the RTEMS operating system is a good RTOS candidate, being already used for applications on board ESA satellites. The other indicated operating system services include the drivers for the on-board memories, the on-board HW timers and the local data bus. The other OS services

mentioned in the structure of Fig. 17 are those not directly provided with the OS kernel. An OS abstraction layer has then been included, in which all middleware libraries have been considered. The middleware services are based on the use of RTOS function calls. They include all library functions dedicated to the low level handling of the ICU HW devices/interfaces. All the middleware libraries will be developed in house and will provide a mean for developing an Application Software virtually independent from the HW and OS below it. This layer is very important and will ease the testing activities.

The Application Layer includes both the ICU Instrument Control software and the Data Processing software. The ICU Instrument Control SW will implement the functions listed in points from 1 to 4 of the list in sec. 5.1: i.e. the TM/TC S/C interface handling, the payload housekeeping data acquisition and monitoring, the instruments operating modes management and the autonomous function execution. The present assumption is that the application software will be written in C++, though some functions may need to be coded in assembly to optimise their performance.

In case stringent timing requirements have to be met for subsystem commanding, an interrupt-driven command sequencer (On Board procedures, OBP interpreter) can be included into the ICU on board software. Based on the experience of Herschels HIFI and SPIRE instrument control software, this is a flexible and effective solution to implement time-critical commanding procedures. Some preliminary tests on the performances of a simplified implementation of such a sequencer on a LEON 3 based SOC implemented on an FPGA development board (GR-XC3S-1500) have been already carried out. A 1 MHz timer has been used to trigger the highest priority interrupt of the system. Under normal workload conditions (only two tasks running, CPU load < 50%), an average time jitter of the order of 1 μ s (for an overall test duration of more than 1 hour) has been measured, as expected. The proposed sequencer offers high flexibility and re-programmability possibilities, thanks to the straightforward way in which scripts can be reloaded during in-flight operation; this feature can be exploited to modify instrument control or measurement procedures in response to changed mission requirements. The sequencer is described in [26] and [27].

5.3 Boot SW

The boot software is stored in a PROM device, while EEPROM memory devices are used to store two or more images of the Application Software (On Board Software, OBS). The boot software is started automatically after the power on. The boot program is in charge of loading and starting the application program (OBS). The boot process is driven by command packets coming from the Spacecraft. The boot SW will be able to load and start:

- one of the OBS images stored in EEPROM (when the boot from EEPROM command is received);
- an OBS image received by means of specific commands; in particular, a series of memory management commands (memory load) are used to store in RAM a complete new OBS image, which is then started at the reception of a boot from RAM command.

The boot procedure described above offers good reliability arguments because:

1. If the EEPROM is corrupted, the boot can still load an OBS image via Memory Load commands.
2. If any RAM cells in the area to be occupied by the OBS are broken, a new OBS image, which does not use that memory location, can be built on ground and uploaded via telecommands.
3. Such an approach has been successfully proven during the Herschel in-flight operations.

Of course there still remains the risk of a broken cell in PROM or in the portion of RAM used by the boot SW, which can lead to unrecoverable failures of the boot process. The drawbacks of this procedure are:

1. Complex Boot program, it needs to handle the exchange of SpW packets (even if only a very limited set of packets is to be supported);
2. Big code size, it may be challenging to fit it into PROM device.

5.4 Data processing

Fig. 18 reports the expected ICU daily data volume, the data rates to the S/C, the CPUs expected processing power and memories usage. The followings assumptions have been taken into account: the averaged number of clock cycles/elementary operation is 3 (1 MIPS = 3 Mega clock cycles); the number of elementary operations/pixel takes into account the OS background activity overhead; digital data are stored in memory (SRAM and SDRAM/FLASH) before CPU processing; masking is performed by an FPGA aboard WFEEs before sending data to the CPU; payload control refers to TC execution activity between ICU and the (3+1)-modules instrument including calibration units management. Once pre-processed, scientific data are temporarily buffered and then sent to the DMS Solid State Mass Memory.

Our basic assumption is that we sample up-the-ramp pixels in a non-destructive manner with a sampling rate ≤ 8 Hz. There will be destructive readouts after different integration times for bright, normal and faint sources, with the length of the ramp determined either by the saturation limits of the detector for a particular target or by the expected maximum length of a ramp, estimated by taking into account the expected cosmic hits rate. This will be determined on-ground by simulations activities and in flight by dedicated calibration procedures. The sampled ramps are fitted and the pixels photocurrent extracted. These data are then processed for pixels cosmic rays deglitching, lossless compressed and transmitted to the S/C in CCSDS format according to the instruments operating Mode.

The average allocated data rate is 35 Gbits/week or 5 Gbits/day. Assuming an HK production rate of 0.2 Gbits/day, a realistic duty cycle of 85÷90% and a lossless compression ratio of 2, then spending 10% of the mission in Bright targets mode, 80% in Normal targets mode and 10% in Faint targets mode gives a data rate of 4.72 Gbits/day. All the ICU processing and buffering capabilities are presently evaluated taking into account a 50% of margin, as usually adopted at the end of the Assessment Study (Phase A) and as required by EID-A.

Scientific channel:	VIS+NIR	SWIR	MWIR-1	MWIR-2	LWIR
Detector pixels covering the spectra	512x512	1024x13	63x13	87x13	50x6
Pixel pitch (μm)	18	18	25	25	25
Binning	5x5	1x1	1x1	1x1	1x1
Digital masking	70%	100%	100%	100%	100%
# bit/pix	16	16	16	16	16
Primary rate (Hz) - Bright targets case	8	8	8	8	8
Ramp lenght (s) - Bright targets case	3	3	3	3	3
# Samples per ramp	24	24	24	24	24
Housekeepings TM (Gbit/day)	0.2				
Efficiency (R-PERF-060)	85%				
Contingency (EID-A R-2430)	50%				
Available lossless compression factor (CR)	2+2.5				
# CPUs (LEON-like running @ 60 MHz)	2 (Processing & Instrument Control)				
# FPGAs (RTAX 2000-like running @ 80 MHz)	3 (pre-process., mem. manag. and aux fnc)				
SRAM needed (MBytes)	16 (4 x 4 banks)				
SDRAM or FLASH needed (MBytes)	20				
EEPROM/PROM (MBytes) - BOOT SW, BIOS SW, ASW	8 (4 x 2 banks)				
Daily averaged data rate	< 60 kbit/s				
Peak data rate (burst mode, if needed)	< 10 Mbit/s				
Science TM (Gbit/day)	< 5				
TOT. expected daily data volume – science + HKs (Gbit/day)	< 5				

Fig. 18 ICU processing power, data rate, data volume, required amount of memories.

Note: Fig. 18 values strongly depend on data processing required for on-board (ICU) deglitching procedures, compression task and pixels pre-processing. Presently pixels deglitching operation is foreseen on-board but could be avoided given the short integration times for bright targets and the very low likelihood of cosmic rays hits on pixels [28].

5.5 On-board processing steps

The most demanding module from the point of view of digital processing is the VNIR spectrometer, which is based on a MCT panoramic detector composed by 512 x 512, 18 μm pixel pitch, on which the VNIR spectra is spread on the two detector halves. Therefore, the main design steps and the system processing needs have been mainly evaluated for this channel. The detectors pixels will be digitally binned (on-chip binning is also possible, as baseline) to produce spaxels, i.e. $N \times N$ binned pixels along the spatial and spectral dimensions ($N=5$ in the baseline VNIR design).

In order to perform on board DPU data processing and pixel deglitching from cosmic rays hitting the VNIR FPA, the two FPA halves (VIS and NIR ones) will be digitally masked and cropped. This pre-processing task will be used to reject all pixels that don't contain any useful information, reducing the overall pixels number to be processed for a factor of the order of 70% of the entire array. Digital masking and image cropping will be performed aboard WFEs FPGAs, as baseline, in order to reduce the overall DPU processing load.

The main processing steps are illustrated in Fig. 19 (mostly for the VNIR channel one, but useful also for all the other channels):

- Bias correction: an internal bias is subtracted to bring all samples to the same ground. This is necessary for later binning of the data down to spaxel resolution;
- Pixel reordering: pixels are extracted from the readout electronics output serial stream and reordered, to increase the effectiveness of the subsequent data processing steps. History and ancillary data buffers can be formed at this level;
- Saturated pixels identification, by defining a cut-off value for the upper limit of the linear region of the detectors response curve. Saturated pixels will be flagged and rejected;
- Responsivity correction, based on radiometric calibration, using an array responsivity map, will be applied if necessary;
- Spatial and spectral pixel binning to build spaxels;
- Temporal samples co-addition: depending on the ramp fitting algorithm, scans and groups have to be formed (m scans per group) if needed;
- Rejection of the data that dont satisfy the noise requirement at the beginning of the ramp, when necessary;
- Non-linearity correction: if necessary, the ramps will be linearised, even during the multi-accumulate processing);
- Progressive linear least square fit to calculate ramps slope (pixels/spaxels photocurrents);

Note: The above last four steps could be necessary to decrease readout noise to specifications. Frames in a group must be contiguous and in the number necessary to reach the required total noise performance limit after co-addition (assuming a multi-accumulation readout mode [23], [24], [25]). These processing steps must run at the spaxels readout speed. Using a fixed very simple parameterisation (to be optimised during calibration and algorithm tuning procedures on ground), it can be conveniently performed in hardware.

- Cosmic rays and other glitches identification: proper glitch detection and rejection strategies will be implemented, if necessary, with a proper algorithm still to be defined;
- Bad spaxels correction and linearisation;
- Frame generation: processed science frames created here will be received on ground;
- Frame buffering;
- Lossless Compression (compression of the data to save data volume and bandwidth);
- Packetisation according to the required TM format: all data products will be packaged;
- Storage in mass-memory (SSMM) and scheduling for transmission.

The listed steps refer to the processing of a single focal plane spectrometer. It is a standard on board processing chain, and a parallel processing of more than one instrument operating simultaneously at the focal plane shall be taken into account. Each detector HK and scientific data owing to a module shall be stored in a different

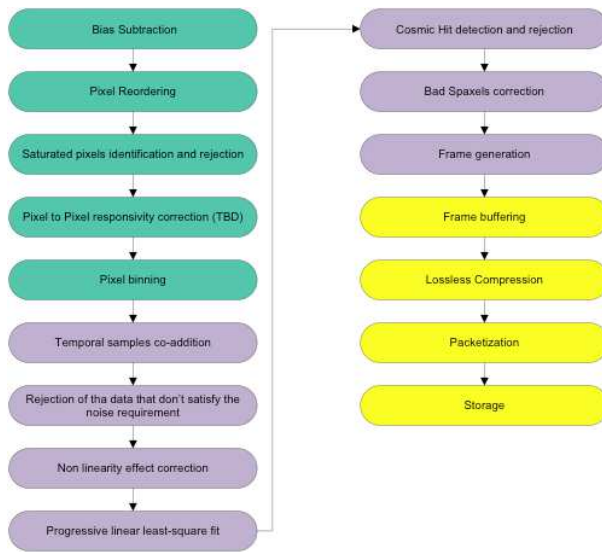


Fig. 19 Scheme of the data processing steps: green blocks refer to pixel pre-processing activities; purple blocks refer to processing steps at spaxel level and yellow blocks identify frame level processing activities.

packet store of the S/C SSMM and each payload ASW process shall be identified by a proper APID (Application Process Identifier).

The final overall processing of EChO data will be defined during Phase B and tailored for each one of the focal plane spectrometers. Dedicated simulated data flows will be used to verify the effectiveness of the data reduction steps. In particular the deglitching algorithm performances should be verified against the expected data redundancy, the data acquisition rate and the spaxels dimensions (see next section for more detailed considerations about onboard deglitching needs). Finally, the need to implement lossless compression on-board is strictly related to the results of the on-board deglitching study. If confirmed, a dedicated trade off activity to evaluate the performances of different standard lossless compression algorithms on the on-board CPU processor shall be planned.

5.6 On-board deglitching

Deglitching detectors pixels arrays from cosmic rays hits is commonly an operation to be performed at pixel-level [29], [30], [31]. Operating binning on-chip (e.g. on-board the VNIR detector ROIC) would lead to lose any pixel-based info on cosmic rays hits that would blur the spaxel integrated signal at the same time. Taking into consideration the predicted cosmic rays flux for the JWST-MIRI instrument at L2, and an integration time from 1.5 to 3 seconds for bright targets, only less than 0.02% of pixels would be interested by cosmic rays hits, so an option to be considered could be discarding any on-board deglitching operations based on pixels processing at least for bright targets.

The classical deglitching pixel-based procedure is a demanding processing task for the DPU CPU that would require the heavy use of the processor FPU (Floating Point Unit) for the second derivative calculus needed for the glitches recognition and correction. Probably it would be better to perform deglitching at spaxel level (i.e. 25 px/spaxel for the VNIR channel) by detecting cosmic rays hits and discarding them as outliers w.r.t. a median operation performed on sub-arrays. Pixels affected by cosmic rays hits should be flagged and not considered for the rest of the ramp production but properly replaced. A possibility to be explored could be to perform this kind of simplified deglitching procedure at FPGA level (HW-level).

The number of pixels belonging to a spaxel and affected by a cosmic ray hit should be determined by the hit geometry and particles energy. Most likely they would affect the detector array in the direction parallel to the optical axis and the angle defined by the optics F number and baffles, if the detector is properly shielded. So just few pixels should be interested by a single cosmic ray hit and it should be possible to operate deglitching only for the faint targets (if needed) which require longer exposition times with a bigger and not neglecting hit likelihood.

Deglitching from cosmic rays hits has surely a big impact on the overall ICU processing architecture and should be carefully evaluated in respect of the overall system budgets. Deglitching is presently foreseen at CPU level in the ICU processing needs evaluation procedure.

5.7 Data compression

Once performed pixels and spaxels on-board processing all the scientific data related to spectra will be compressed, before sending them to the S/C SSMM. Lossless data compression techniques such as zip, gzip, and winzip are widely used for compressing files residing on PCs. These techniques are all based on the Lambel-Ziv-Welch (LZW) [32] algorithm or its variations, and would generally yield poor compression ratios on data originating from spacecraft instruments.

A second well-established technique is arithmetic coding [33]. This technique works on most types of data, but exhibits relatively slow speed due to the need to update statistics along the process. The Consultative Committee on Space Data Systems (CCSDS) has adopted the extended-Rice algorithm as the recommendation for international standards for space applications [34]. This Recommendation defines a source-coding data compression algorithm and specifies how data compressed using the algorithm are inserted into source packets for retrieval and decoding.

Our present assumption is to implement a SW Rice-like lossless compression. The preliminary tests on very simple simulated spectra lead to lossless compression ratios (CR) well above the needed factor of 2. The processing time and overall performance is strictly dependent on the target CPU, see for example the results of the compression tests on the EUCLID VIS simulated images described in [26]. An activity to assess the feasibility of the lossless compression using a HW compressor is planned for the next mission phase, where the implementation of the compression algorithms at FPGA level (HW-level) in VHDL language or the use of a dedicated ASIC will be evaluated.

6 Conclusions and future developments

At the end of the Assessment Phase the baseline EChO Payload electrical architecture has been defined and a preliminary design has been provided. Some still open issues as e.g. the ICU overall processing capabilities depending mainly on the adopted on board deglitching procedures shall be addressed by further analysis. These shall take into account the mission requirements and the available budgets (thermal, mechanical and power dissipation) on a side and the overall system efficiency and reliability on the other side.

Future developments and analysis during the next phase will consider these open issues from the different perspective of the more detailed Definition Phase design.

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