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Formation Flying Metrology for the ESA-PROBA3 Mission: The Shadow Position Sensors (SPS) silicon photomultipliers (SiPMs) readout electronics

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ABSTRACT

The European Space Agency (ESA) is planning to launch in 2018 the PROBA3 Mission, designed to demonstrate the in-orbit formation flying (FF) attitude capability of its two satellites and to observe the inner part of the visible solar corona as the main scientific objective.
The solar corona will be observed thanks to the presence on the first satellite, facing the Sun, of an external occulter producing an artificial eclipse of the Sun disk. The second satellite will carry on the coronagraph telescope and the digital camera system in order to perform imaging of the inner part of the corona in visible polarized light, from 1.08 R⊙ up to about 3 R⊙.
One of the main metrological subsystems used to control and to maintain the relative (i.e. between the two satellites) and absolute (i.e. with respect to the Sun) FF attitude is the Shadow Position Sensor (SPS) assembly. It is composed of eight micro arrays of silicon photomultipliers (SiPMs) able to measure with the required sensitivity and dynamic range the penumbral light intensity on the Coronagraph entrance pupil.

In the following of the present paper we describe the overall SPS subsystem and its readout electronics with respect to the capability to satisfy the mission requirements, from the light conversion process on board the silicon-based SPS devices up to the digital signal readout and sampling.

Keywords: Solar Corona, Coronagraph, Formation Flight, In-Orbit Demonstration (IOD), Global Navigation System (GNS), Satellite attitude control, Silicon Photomultiplier (SiPM), low-noise readout electronics.

1. INTRODUCTION

The PROBA3 mission has been conceived by the ESA's Directorate of Technical and Quality management (D/TEC) exploiting the relevant part of the General Support Technology Program (GSTP) to in-orbit demonstrate, with the required accuracy, the formation flying techniques and technologies to be adopted on-board the next generation of FF satellites.
PROBA3 will host the ASPIICS (*Association of Spacecraft for Polarimetric and Imaging Investigation of the Corona of the Sun*) Coronagraph as primary payload [1, 2]. It will adopt the formation flying technique applied on the two satellites located at a distance of ~150 m to form a single giant coronagraph (Figure 1) capable of producing a nearly ideal eclipse allowing to observe the sun corona closer to the solar limb than ever before.
ASPIICS is a classical externally occulted Lyot coronagraph. The external occulter (EO) disk, hosted by the Occulter Spacecraft (OSC), blocks the light from the solar disk while the coronal light passes through the circular input pupil of the Coronagraph Optical Box (COB), located on the Coronagraph Spacecraft (CSC).

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The Coronagraph instrument optical axis will constitute the reference pointing axis on the CSC. In order to achieve the required opto-mechanical stability, ASPIICS will be mounted on an optical bench together with metrology instruments and platform attitude star trackers.

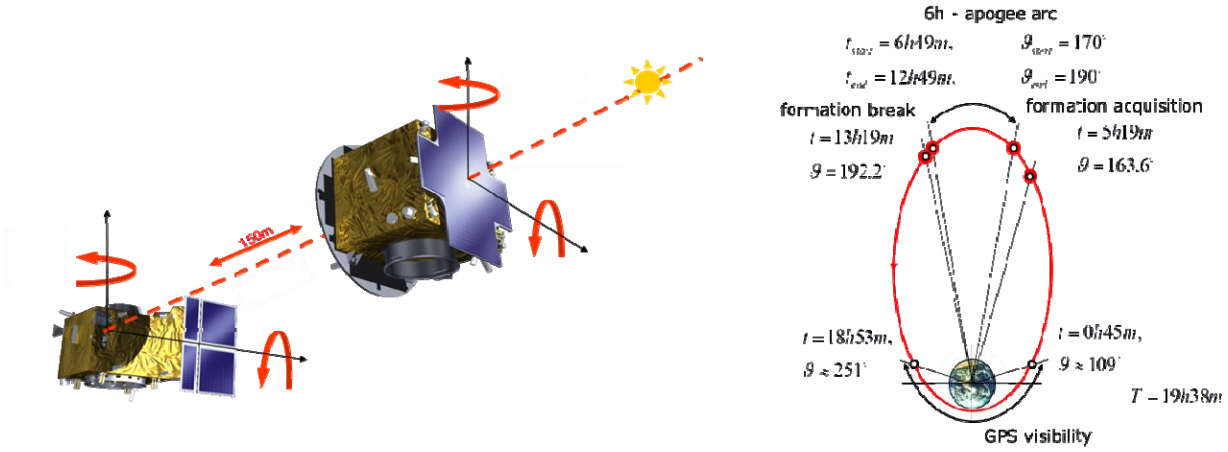

Figure 1: PROBA3 formation flying satellite overview and orbit.

The Shadow Position Sensors shall measure the absolute position of the EO disk with respect to the entrance pupil of the instrument by verifying the centering of the entrance pupil in the shadow cone of the same EO. To perform their function they are accommodated on the Coronagraph input pupil plane, hosted by a mechanical flange designed to host the SPS readout electronics up to the digitization and communication I/F stages.
ASPIICS will be the first space coronagraph to cover the range of radial distances between 1.08 and 3 solar radii where the magnetic field plays a crucial role in the coronal dynamics, thus providing continuous observational conditions very close to those during a natural total solar eclipse, but without the unwanted effects connected to the presence of the Earth's atmosphere. ASPIICS will combine observations of the corona in white light and polarization brightness with images of prominences in the He I 5876 Å or Fe XIV 5303 Å lines.
It will provide novel solar observations to achieve the two major solar physics science objectives: to understand mechanisms driving the quiescent solar corona behavior and to study physical processes that lead to coronal mass ejections (CMEs) and determine space weather as well.

2. REFERENCE FRAMES AND REQUIRED POSITIONING ACCURACIES

To reach its pre-defined scientific targets the ASPIICS coronagraph shall be operated in the nominal FF conditions, defined as follows. Assuming two spacecraft, the origins of the Payload reference coordinate frames (PLF) of each spacecraft are co-linear with some given inertial target direction vector, which may be varying in time. The line parallel to the target direction vector, which passes through the CSC PLF origin, is defined as the target line.

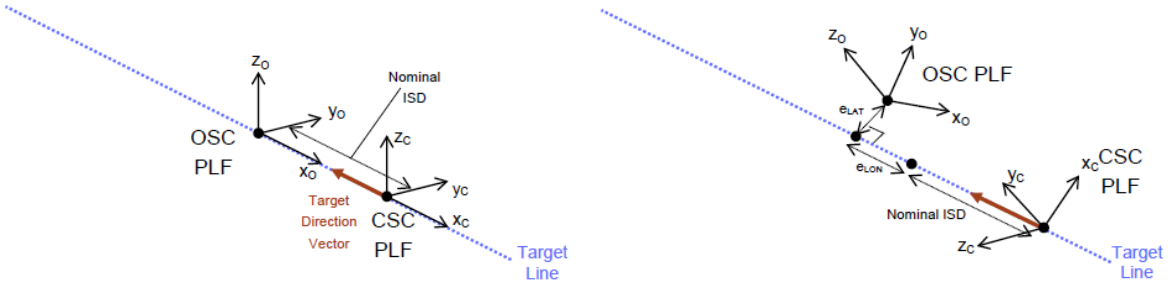

Figure 2: Nominal Formation Conditions (left) with Lateral and Longitudinal Errors shown (right).

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In nominal formation conditions, the two spacecraft PLF reference coordinate frames both have the -X axis parallel to the target line, and both spacecraft PLF reference coordinate frames are parallel with each other. The distance between the PLF origins is defined as the nominal ISD (Inter-Satellite Distance).
For PROBA3, the Coronagraph instrument aperture is the origin of the CSC PLF reference coordinate frame, which has a -X axis parallel with the instrument boresight. For the Occulter spacecraft, the PLF reference coordinate frame origin is the center of the occulting disk, and the -X axis of the reference frame is perpendicular to the plane of the disk. The Coronagraph PLF origin is also the center of the formation, and a point on the target direction vector.
For Coronagraph nominal observations, the target direction vector points from the Coronagraph PLF origin to the center of the Sun and both spacecraft PLF frames are parallel to the -X axis of the Sun Target reference coordinate frame (STF, which also fixes the roll about the target line). This condition shall be assured by the PROBA3 FF metrology subsystems, in particular by the use of the SPS assembly, once properly in-flight calibrated.
For nominal formation conditions, the *lateral position error* is defined as the perpendicular distance from the OSC PLF origin to the target line. The longitudinal position is defined as the distance between the OSC PLF origin projected on the target line to the CSC PLF origin and the *longitudinal position error* is defined as the difference between the longitudinal position and the nominal ISD.

The allowed pointing errors and required accuracies are defined and quantified by means of the two following requirements, relevant for the SPS subsystem:

"SPS performance requirement"
The Shadow Position Sensors (SPS) shall be used to verify that the Coronagraph Instrument's entrance pupil is centered within the umbra cone of the Occulter Disk. At the ISD specified in COR-IIDA-1012[1] and within +/- 10 mm of the ideal position in lateral and +/- 100 mm in range, the SPS shall have a lateral measurement accuracy of 50 μm (3σ) in each axis, and a longitudinal measurement accuracy of 1 mm (3σ). These accuracies are with respect to the axis connecting the center of the Occulter with the center of the Sun.

"SPS performance goal"
The SPS should be able to return a 3D relative position measurement at reduced performance within a range of +/- 50 mm in lateral and +/- 500 mm in longitudinal (i.e. the SPS should always return a 3D measurement within a box of 100 mm in width and height and 1000 mm in depth, centered on the ideal position).

These two fundamental requirements drive the overall SPS readout electronics design, defining the required sensitivities and dynamic ranges as well as the so-called *"requirement box"* (20 mm x 20 mm x 200 mm) and *"goal box"* (100 mm x 100 mm x 1000 mm) in which the relevant requirements shall be satisfied.
Basically, the SPS will provide information on the lateral and longitudinal position of the OSC with different accuracies. If the SPS will be able to work nominally, they will be used by the S/C GNC loop. They will have a much higher accuracy than any other metrology sensor on-board PROBA3 (estimated increasing factor of about 10^1-10^2). Therefore, the SPS cannot rely on any other metrology input to cross-calibrate and bootstrap its own computations.

3. EXPECTED PENUMBRA ILLUMINATION PROFILE ON THE INPUT PUPIL

The geometrical problem

Every point (x, y) in the penumbral region lying over the Coronagraph entrance pupil plane (SPS plane) is characterized by a level of illumination related to the fraction of the solar disk seen by the considered point, going from no illumination for the points located in the umbra (where there is no visible fraction of the solar disk) up to total illumination for the points located out of the penumbra (where the whole solar disk is visible).
For all the intermediate points located in the penumbra the amount of light impinging on the SPS sensors can be computed geometrically (i.e. without taking into account the diffraction effects produced by the OSC) by estimating the

[1] It is an ESA requirement specified in the Instrument Interface Document (IIDA - Part A) providing the adopted equation to properly compute ISD.

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fraction of the solar disk seen by each point [3]. The shape of solar disk projected on the plane where the occulter should be in the ideal case can be well approximated with a circle, while the occulter can be described by an ellipse in order to take into account possible OSC tilt angles although these can be considered negligible.
The level of illumination is also dependent on two other effects: the limb darkening effect and the presence of sunspots close to the limb. This can be understood as follows: the SPS detectors are located very close to the edge of the umbra region and the corresponding amount of light they collect is due to the electromagnetic emission coming from a thin crescent-shaped fraction of the solar disk emerging behind the occulter. This fraction of the disk is for the majority located at the solar limb, where the emission is reduced by a factor of about ~ 2.7 (Allen 2000) with respect to the emission coming from the center of the disk because of the limb darkening effect.
Hence, the level of illumination estimated in the penumbra by assuming uniform distribution of solar radiation on the disk is significantly overestimated. Moreover, when a meaningful sunspot group will be located at the limb, this will correspond to a further reduction in the illumination in the penumbra for all the points located in the entrance pupil plane seeing emission coming from the crescent-shaped fraction of the solar disk where the sunspots are located.
Because the photospheric emission coming from sunspots is reduced, respectively, down to 5-25% and 65-85% of the quiet sun photospheric light in the sunspot umbra and penumbra (Borrero & Ichimoto 2011), this will provide a further reduction in the SPS illumination depending mainly on the sunspot size and location. The limb darkening effect can be easily included in the requested algorithm, while the second effect cannot be included in our computation because it is not possible to forecast at any time the transit of a sunspot at the limb. For this reason the sunspot effect is here neglected but it should be considered once in-flight by means of follow up observation from ground.

A more realistic model, to be developed during the next project phase shall also include the diffraction effects produced by the edges of the occulting disk [4], which shall be optimized:

1. to reduce the overall amount of diffracted stray light falling inside ASPIICS input pupil;
2. to minimize the unpredictable effects of diffracted stray light as relevant uncertainty term concerning the SPS measurement accuracy.

Estimate of the SPS SiPM output currents

The solar flux or spectral irradiance F_λ [W m^{-2} nm^{-1}] is shown in Figure 3 together with the SPS responsivity [A/W].

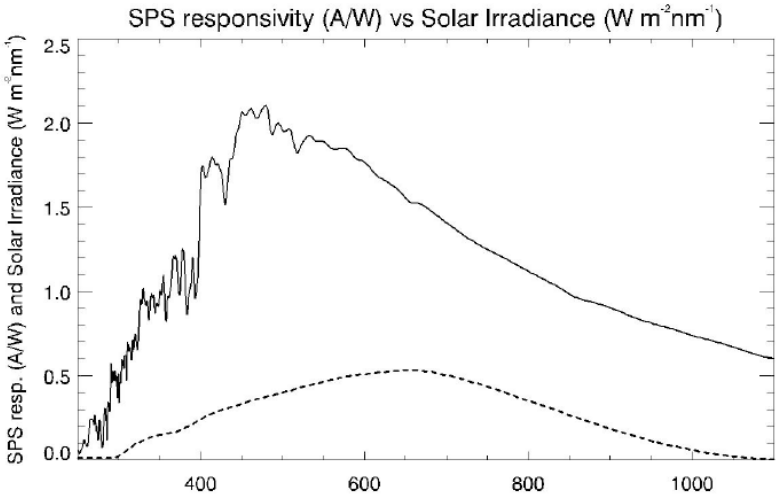

Figure 3: the solar spectral irradiance (solid line, [W m^{-2} nm^{-1}]) and the SPS responsivity curve (dashed line [A/W]).

In general the radiation emitted by the solar disk is not uniform because of the center-to-limb variations, resulting in a limb darkening in the visible range and limb brightening in the EUV range (it is a wavelength dependent effect). Hence, numerical integration is needed in order to estimate the average solar radiation coming from the fraction of the disk seen by the SPS and taking into account the limb darkening effect.

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The output current response R_{SPS} [A m^{-2}] expected by the SPS was computed [3] in the penumbra around the location of SPS on the entrance pupil plane by assuming (as a first step) that the occulter and the coronagraph spacecraft are perfectly aligned and by operating the numerical convolution between the two curves reported in Figure 3.
The illumination in the penumbra has been computed for all the three cases mentioned above and the resulting curves are shown in Figure 4. In general the inclusion of the limb darkening corresponds to a reduction by about a factor ~ 1.9 in the illumination level at the SPS location, while the presence of the sunspots induces a further decrease by about an average factor of ~1.1.

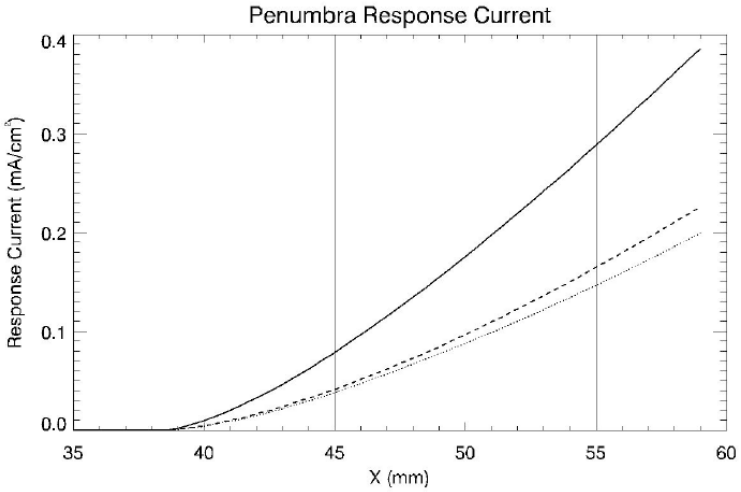

Figure 4: Level of expected SPS response current densities in the penumbra on the entrance pupil plane as a function of the distance from the telescope optical axis around the possible SPS location radii. The current is given for the three mentioned cases, i.e. by neglecting the limb darkening (solid line), including the limb darkening (dashed line) and adding to the limb darkening a sunspot located at the limb (dotted line).

4. REQUIRED SENSITIVITIES AND DYNAMIC RANGES

The expected current densities (Figure 4) and their variations within the *requirement* and *goal* boxes are different, in principle, when considering different reference locations of the SPS devices on the coronagraph input pupil plane and, to determine the best location for the SiPM sensors, we took into account:

- the main geometrical constraints concerning the *performance* and *goal* requirements and the diameter of the umbra projected by the EO on the coronagraph input pupil;
- the effects of the diffracted light profile on the pure geometrical illumination profile.

SPS location - geometrical constraints

The *performance* and *goal* requirements, along with the umbra diameter (77 mm) and the SPS physical dimensions, play a fundamental role in determining a suitable location for the SiPM devices. In particular, the minimum diameter to avoid two sensors at the same time falling inside the umbra, compromising the measurement, is 55 mm.

SPS location - diffraction constraints

As already pointed out the minimum current variation value will be different, in principle, for the two cases of geometrical and diffracted light illumination profile. In particular, in the former case, the minimum current density variation will tend to zero when approaching the umbra limit requiring an infinite sensitivity and dynamic range as well.
This consideration, along with the umbra radius value of 38.5 mm, imposes a limit for the inner circumference radius of the SPS device when considering only the geometrical illumination profile.

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It is also worth noting that the baseline SiPMs are square devices with 3 mm side (ref to Paragraph 5) and to properly assess the SPS readout electronics measurement capability with respect to a very small current density variation we should consider the convolution effect between the SPS area and the illumination profile for the smallest and generic displacement along all the directions on the input pupil plane.
This effect will be bigger and not negligible when moving the SPS towards inner locations as it could nullify the actual SPS measurement capability. In this sense it is preferable to move as much as possible the SPS devices towards outer circumferences (still taking into account the mechanical constraints as imposed by the SPS flange).
Furthermore, for outer locations, the diffraction light profile will have a reduced weight when compared to the geometrical illumination profile, which leads to an acceptable definition of the SPS sensitivity and dynamic range concepts. In this case, in fact, we would not distinguish between the two illumination profiles avoiding the uncertainties connected to the diffraction profile, still to be precisely assessed by SW simulations and laboratory tests during Phase C.

Taking into account all these constraints we decided to locate all the 8 SPS devices (4 nominal and 4 redundant) on the same circumference of 55 mm radius, equally spaced if not precluded by the PCB layout (e.g. the presence of an IF connector) or other limitations imposed by mechanics still to be designed.

SPS sensitivity and dynamic range

To determine the SPS required sensitivity and dynamic range we considered the virtual position (i.e. with respect to the umbra center) of the SPS devices when moving the illumination profile on the SPS plane for the boundaries stated in *SPS performance requirement* in order to determine the minimum required measurable current density variation for the worst case. This happens when the chosen SPS will fall in the nearest location to the umbra. The same considerations should be done to determine the maximum expected value, for the farthest location of a chosen SPS from the umbra limit.
For the identified virtual position, the minimum current density variation shall be defined as the minimum variation associated to a required displacement of 50 μm transversal or 1 mm longitudinal.
From the penumbra geometrical illumination profile study and the chosen SPS location, we derived the analog required sensitivities (basically current densities variations, being independent from the particular device or from its own area) for the requirement box as hereafter reported:

- Min **transversal** current variation: **$2.4\ 10^{-4}$ mA/cm^2** (i.e. 21.6 nA for SPS area = 9 mm^2);
- Min **longitudinal** current variation: **$2.5\ 10^{-5}$ mA/cm^2** (i.e. 2.25 nA for SPS area = 9 mm^2).

To properly sample these currents the SPS readout electronics shall adopt an overall gain able to amplify them at least twice the ADC Least Significant Bit value (the LSB analog value is given by the voltage range covered by the ADC input divided by the ADC effective resolution).

"SPS performance requirement" (requirement box)

Physical quantity	Expected value	Note
Min current density variation (mA/cm^2)	$2.4\ 10^{-4}$ transversal $2.5\ 10^{-5}$ longitudinal	50 μm transversal 1 mm longitudinal
Min current density (mA/cm^2)	$6.273\ 10^{-3}$	X= +100
Max current density (mA/cm^2)	0.4124	X= -100
Dynamic range (#)	14 bit at least 16245	Nyquist sampling 16 bit ADC

Table 1: Current densities and dynamic range requirements (with respect to the *SPS performance requirement*).

In other terms the ADC LSB shall be able to represent an input current density of about $1.2\ 10^{-4}$ mA/cm^2 (or ~10 nA, in current, for SPS with 3 mm side) for the required transversal sensitivity and $1.25\ 10^{-5}$ mA/cm^2 (or ~1 nA, in current, for

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SPS with 3 mm side)[2] for the required longitudinal sensitivity, in order to sample properly (Nyquist) the required sensitivities.
It will be care of a DAC on board the SPS PCB to remove, with the needed voltage accuracy, the bias or offset voltage at the ADC input in order to sample properly the required sensitivity and to match the needed dynamic range avoiding the use of a 16 bits ADC (refer to Table 1). As these 16 bits device have commonly 1 analog input channel it is necessary to use an analog switch to select 1 of 4 signals from the sensor amplifiers. Whilst, in theory, this solution meets the sensitivity requirement (> 14 bits, refer to Figure 5) the design would have a number of significant drawbacks.
Figure 5 shows a plot of the required sensitivity ($\mu A/cm^2$) versus the overall sensor current (mA/cm^2). The dynamic range of the sensor has been defined as the interval between 6.273 10^{-3} mA/cm^2 to 0.4124 mA/cm^2. From the same figure it can be seen that, at the low end of the range the required sensitivity is 0.025 $\mu A/cm^2$. Therefore, to achieve this sensitivity over the entire dynamic range it would require an ADC with a resolution greater than 14 bits.

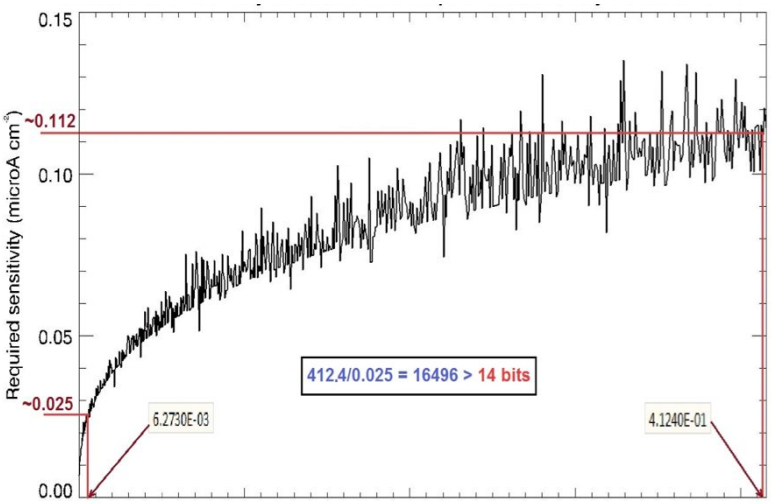

Figure 5: Required absolute ($\mu A/cm^2$) longitudinal sensitivity and dynamic range as a function of the expected currents along the requirement box for a minimum displacement of 1 mm (the minimum is found at the edge of the requirement box, i.e. @ X = +100 mm, ref. to Table 1). The noise on the curve has a numerical computation origin.

5. SPS SENSORS

Silicon photomultipliers (SiPMs)

The adopted SiPM sensors design is based on a diode array of high gain, single-photon sensitive, visible light detectors commercialized by Sensl (Cork, Ireland) [5]. They have performance characteristics similar to a conventional PMT (Photo Multiplier Tube), while benefiting from the practical advantages of solid-state technology: low operating voltage, robustness, compactness, insensitivity to magnetic fields and light over-exposure.
Each element of the array has its own quenching resistance providing stable operation when operating above the breakdown voltage. Its typical value is 360 kΩ and the typical diodes density is ~500/mm^2. In the present application SiPMs are operated in photovoltaic mode, as the quenching resistance is not known to affect their performance when operating in this mode.

[2] 1 nA is the order of magnitude of the SPS 3 mm side *intrinsic current noise* (shot + Johnson) for a SPS output bandwidth of the order of 100 Hz (transimpedance operational amplifier input bandwidth).

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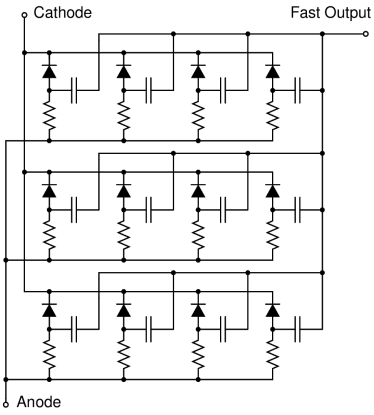

Figure 6: SPS SiPM package design.

The present design is based on a MicroSM-30035-X05 (3 mm side) product hosted inside a TO5 can (refer to Figure 7), which shall be provided with a radiation hard window transparent to visible light on a large part of the solar spectrum.

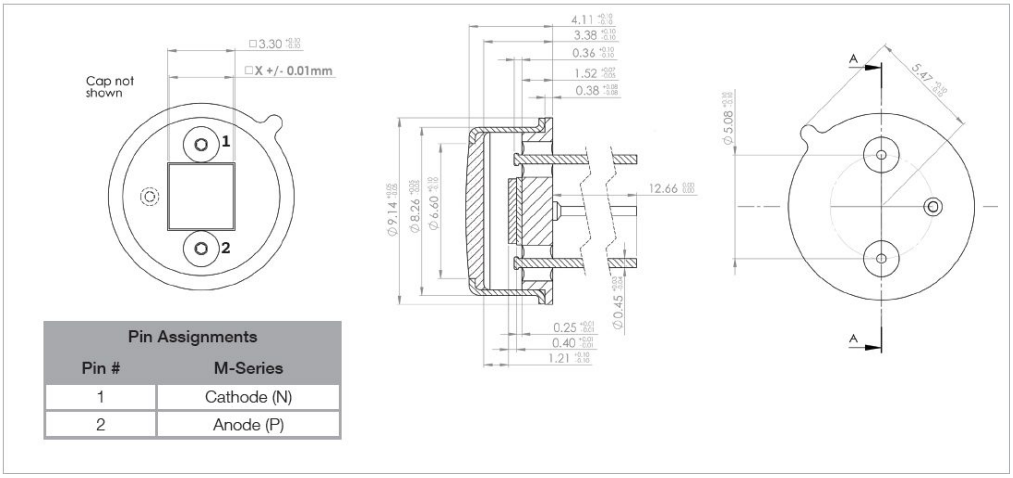

Figure 7: SPS SiPM package design.

6. SPS READOUT ELECTRONICS DESIGN

Baseline design

The present SPS readout electronics scheme foresees three amplification stages:

- A high gain transimpedance stage ($G = 10^4$);
- A first low gain (LG) amplification stage ($G \sim 10$);
- A second low gain amplification stage ($G \sim 20$), whose output benefits of the previous amplification stage and for this reason is called “high gain” (HG) output stage (refer to Figure 8).

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All the adopted gains, as well as the narrow electronics bandwidth (~10 Hz, as we are mainly facing quasi-DC signals), have been assumed for the reference design to evaluate the readout electronics design performance in terms of expected noise and, for this reason, could be fine tuned during the next design phase exploiting a breadboard for test.

The two amplification stages outputs are converted by an eight inputs 12-bits space qualified ADC (ADC128S102QML) capable to serially sampling all the low and high gain outputs (8) of a set of 4 sensors (nominal or redundant) and allowing a compact design of the electronics with a minimum signals count for the readout interface bus. The LG outputs signals are sampled with the required lower transversal sensitivity, while the HG outputs signals are sampled with the required higher longitudinal sensitivity, achievable thanks to the use of a higher gain.

One of the high gain stage opamp inputs (the inverting one) is fed by an analog voltage level provided by a 12-bits DAC to set a proper offset in order to sample the high gain output stage with the required sensitivity along the required dynamic range. The DAC digital input is set by an external FPGA providing the needed offset values as feedback from the readout of the LG stage output and avoiding in this way the use of an ADC with a higher digital resolution. This allows the signal to be readout by means of a 12-bit ADC whilst achieving an effective ADC bit range of greater than 16-bits.

A design with a 16 bits space qualified ADCs was also an option that has been discarded because these devices have several drawbacks: they commonly have one only input, a higher cost and are not very common on the market as the commercial, not qualified, equivalent devices.

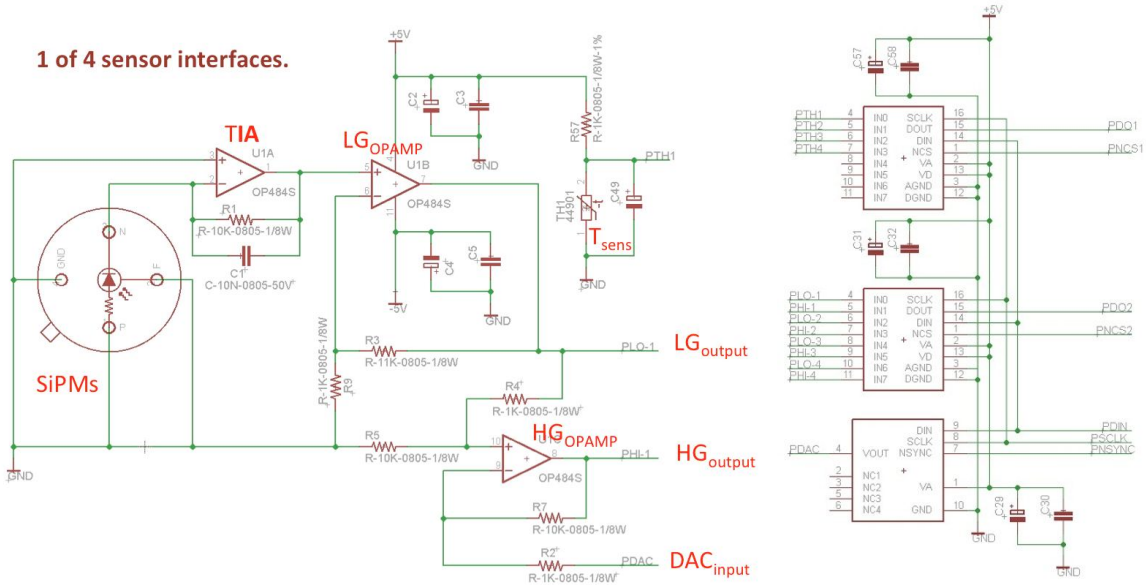

Figure 8: Baseline SPS readout electronics schematic design. Analog amplification chain (left) and A/D conversion stage (right).

PCB design

A preliminary design of the SPS PCB for a first assessment of the space needed to host all the electronics components is illustrated in Figure 9. It shows only major components, mainly mounted on the top layer. The bottom layer is presently used only to mount secondary passive components and could be used to implement transmitters and receivers as they are not yet included in the design.

A particular care shall be adopted when designing the tracks routing in order to avoid cross talk effects between analog and digital signals, potentially affecting the readout electronics noise budget. Laboratory measurements are already foreseen in order to assess the relevant contribution.

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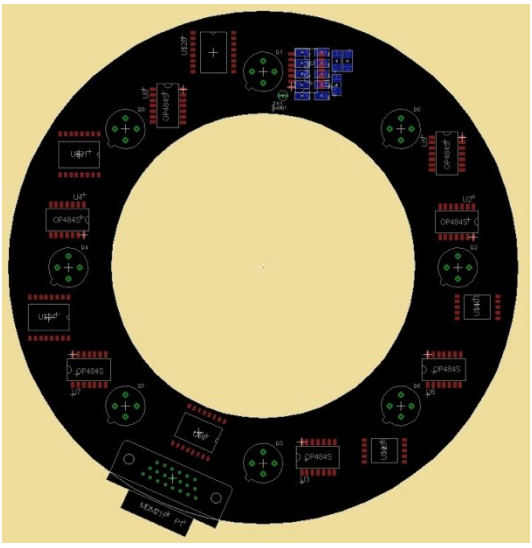

Figure 9: SPS PCB design draft.

SPS readout electronics expected performances

The overall poissonian (shot, thermal included) and readout electronic noise budget can be expressed by the following equation:

$$1. \qquad \sigma^2_{ROAD} = \sigma^2_{shot} + \sigma^2_{John} + \sigma^2_{amp} + \sigma^2_{DAC} + \sigma^2_{ADC} + \sigma^2_{cte}$$

where:

- σ^2_{shot} is the overall shot noise given by the photocurrent and the dark current produced by the adopted SiPM devices;
- σ^2_{John} is the Johnson noise term produced by the thermal noise inside the resistances R_d and R_i of the SiPM devices (refer to Figure 10).

Both these terms can be treated as analog values (voltages) at the ADC input (i.e. analog values as they would be measured at the identified noise source multiplied by the overall adopted gain from the source itself to the ADC input, taking into account the analog bandwidth stage by stage).

- σ^2_{amp} is the electronic noise of the transimpedance and following (low gain, LG, and high gain, HG) amplification stages;
- σ^2_{DAC} is the electronic noise or uncertainty introduced by the use of a DAC to remove the voltage offset and sample properly (i.e. with the required sensitivity) the required dynamic range;
- σ^2_{ADC} is the ADC conversion error in DNs due to its INL (integral non-linearity), ENOB (effective number of bits) and overall accuracy characteristics;

σ^2_{cte} is the electronic noise contribution associated to likely cross-talk effects on PCB between analog and digital components/tracks/parts (to be assessed by laboratory measurements). It will be care of a proper SPS PCB layout and signal routing design to minimize its quasi-systematic contribution.
The noise model (shot noise + Johnson noise) for the SPS sensors is represented in the following figure:

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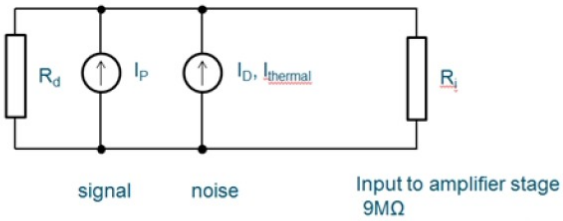

Shot noise and thermal noise make up total noise contributions:

$$I_{noise} = \sqrt{2q(I_P + I_D) + {}^{4kT}/_{R_{eq}}} \qquad \left({}^{A}/_{\sqrt{Hz}}\right)$$

Where:

$$\frac{1}{R_{eq}} = \frac{1}{R_d} + \frac{1}{R_i}$$

Figure 10: SPS sensors noise model electrical circuit (R_d ~7 GΩ).

The noise spectral density from the SPS sensors is reported in the second column of Table 2 as a function of the SiPMs devices active area (squares with sides of 1 mm, 3 mm and 6 mm). The same Table also reports the equivalent voltage noise spectral densities after the transimpedance stage (adopting G_{TIA}= 10k) and the post-amplification stage (LG opamp, $G_{LGopa->ADC}$ = 10).
In the present case (sensors noise computation) the two amplification stages (TIA and LG opamp) are considered as ideal and their intrinsic noise sources are apart considered.

	current noise from sensor (pA/√Hz)	voltage noise after TIA (μV/√Hz)	voltage noise after voltage amp (μV/√Hz)
MicroFB-10035-X18 (1mm)	34.3	0.34	3.5
MicroSB-30035-X05 (3mm)	102.9	1.03	10.4
MicroSB-60035-X08 (6mm)	205.8	2.06	20.8

	voltage noise after amp @ 10Hz	voltage noise after amp @ 1KHz	voltage noise after amp @ 1MHz
MicroFB-10035-X18 (1mm)	11.1μV	111μV	3.5mV
MicroSB-30035-X05 (3mm)	33μV	328μV	10.4mV
MicroSB-60035-X08 (6mm)	66μV	658μV	20.8mV

Table 2: SPS noise spectral densities and voltage noise for different bandwidths (10 Hz, 1 KHz, 1 MHz) at different stages of the readout electronics circuit ($G_{TIA} = 10^4$; G_{LGopa} = 10).

The first two terms of the readout electronics error budget were evaluated by the adoption of the above described model and by electrical measurements and can be considered constrained inside the adopted ADC LSB, at least when using a max bandwidth of 1 KHz and for the LG opamp output only.

Indeed all the error budget terms connected to the electronic parts shall be revised and precisely assessed during the next phase of the project. Their values shall be updated once determined the needed gains and bandwidths, stage by stage, as a further step towards a more detailed readout electronics design.
The noise budget shall consider the intrinsic noise spectral densities (SD) concerning all the amplification stages as well as the accuracy of the ADC as provided by the analog to digital conversion task. The operational amplifiers contribution to the overall variance at the ADC input will be given by:

$$\sigma^2_{amp} = \int_0^{ROE_{BW}} \left\{ \left(G^2_{TIA \to ADC}\, SD^2_{TIA}\right) + \left(G^2_{LG_{opa} \to ADC}\, SD^2_{LG_{opa}}\right) + \left(G^2_{HG_{opa} \to ADC}\, SD^2_{HG_{opa}}\right) \right\} df$$

2.

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Concerning the ADC accuracy the relevant data are reported in the following Table:

ADC used is 8-Channel, 12-bit, serial:
Commercial: ADC128S102 ENOB = 11.3 Min (Typical 11.8)
SPACE:ADC128S102QML ENOB = 11.1 Min (Typical 11.6)
ADC LSB = 5V/4096 = 1.22mV
Therefore - can assume accuracy of ADC is ± LSB = ±1.22mV
For gain of pre-amps selected such that operating light level signal near 2.5V (½ range)
Relative ADC accuracy = ±1.22mV/2.5V = ±0.05%

Table 3: ADC accuracy data.

Indeed, given the typical ENOB of the Space Qualified part, equal to 11.6 bits, the assumed ADC accuracy is given by:

$$3. \quad 5V/2^{11.6} = 1.61 \text{ mV}$$

The present readout electronics design foresees the use of a 12 bits DAC to remove an analog offset (or pedestal) from the ADC input in order to sample properly and to match the required large dynamic range. Hence each analog voltage instability or fluctuation at the ADC input shall be considered as a source of noise:

$$4. \quad \sigma^2_{DAC} = (LSB_{DAC} \text{ x } G_{HGopa->ADC})^2$$

where LSB_{DAC} is the DAC Least Significant Bit expressed as analog voltage at the HG opamp input ($DAC_{LSB} = 5V/2^{12} = 1.22$ mV).
Another source of noise to be properly assessed thanks to laboratory measurements concerns the actual presence of analog and digital components cross-talk effects, once designed the PCB layout for the signals routing (σ^2_{cte}).

The noise introduced by the overall SPS readout electronics (HG output), considering the minimum longitudinal current variation (2.25 nA) to be resolved, is given by:

$$5. \quad \sigma^2_{ROAD} = \sigma^2_{shot} + \sigma^2_{John} + \sigma^2_{amp} + \sigma^2_{DAC} + \sigma^2_{ADC} + \sigma^2_{cte}$$

Substituting their numerical values, as provided by the electronics components datasheets, we obtain:

$$6. \quad \sigma_{ROAD} > 34.7 \text{ mV}$$

and for the longitudinal actual measurement accuracy we have: 34.7 mV/4.5 mV x 1 mm = ~7.7 mm, taking into account that 4.5 mV = 2.25 nA x 2 10^6 V/A.
The noise introduced by the LG readout electronics only, considering the minimum transversal current variation (21.6 nA) to be resolved, is given by:

$$7. \quad \sigma^2_{ROAD} = \sigma^2_{shot} + \sigma^2_{John} + \sigma^2_{amp} + \sigma^2_{ADC} + \sigma^2_{cte}$$

Substituting their numerical values (from datasheets) we obtain:

$$8. \quad \sigma_{ROAD} > 2.02 \text{ mV}$$

and for the transversal actual measurement accuracy we have: 2.02 mV/2.16 mV x 50 μm = ~50 μm, taking into account that 2.16 mV = 21.6 nA x 10^5 V/A.

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It is worth noting that within the present assumptions the adopted longitudinal current sample is slightly oversampled (4.5/1.6 = 2.8) while the transversal one is slightly undersampled (2.16/1.6 = 1.35), having the effect to underestimate the transversal error.
The present readout electronics design, assuming a bandwidth of 10 Hz, is able to provide a longitudinal measurement accuracy of the order of 7.7 mm and a transversal one of the order of 50 μm, without considering the error contribution associated to analog and digital cross talk effects. These latter will be assessed once designed and realized the SPS readout electronics Development Model (DM) and Engineering Model (EM).
It is also worth noting that the readout electronics error budget does not consider other error contributions (mechanical, thermo-elastic, illumination profile, fitting algorithms etc.), so the overall error budget in terms of displacement error is expected to be bigger than the accuracy requirements for the SPS performances.
For what concerns the electronics contributions several options are going to be investigated to reduce the electronics noise.

Readout electronics uncertainties mitigation

The readout electronics noise budget is susceptible to mitigations as it represents a first assessment of the performances provided by the present design. Some actions can be undertaken as hereafter summarized:

1. TIA stage intrinsic noise: the TIA opamp intrinsic noise should be reduced as much as possible as it will be amplified, as the signal itself, along all the electronics stages up to the ADC input;
2. DAC uncertainty: it can be reduced increasing the DAC resolution or by means of a proper on-ground calibration and in flight verification of a subset (max 32) of reference voltages to be used as HG stage reference levels. Also the HG stage gain opamp should be chosen properly in order to avoid an unsustainable noise amplification;
3. Readout electronics bandwidth: it should be chosen in order to limit as much as possible the white noise contribution but respecting the needed signal spectral content and the ADC sampling frequency;
4. Opamps amplification stages: the amplification stages intrinsic noise should be limited as much as possible although its influence on the overall error budget is limited by the reduced adopted gain;
5. A proper PCB layout design and signal routing should be performed in order to limit as much as possible or to avoid A/D signals crosstalk effects.

These suitable actions can be exploited to meaningfully reduce the SPS readout electronics noise term and could lead to a compliant design with respect to the required transversal and longitudinal sensitivities.

Limitations

Limitations to the electronics design and a further reduction of the electronics noise are mainly due to the available space-qualified devices on the market and by the reduced available space inside the SPS flange for a proper PCB design as well as the unavailability of in-flight cooling the SPS PCB. These restrictions lead to choose component packages in a dual or quad configuration, hosting multiple devices and further reducing the suitable space-qualified products availability on the market.

Multiple sampling

The adopted ADC provides 8 input ports to sample the 4 LG and 4 HG operational amplifiers outputs of a SPS set. The ADC single port conversion (digitization) time is of the order of 8 μs and the SPS data are required to be sent to the On-board Data Handling system with an update rate of 2 Hz. This leave some margin to accumulate several samples and to perform an averaging operation on them, reducing the overall uncertainty of a single measurement and improving the readout process accuracy.

What we expect is that the signal to noise ratio (S/N) of a set of *n* measurements will be improved by a factor given by the square root of the number of measurement that are going to be summed, as we can write:

9. $$\frac{S}{N} = \frac{n\,f}{\sqrt{n\,(f + f_{dark} + RO^2)}} = \sqrt{n}\,\frac{f}{\sqrt{f + f_{dark} + RO^2}}$$

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where *f* is the flux collected by a single measurement, f_{dark} the equivalent flux concerning the poissonian source(s) of noise and *RO* the electronics readout noise. This prediction is going to be confirmed by preliminary laboratory measurements performed by Sensl at their premises and shall be further investigated during the next phase of the project (refer to Paragraph 7).
Considering a set of *n* measurements (*n* with a value between 128 and 512) the readout electronics accuracy could be in principle improved by at least an order of magnitude, leading to an error budget of the order of 770 µm for the longitudinal measurement accuracy and of the order of 5 µm for the transversal measurement accuracy (TBC, mainly due to the actual needed electronics bandwidth), respecting the *SPS performance requirement* and leaving some margin for the uncertainty value allocated to the other sources of noise.

LT Spice noise model

To properly assess the SPS readout electronics noise we performed some simulations using LT Spice from Linear Technology and Cadence Orcad. We found very similar results.

The adopted scheme is reported in Figure 11. The operational amplifiers models include their own sources of noise as well as all the discrete components we introduced. We explicitly excluded the digital parts (DAC and ADC) in order to evaluate the noise contribution associated to the analog electronics parts only.

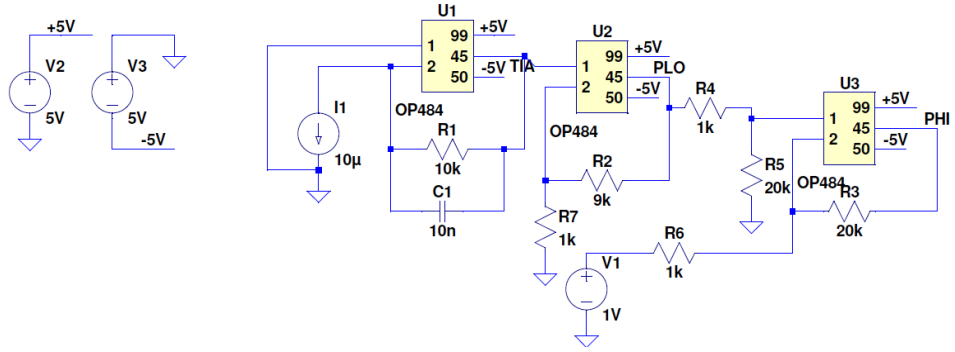

Figure 11: SPS readout electronics scheme used for noise evaluation and simulations with LT Spice.

From the performed simulations (refer to Figure 12) we evaluated the σ_{amp} noise term to be negligible (integral noise lower than 1 mV, adopting an analog bandwidth from 100 µHz to 1 MHz) with respect to the uncertainties introduced by the ADC and mainly by the DAC. In particular, thanks to the impedance coupling between the transimpedance stage and the SPS detectors, the noise produced by the transimpedance stage itself can be limited to a very small contribution that does not affect at all the overall noise value, despite the high gain to be taken into account between the SPS sensors and the analog electronics chain output.
These results leave us some margin for the σ_{cte} noise term and highlight at the same time the importance of the σ_{DAC} contribution. For this reason we are planning to generate by the DAC only a few calibrated voltage levels (those strictly needed to match the overall dynamic range) in order to limit as much as possible its contribution to the overall noise.
Another important aspect concerning the overall noise contribution is related to the stability and noise level on the power supply voltage lines. This could be a very critical issue especially when operated the SPS electronics at system level, as the satellite environment is often affected by electromagnetic disturbances.

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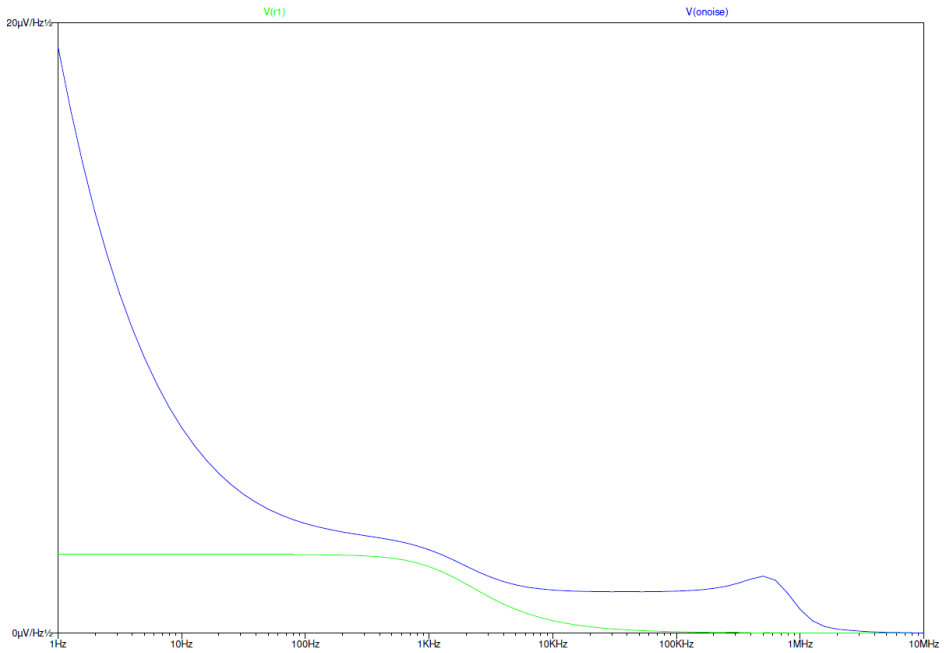

Figure 12: SPS analog readout electronics noise spectral density as a function of frequency. Blue curve: overall output noise. Green curve: transimpedance stage feedback resistor contribution.

7. SPS BREADBOARDING ACTIVITY

In order to evaluate the performances of the SPS readout electronics design, it has been realized a simple single-sensor breadboard (Figure 13) based on the design evolutions occurred during Phase B2 of the project.

Breadboard design

The schematic for the breadboard is shown in Figure 14. The sensor is fed to the input of one of the four OP484 amplifiers in a single package. This amplifier is configured as a trans-impedance amplifier with a gain of 10^4. A jumper (J3) allows the input of the LO gain amplifier to be routed from the output of the trans-impedance amplifier on a SMA connector (J4). The SMA connector can be used to simulate the signal from the TIA to evaluate the performance of the readout electronics section.

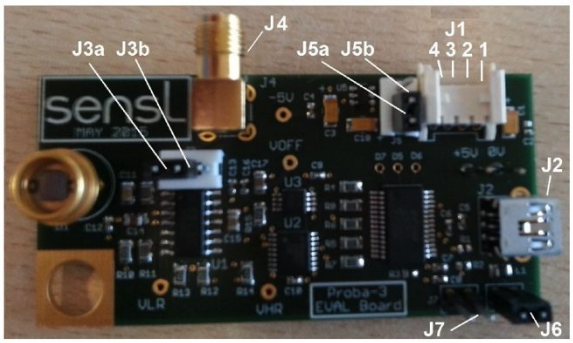

Figure 13: Single channel breadboard PCB design.

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The output of the LO gain amplifier (G = 12, tuned for the breadboard) is routed to one of the ADC channels as well as an input to the differential amplifier (G = 10, tuned for the breadboard). The output of the differential amplifier is fed to a second ADC channel. The second input of the differential amplifier is set by the output of the 12-bit DAC (DAC121S101).

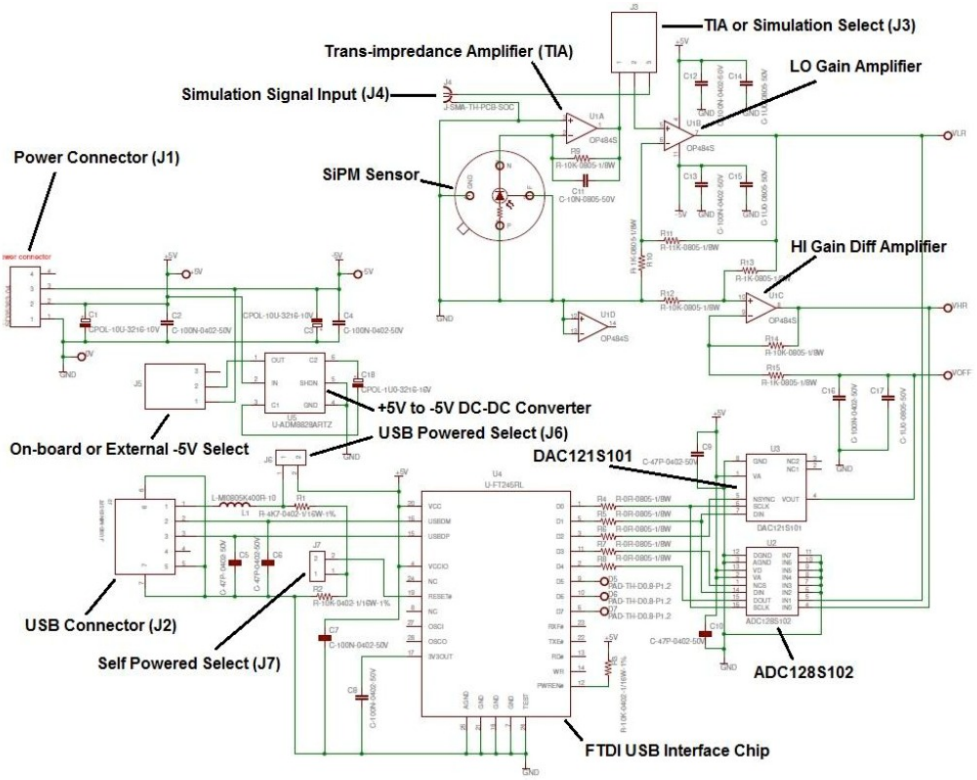

Figure 14: Schematic of a single channel breadboard.

All reading and writing operations on the DAC and ADC are carried out via a standard FTDI USB 1.0 interface. J6 and J7 are jumpers that allow the board to be either powered by the USB (J6 ON, J7 OFF) or by the Power Connector J1 (J6 OFF, J7 ON). A further jumper is provided to select either on-board -5 V supply (from DC-DC converter) or external -5 V supply via J1.

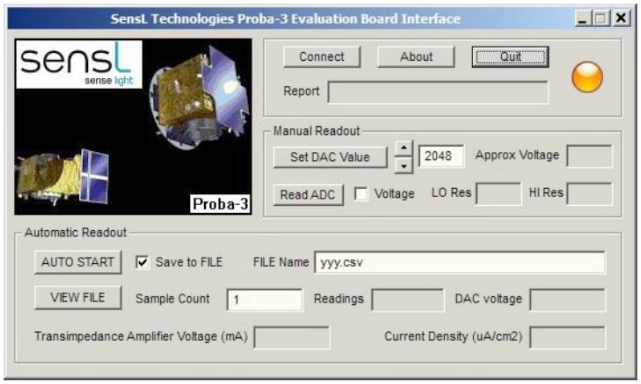

Figure 15: SPS evaluation board GUI.

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To facilitate the evaluation of the breadboard has been designed a Graphical User Interface (GUI) software package to allow the user to manually set the DAC and read the ADC values. The GUI (Figure 15) also allows the user to run the breadboard in AUTO mode. In this mode the ADC values are read and then based on the value of the LO Gain Amplifier, the DAC is set to an offset to allow the HG resolution Difference Amplifier voltage to be used to report the sensor current in $\mu A/cm^2$.

Breadboard test

Using the AUTO mode 60 readings were saved to a file using sample counts of 1, 100 and 512. This test was carried out for three different signal levels representing the low, the middle and the high end of the dynamic range. From the recorded values the Average value, Max, Min, Range and Sigma (Standard Deviation) were calculated. The results for the signal level of ~6 $\mu A/cm^2$ (low-end dynamic range) are reported in Table 4, showing that multiple sampling improves the accuracy of the readout as expected.

The results show that, in all cases, for a sampling count of 512 the variation of the signal (range and sigma rows) was less than the required resolution. Indeed, the 3-Sigma value obtained with 512 samples is just one half the required accuracy. This result, if confirmed by further measurements, shows the SPS readout electronics compliance with respect to the *SPS performance requirement* in terms of Nyquist sampling concept.

Samples count	1	100	512
Average	6.2872	6.2842	6.2843
Max value	6.5460	6.3030	6.2940
Min Value	6.0820	6.2570	6.2760
Range	0.4640	0.0460	0.0180
Sigma	0.0808	0.0083	0.0044
3-Sigma	0.2424	0.0250	**0.0133**
Sigma(1)/Sigma(512)			18.3

Table 4: Signal set to ~6 $\mu A/cm^2$ (required resolution ~ 0.025 $\mu A/cm^2$).

It should be also noted that the variation of the signal for a fixed input could be due to the source signal drift and may not be completely due to the accuracy of the electronics. This parameter will be investigated in more detail as part of the DM evaluation.

In the actual SPS electronics design the digital signal readout will be carried out by an FPGA. It is therefore important to estimate the rate at which the FPGA will be able to carry out a single measure to estimate the maximum possible samples that can be taken per cycle. The readout procedure will be carried out using the ADC128S102, for reading signal values, and DAC121S101 for setting the DC offset. For a 2 Hz cycle time the FPGA will be potentially able to average more than 7k samples.

8. CONCLUSIONS

In this paper we have provided an overview of the current design status of the readout electronics of the SPS subsystem on board the PROBA3 Mission, as derived from the SPS relevant requirements. The presented electronics error budget shows that its contribution to the overall SPS error budget could be properly limited adopting the multiple sampling readout technique at least. Likely, the SPS overall error budget will not allow a full compliance with respect to the *SPS*

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performance requirement but some ways to reduce the SPS electronics noise term have been identified and will be further investigated in the next phase of the project.

9. ACKNOWLEDGMENT

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