Design and prototyping of the Italian Tile Processing Module 1.6 (ITPM) for the Low-Frequency Aperture Array deployment.

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ABSTRACT

A novel version of digital hardware Italian Tile Processing Module (ITPM) 1.6 has been released for the Low-Frequency Aperture Array (LFAA) component of the Square Kilometre Array (SKA). This back-end includes two plugged-in main blocks, as an analog device , the Pre-ADU board, and an Analog to Digital Unit (ADU), a 6U board containing sixteen dual-inputs Analog to Digital Converters and two Field Programmable Gate Array (FPGA) devices, capable of digitizing and processing 32 RF input signals (50-650 MHz). We present the main features of the upgrade of the board compared to previous versions: there are new and high performance components improving processing capability, mechanical changes matching the design of the housing sub-rack and finally a general reduction of the overall power consumption. The ITPM ADU 1.6 version, now in engineering phase together with its sub-rack system, is currently the last prototype before the design of the industrial line for mass production, necessary for the LFAA deployment. Results of system performances will be presented.

Keywords: Italian Tile Processing Module (ITPM), Low Frequency Aperture Array (LFAA), Square Kilometre Array (SKA), Aperture Array Verification System 1 (AAVS1), Kintex Ultrascale+ Field Programmable Gate Array (FPGA), Digital Beamforming, Digital Signal Processing.

1. INTRODUCTION

The Square Kilometre Array (SKA) will be the largest and most sensitive radio telescope ever built[1]. It will be constructed in two phases (SKA1 and SKA2)[2] over two sites, South Africa and Western Australia, and at the end of the second phase, it will provide about a million square meters of collecting area through many thousands of connected radio telescopes.

The Low Frequency Aperture Array (LFAA)[3] is the low frequency section of the SKA, and is currently designed to produce 512 logical stations to be installed in Australia, which can be flexibly configured by programming the signal processing platform to send its traffic across a highly configurable network.

A single LFAA station is composed of 16 tiles, each of which gathers the signals from 16 dual polarized antennas. Signals are digitized, channelized and beamformed together, in order to allow the electrical pointing of the telescope. Each tile (16 antennas) is processed in a Tile Processing Module (TPM)[4,5] that is the data processor of each group of antennas, as well the core of the digital equipment of the overall LFAA section.

The purpose of this work is to mainly describe the Italian TPM prototype (ITPM), developed since 2013 together with its digital, mechanical and firmware platforms in the framework of the activities of two working phases: first, the Aperture Array Design and Construction Consortium (AADC) of the SKA LFAA and next the SKA Bridging Phase, that is still ongoing, which will follow the construction phase of the radio telescopes. The project was led by the Italian Istituto Nazionale di Astrofisica (INAF) in collaboration with University of Oxford, Malta University, Science Technology

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Facility Council (STFC) and Sanitas EG company. After various successful prototypes, the first release of the complete design was the ITPM 1.2 version, obtained assembling an Analog to Digital Unit (ADU) board and two Pre-ADU boards. That release was used in 2017 for the Aperture Array Verification System 1 (AAVS1)[6] demonstrator, which includes the deployment of 200 antennas at the Murchison Radio-astronomy Observatory (Western Australia), and now deployed for AAVS2 and EDA2[30,31] demonstrators.

The last ITPM 1.6 version described here, was adopted as reference design for the Tile Processing Module in 2019 by AADC consortium within the LFAA Critical Design Review process[7]. INAF supports an activity for engineering the digital equipment in order to make it ready for the phase of industrialization and mass production for the incoming SKA low frequency radio telescope deployment.

The next paragraph describes the scientific context in which ITPM was developed and the intermediate prototypes until the last release 1.6. The section 2 reports the architecture of ITPM and its functional requirements; the section 3 briefly describes the FPGA firmware for the signal processing chain, while the section 4 contains the results in terms of performances that match the final LFAA functional and operational specification.

1.1 ITPM Evolution

Objective of the Italian Tile Processing Module project, born from an international collaboration led by Italian Istituto Nazionale di Astrofisica (INAF) operating within the Aperture Array Design and Construction Consortium, was the design and prototyping of an acquisition and processing system for the SKA Low Frequency Aperture Array telescope. The project started in 2013 and various releases of the system have been implemented in the course of the years; its progressive maturation until the final release for the CDR is ITPM 1.6, consisting of ADU 1.6 and Pre-ADU 2.5 boards.

The rationale for the development of ITPM 1.6 has been twofold: a global effort towards power consumption reduction and integration and an increase of the processing capability of device itself.

The main concern for the first prototyped ITPM, with ADU 1.2 version, was the power dissipation, given the small board size and the need to keep the device temperature below 65° C. The conceived air cooling system for the LFAA site required bulky heat exchangers and a related amount of power, and plenty of space inside the cabinet for ventilation. The availability of a new generation of components (FPGA at 16 nm and ADC at 28 nm) has allowed the reduction of the power density and a significant increase in the efficiency of the system, both for the consumption of the board and the consumption / volumes required for the cooling system. The main components of the ADU board have been upgraded with respect to initial 1.2 release: FPGAs have been replaced by Xilinx 16 nm Kintex Ultrascale+ devices, the AD9680 ADCs have been substituted by low power AD9695 ADCs, DDR3L memories have been updated to the DDR4 family to improve RAW data buffering. The board hosts sixteen memory chips, 4 Gbit each, with a 64-bit wide memory bus, for a total of 4+4 GByte memory. Thanks to this evolution, the ADU board maintains the original architecture and increases the performance/resources reducing about 20% of the absorbed power.
Moreover, through a careful mechanical design of the sub-rack hosting ITPM, in order to minimize cabling at cabinet level, has been developed a solution consisting of a backplane, implementing connections among ITPMs and allowing for an easier installation/maintenance of the overall system. It has been possible to integrate in the same subrack eight ITPM units, each with local management functions for power supply, clocks and networking.

1.2 ITPM Applications

ITPM board assembly is not only used for SKA applications such as Low Frequency Aperture Array, but also for a number of scientific programs developed mostly in the fields connected to radio astronomy. The international team that developed ITPM since the beginning of the design aimed to build a general purpose board, realizing a new generation high speed and multichannel acquisition/processing platform, able to cover different needs in radio astronomy.

Among these applications the first to be mentioned is PHAROS II[8,9] project, a cryogenic C band (4-8 GHz) Phased Array Feed (PAF) demonstrator developed by University of Manchester and INAF. The ITPM board has been used to process the signals coming from sensors composing the array feed.

Other important applications in which ITPM is widely used are Space Debris Monitoring[10,11,12,13] and Fast Radio Burst Monitoring[14], both have in common the same instrument, the Italian Northern Cross radio telescope, located in Medicina

(Bologna, Italy). In addition, the Sardinia Array Demonstrator[15], that is an important Italian array demonstrator deployed in the neighborhood of Sardinia Radio Telescope (SRT).

Another application of ITPM involved the Mexican Radio Telescope (MEXART)[29], that is a regular aperture array consisting of 4096 full wavelength dipoles whose primary scientific objective is to carry out interplanetary scintillation observations of solar wind disturbances, located in the state of Michoacan in Mexico.

Commercial applications in the field of radar and automotive are in phase of feasibility study by SANITAS EG.

2. ITPM 1.6 ARCHITECTURE

2.1 ITPM Overview

The TPM is the main sub-system of the LFAA signal processing system. This is a rack-mounted unit that processes the signals from 16-antennas in dual polarization. The TPM receives the analogue signals from the RF antenna amplifiers, as analogue RF over Fibre optical signals, amplifies and filters them (RF conditioning), converts them in digital form and digitally processes them to form station beams. A number of 16 Tile Processing Modules related to one station are connected in a daisy-chain using a high-speed data switch. Partial beams are sent along a chain of 16 TPMs, with each TPM combining the internally generated partial beam with the travelling one. The final station beam is then sent to the Central Signal Processing (CSP) facility. The data switches are used also to interface the TPM to the monitor, control and calibration servers, both for local monitor and control functionalities and for sending to these servers calibration samples to be stored in the transient buffer. A functional diagram of the TPM is illustrated in Figure 1.

The Italian TPM presented here is mainly composed of two boards: the ADU (Analogue to Digital Unit) board and pre-ADU boards. Pre-ADU boards are devoted to optical-electrical conversion, filtering, amplification and equalization of 32 analogue signals. The ADU board has the task of: analogue to digital conversion, polyphase filtering, application of calibration and beamforming coefficients, sum of all 32 signals to form the tile beam (local), sum the tile beam with the incoming partial station beam and transmission of the data to the network (switch). A photo of the assembly is shown in Figure 2.

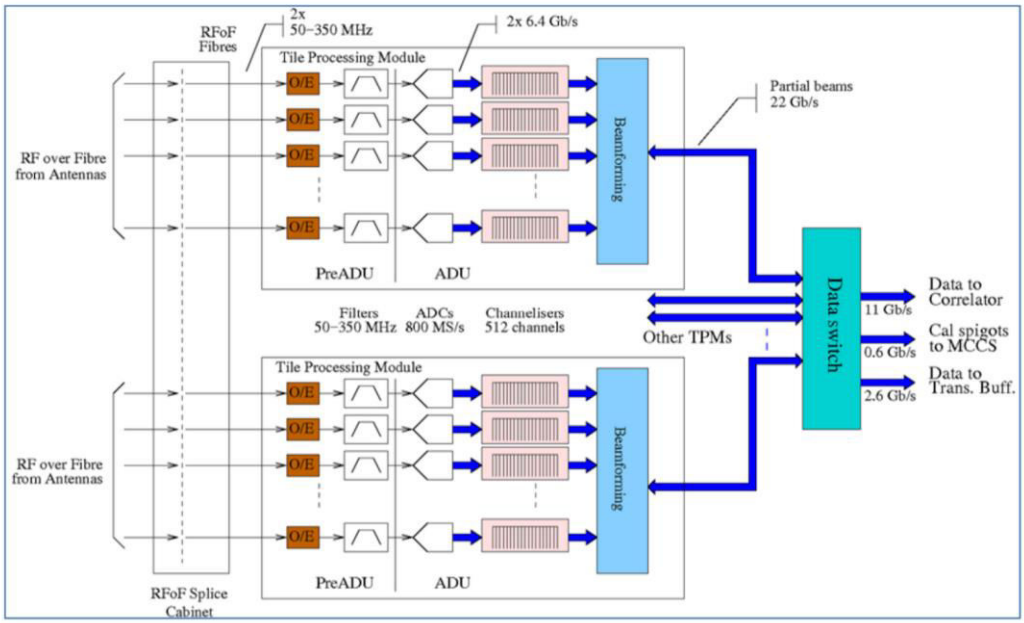

Figure 1. ITPM 1.6 Functional Scheme: Analog section on the left, digital processing block on the right, digital flow from left (antennas) to right (Correlator) .

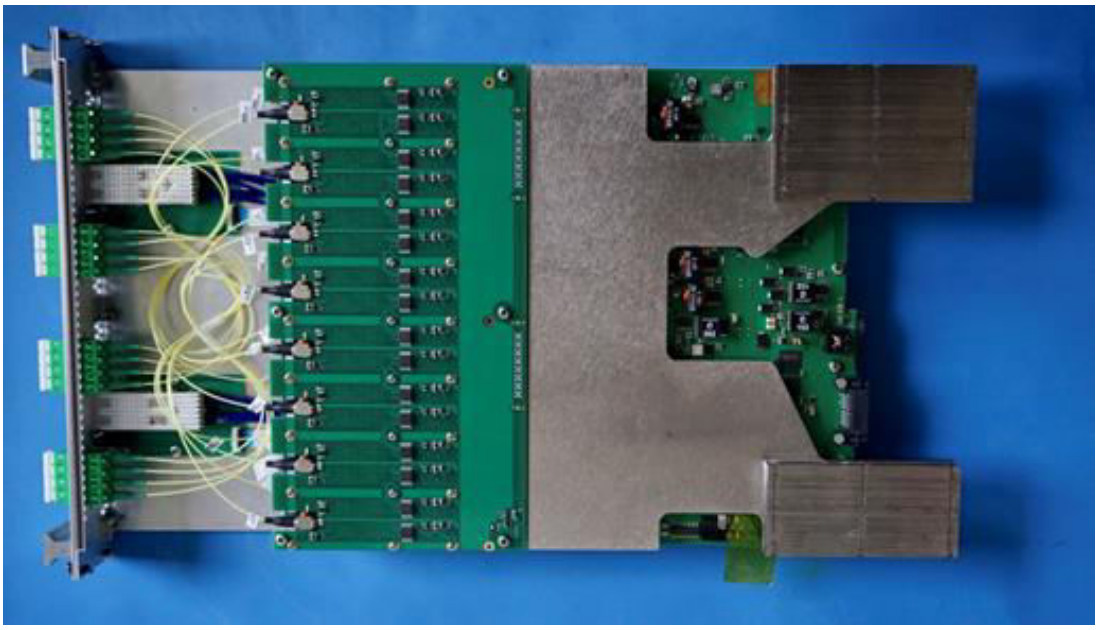

Figure 2. ITPM 1.6 assembly: from left to right, Pre-ADU, ADU board plugged in together, and heat sink.

2.2 Pre-ADU

Pre-ADU board corresponds to the analogue receiver in front of the ADU. The current design pre-ADU 2.5 hosts 8 double channel analogue receivers (i.e. 16 analogue chains). The two chains in each double channel receiver correspond to the two antenna polarizations. The first stage of any pre-ADU channel is an optical receiver (ORX) which converts back to the RF domain the signal transmitted through an optical fibre from the remote antenna. The current pre-ADU version adopts WDM (Wavelength Division Multiplex) optical receivers, which paired with WDM optical RFoF transmitters at the antennas, allows the use of one single fibre for both antenna polarizations.

A standard direct RF receiver (i.e. without any frequency conversion) follows the ORX connectors. Several functions are here included to adapt the signal for the digital conversion as amplification, level adjustment (by means of a digital step attenuator, 31 dB range/1 dB step). The digital step attenuator is controlled by the ADU board via the SPI bus. Architecture of the pre-ADU board[16] has simplified the mechanics and interconnection to the ADU, but also the RF electronics. For the future generation of ITPM it will be considered the possibility to use a differential driver stage in front of ADC (what we called VGA), thus allowing to avoid the last amplification stage and any digital control on board because the VGA is directly controlled by SPI.

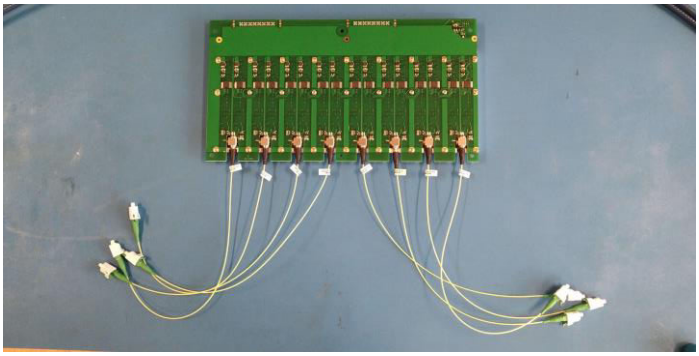

Figure 3. ITPM 1.6 Pre-ADU board

2.3 ADU

The ITPM ADU is a 32-channel 1GHz 8/14 bit Analog to Digital conversion/preprocessing board [4,16,20,21,22], equipped with management functions to support the integration into the rack structure. Best-in-class 14 bits AD converters, last 16nm FPGA, 40Gbit Ethernet optical links have been selected focusing on the best commercial compromise between quality, performance and power consumption.

Compact board size, low noise clock network, advanced 14-layers board build-up, complete Ethernet-based management functions (including health monitoring capability), high efficiency and low noise power distribution system complete the main board features. The ADU also needs external synchronization signals and high speed DDR4 memory banks to allow RAW data buffering. An on-board 32 bit microprocessor and large flash memories allow for high-level management operations including on line multiple configuration selection and structured communication with infrastructure management applications. A low-level management firmware performs board configuration and monitoring through the Ethernet interface exploiting a UDP based protocol.

The following list sums up the remarkable ADU characteristics and features:

- Compact size, 6 unit format, designed for backplane installation;
- Thirty-two analog inputs capability with high quality and high isolation stackable RF 50Ohm input connectors;
- Thirty-two optional analog programmable drivers (amplifier/attenuator, not present on default configuration);
- Sixteen dual channels 14 bits 1Ghz AD converters;
- High quality clock distribution system with full JESD204B Subclass 1 capability on all inputs, with deterministic latency between the channels and the user configurable low noise PLL;
- Two Xilinx Ultrascale XCKU9P 16 nm FPGA devices dedicated to data processing, implementing the same functionality, managing 16 channels each;
- Two DDR4, 64 bit memory banks, up to 16+16 GByte total size;
- Two 40Gbit Ethernet interfaces (QSFP+), one for each FPGA;
- High speed internal bus to connect the 2 FPGAs, up to 75 Gbit + 75 Gbit bidirectional;
- Low-level Gigabit Ethernet management interface with instant ON flash based Lattice CPLD;
- Complete system monitor interface with power, voltage and temperature monitoring;
- On board two 256Mbit SPI user flashes for multiple FPGA configuration options;

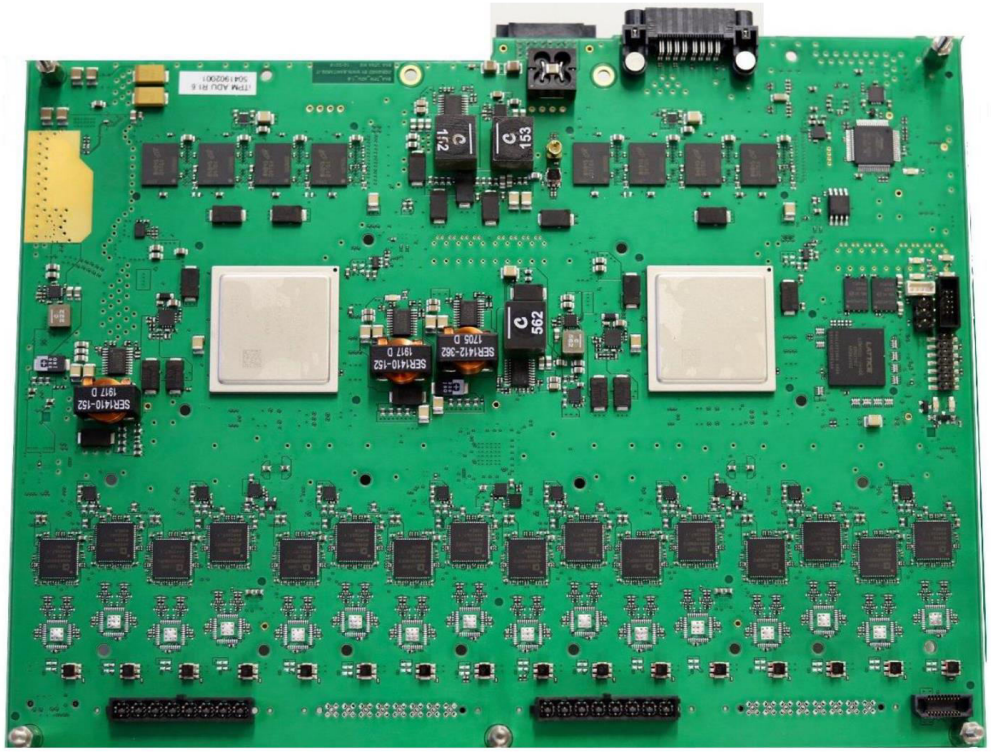

Figure 4. ITPM 1.6 ADU board top view.

- High efficiency multistage Power Distribution system, with configurable start up and power sequence.
- Compatible with Xilinx JTAG Virtual cable capability for complete remote debugging based on the Gigabit Ethernet management link.

The ITPM ADU processor board is organized in three areas, from left to right as reported in Figure 5: management and power supply, FPGA and memories, analog signal interface. The organization of physical components layout into three separate areas has been adopted to obtain high performance and noise isolation among DC-DC converter, digital elements and analog interface. The **management interface** includes the 10/100/1000 Mbit/sec data link, the flash based CPLD (U1), the Micro Controller Unit & System Monitor (U4), the SPI flash memories (U6, U7) and the CPLD external configuration flash (U19).
The configuration registers and the device control signals are managed by the CPLD (U1). This device has an internal flash and is auto-configuring at the board start-up. It provides Ethernet user interface and bus lines to connect all the devices configuration interfaces. The low level CPLD functions can be grouped in upper level functions by the MCU that interfaces with a dedicated SPI bus and GPIO with the CPLD.

ITPM ADU acquisition data path is organized in five sections: the analog to digital conversion, the data elaboration inside FPGAs, the data buffering in the memory banks, the data communication between FPGAs and the external interface optical link. Sixteen lines from ADCs can generate up to 16 GByte/s of raw data at maximum sample rate. JESD IP core manages the physical interface and is connected with an internal bus to the data processing core. The DDR 64 bit memory interface can perform read or write operations (800 MHz clock) on a maximum amount of data of 16GByte. Also, it can be connected to the JESD interface to implement a 128 Msample raw buffer. The FPGA**s** are two identical devices (U2, U3) Xilinx Ultrascale XCKU9P 16 nm, that provide suitable and efficient resources to implement all the main board data management and elaboration.

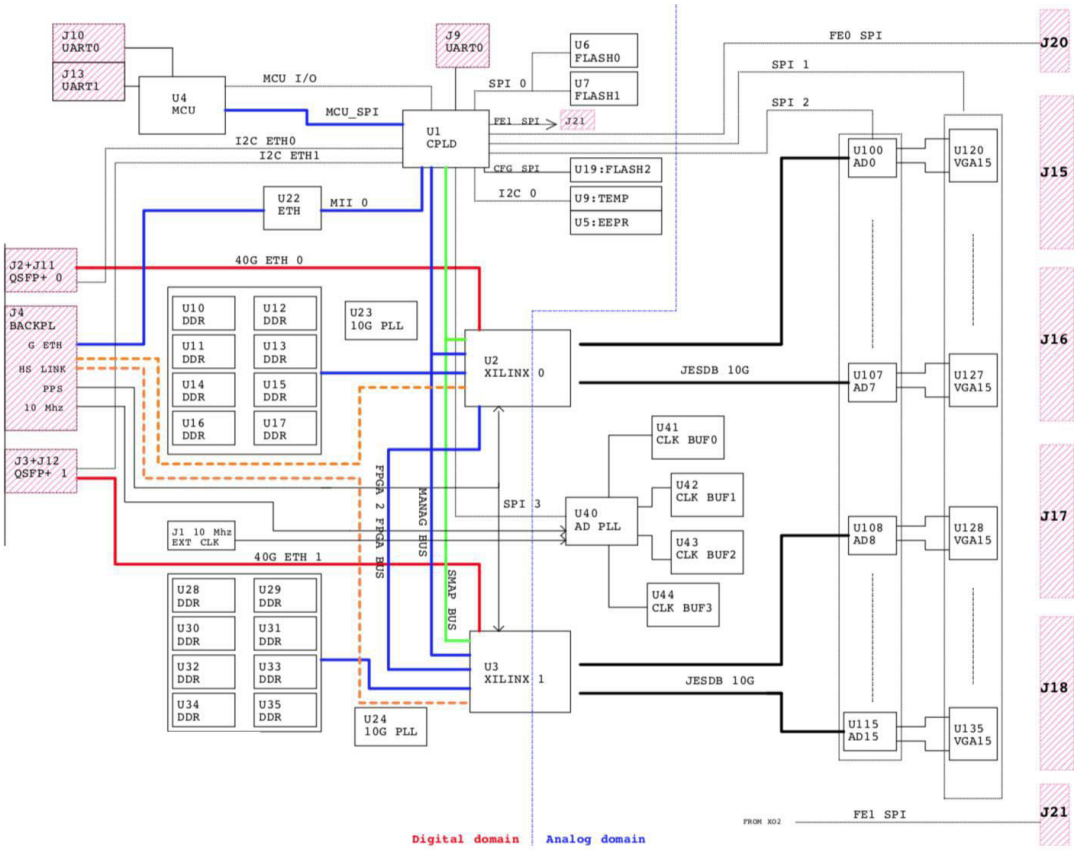

Figure 5. ITPM 1.6 ADU Schematic view, data processing flow reading from left to right.

Finally, the analog section includes the acquisition clock generation and distribution network (U40, U41 – U44), the sixteen dual channel ADCs AD9695 14 bit 1GHz (U100-U115), the sixteen dual channel analog buffers (U120-U135) and the four RF high isolation x8 input connectors (J15-J18). Two connectors (J20 and J21) provide power supply and digital SPI control for a pluggable analog board for signal over-fiber connection and physical connection, as the Pre-ADU module.

2.4 ITPM Housing

The sub-rack system[21] is the basic structure required for the ITPM board integration. The current sub-rack version includes a backplane that implements all the links among the ITPM boards and power distribution, leaving the high speed 40Gb/s optical fiber links and RF connections on the front panel only. This element provides accessory functions needed for continuous operation inside the LFAA cabinet. In order to simplify rack cabling and design, the idea is to provide to the ITPM all the services that can be moved from the front-panel to the opposite side, with a backplane. The backplane design is not critical, in terms of connection density and signal speed.

Each sub-rack shall provide the following functions:

- Mechanical support for 8 ITPM boards;
- Backplane to distribute to ITPMs Power, Gigabit management Ethernet, 10MHz clock and PPS;
- Support the air cooling at sub-rack level for ITPMs and management boards;
- Monitor each board absorbed current;
- ON/OFF Power capability of each ITPM board (hot-swap if possible);
- CPU with Linux OS to manage high level operations;
- Two Ethernet gigabit management interfaces;
- Power Supply;
- Easy access to the input optical interfaces: the RFoF LC connectors are plugged on the front panel;
- Easy access to the 40Gbit Ethernet QSFP+ cables: the QSFP+ cages are plugged on the front panel.

The proposed solution is a 6U standard chassis with a custom backplane, a management board placed within the ITPMs and a power supply unit on one side. The Management board is placed in the center of the sub-rack and implements all the required functions needed to the ITPM to operate, including the power control, the distribution of clock and synchronization signals and the gigabit connection. The Management board can be remotely interfaced with a control application to execute cabinet-level operations, as ITPM configuration and monitoring.



Figure 6. Detailed view of ITPM sub-rack rear (left), front (right)

3. ITPM FIRMWARE

In this chapter, a brief description of the firmware blocks that have been developed for LFAA is reported [24,26]. According to the functional point of view, the ITPM is organized in two main sections: the management and control plane and the acquisition and processing plane, as shown in Figure 7.

3.1 Management and control plane firmware

The CPLD is the main component in the control plane. This device hosts an internal Flash memory and is auto-configuring at board power-up. It manages the access to the control registers of on-board devices through dedicated busses:

- RGMII to Ethernet PHY for the remote board control;
- FPGA management bus for FPGA register access and debug purposes;
- SelectMap bus for fast configuration, reconfiguration and monitoring of the FPGAs;
- C2C Stream bus for transferring data from the FPGAs to the CPLD;
- I2C to the system monitor, temperature sensor and 2 Kbit EEPROM;
- I2C to both QSFP+;
- SPI to three identical high speed Flash memories to store non-volatile configuration data;
- SPI to the ADCs;SPI to PLL.

The main CPLD responsibility is twofold:

1. After board power-up the CPLD is responsible for enabling the on-board voltage regulators powering FPGAs, ADCs, PLL and Analog Front End. The power-up sequence can be customized to avoid excessive in-rush current.
2. It acts as a bridge between the network and the on-board devices such as FPGAs, ADCs, PLL, allowing the user to access them through the 1Gbit Ethernet link.

The user interface to the CPLD is based upon an UDP-IP core which manages MAC, IP and UDP layers and allows the user to execute sequences of memory mapped bus accesses from a network device. The specific protocol implemented

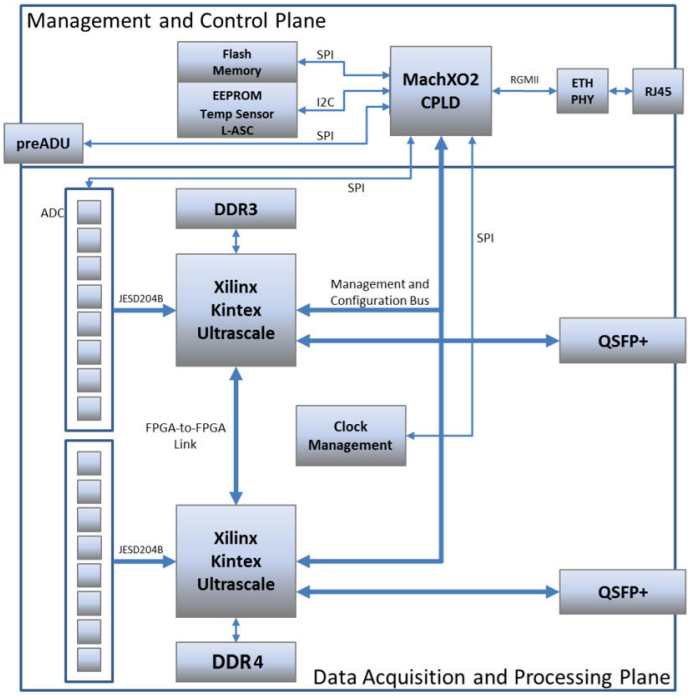

Figure 7. Firmware functional components.

over UDP to convey the information about the memory mapped accesses is the Uniboard Control Protocol. The CPLD is able to decode a UCP packet and translate the memory access into an internal bus access, thus allowing the user to access registers that have been memory mapped into the CPLD address space.

3.2 FPGA Firmware Architecture

The FPGAs constitute the main processing elements on the ITPM. They provide high-speed interfaces to ADCs, DDR4 modules, 40Gbit Ethernet links and CPLD, and implement the DSP functions to process data acquired from ADCs. Additionally, the FPGAs provide the functionality to extract data from the DSP chain and transmit them to the CPLD over the C2C streaming bus at suitable data rate such that the extracted data can be forwarded over the 1Gbit link for monitor, control and debug purposes.
The FPGA Firmware is mainly coded in VHDL and structured in such a way to simplify the transition to different boards, FPGA vendors and families. Technology dependent code is isolated into specific portions and industry-standard interfaces are implemented to enable the communication between main parts of the design.
Leveraging standard interfaces allows the designer to transparently modify the implementation of part of the design while maintaining compatibility with the rest of it. The FPGA Firmware consists of a top level board wrapper, which is customized to support the specific board pinout; the firmware is then partitioned into two main sections. An I/O ring section includes all external interfaces and technology dependent modules such as PLLs, transceivers and physical layers. The I/O ring is directly connected to the DSP section using industry standard busses, as shown in figure 8.

3.3 DSP Firmware

The LFAA station beamformer structure is based on a frequency domain beamforming architecture. Data streams from the individual antennas are channelized with a channel spacing of 781.25 KHz, and delayed in the frequency domain by applying a dynamic phase correction to each individual channel. Each signal is also corrected using a static instrumental gain, phase and polarization calibrations, updated on a timescale of a few minutes. It is possible to select multiple regions in the processed band, and/or to generate multiple beams of the same or different spectral regions. The channelization process is used both to allow for frequency dependent calibration, for frequency domain beamforming, and to provide the first stage of a two-stage channelizer.

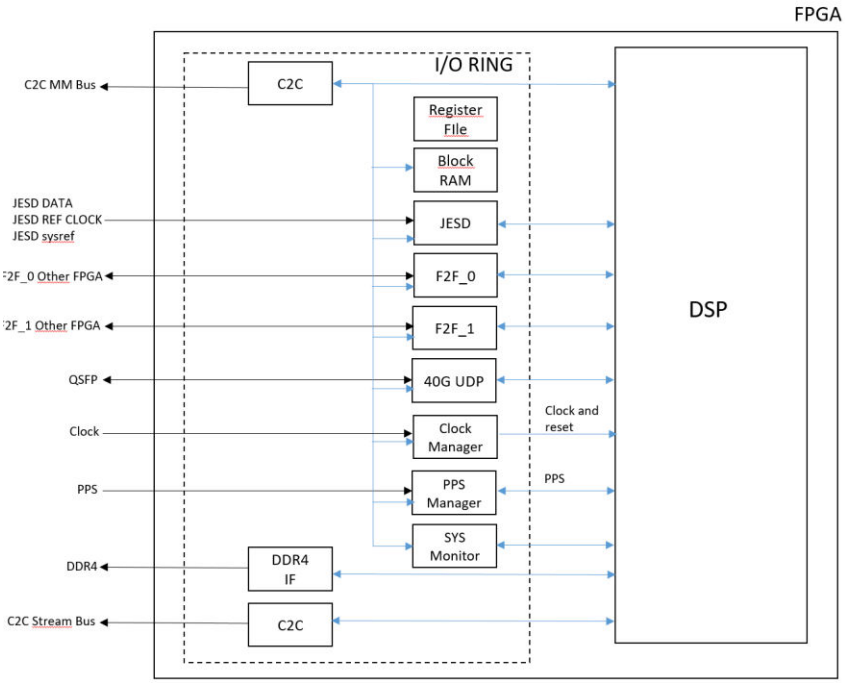

Figure 8. Functional separation of FPGA firmware.

Processing is performed in groups (tiles) of 16 antennas in a TPM. TPMs are connected together in a flexible way using the 40 Gbit Ethernet high speed network, with non-blocking network switches. Stations can then be configured dynamically as arbitrary groups of tiles. The same network is used to transfer samples from individual antennas to the control, calibration and monitor subsystem, and beamformed samples to the Central Signal Processor. Data to be sent to the CSP is packed into frames of 2048 samples for one frequency channel, two polarizations. This requires a corner turner operation from the channelizer output (frames of one time sample, all channels) to the CSP frames (one channel, many consecutive time samples). The firmware has been optimized for the Italian TPM.

The firmware structure is adapted to a time multiplexed data stream, with 4 samples processed in parallel at each FPGA clock cycle. After channelization and beamforming, odd and even frequency channels for the whole tile beam are processed separately in the two FPGAs. Channelized data is stored in an external local memory, that is used for the corner turner function.

Data rates are also shown in Figure 9. Each ADC generates 800 Mbyte/s of 8 bit samples, for an aggregate data rate of 204 Gbps. The channelizer selects a bandwidth of 300 MHz, oversampled to 356 Msample/s, with resolution increased to 12+12 bit complex samples. The aggregated data rate after the channelizer is then 274 Gbps, that is reduced by a factor of 16 (one beam every 16 antennas, 17 Gbps) in the tile beamformer. Half of this information is exchanged between the two FPGAs. The travelling sum on the 40 Gb interface uses 16+16 bit complex samples, for a data rate, including packet overhead, of 23.2 Gbps. The final beamformed data to the CSP is represented with 8+8 complex samples, with a data rate of 11.6 Gbps. The calibration subsystem requires a subset of the channelized samples for one channel, all antennas and polarizations, represented with 8+8 bit complex samples. The corresponding aggregated data rate is about 0.5 Gbps.

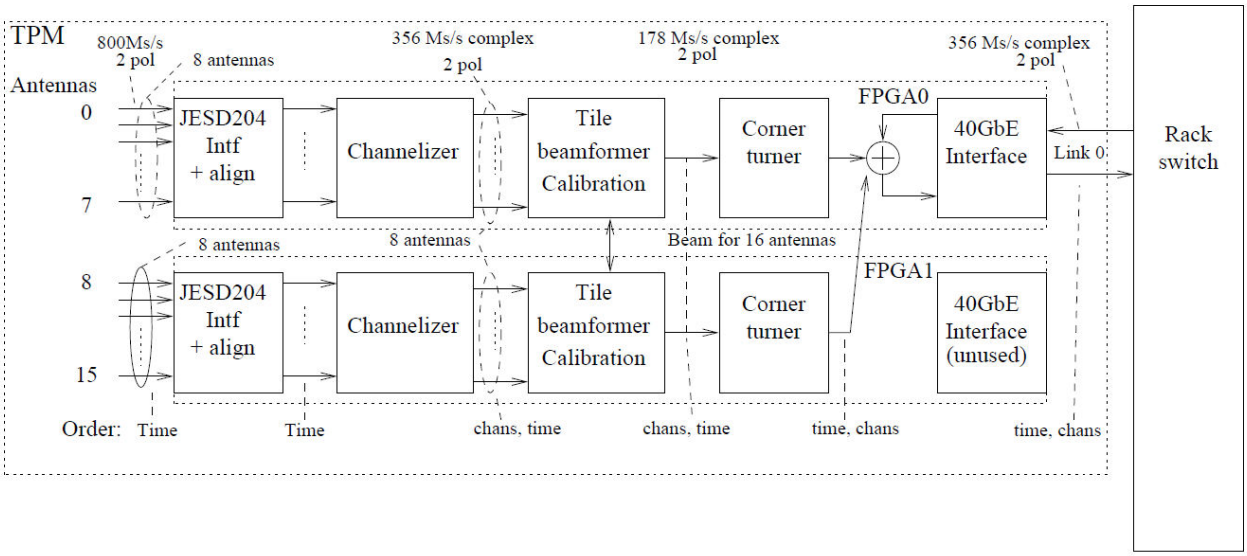

Figure 9.Tile Processing Module signal chain .

4. ITPM PERFORMANCES EVALUATION

This section presents the performance parameters of ITPM equipment, in terms of the two main aspects required by Aperture Array Consortium design of overall LFAA, the RF parameters and the power consumption.

4.1 RF Results

Preliminary RF results are reported in Table 1; they are compliant with the LFAA specifications[6,7,16] arising from simulations and on the field verifications carried out by AADC teams.

The hardware setup for performance tests on the ITPM board is depicted in Figure 10 and is composed of:

- a signal generator with good signal purity and low phase noise locked to a stable reference signal;
- band-pass filters;
- power meter (or spectrum analyser) and low noise power supply;
- ITPM Board under test supplied with stable reference signals (10 MHz ref. and PPS);
- a server for instrument control, data acquisition and data analysis.

Tests have been accomplished by using a previously developed method comprising the following steps: to inject a very pure and stable tone into each ADC RF input and acquire it (acquisition sample rate at 800 MSPS) into the buffer memory of the FPGA that captures a block of digital data. Data is then transferred to a server that performs FFT computation and returns some performance parameters, including SNR, SFDR, SINAD, and ENOB. The procedure is repeated for a predefined number of frequencies (typically 50) evenly covering the SKA LFAA bandwidth (50-350MHz).

Results are illustrated in Table 1. Data represents the worst value of the parameters measured for each input channel.

Table 1. Measured ITPM - ADU RF performances

Fs: 800 MSPS --- BW: 50 ÷ 375 MHz	
ADC Performance Parameters	**ADU Board ver. 1.6**
Signal to Noise Ratio referenced to Full Scale [dBFS]	**≥ 48.14**
Gain Flatness [dBFS]	**≤ ±0.81**
2nd-order Harmonic Distortion [dBc]	**≤ -69.86**
3rd-order Harmonic Distortion [dBc]	**≤ -65.28**
Worst Other Spur [dBc]	**≤ -59.02**
Spurious Free Dynamic Range [dBc]	**≥ 59.02**
ENOB [bits]	**≥ 7.70**
Cross-Talk [dBc]	**≤ -44.30**



Figure 10. Test bench used to test the first prototype of ITPM board ver. 1.6 at Medicina radio astronomical station.

4.2 RF Results

Power consumption is a fundamental parameter of the design, as radio telescopes are deployed in desert zones. The study of different versions of ITPM in many years has focused particular efforts towards the reduction of the power consumption of the boards, and the operative equipment as well, first of all the sub-rack. The final design of ITPM and sub-rack is compliant with power budget requirements.

Table 2. Measured ITPM - ADU Power budget divided in sections or components.

Item/Section	**Power (W)**
CPLD, Eth, Flash, MCU	3
STATIC IP DATA ACQ DDR CORE Local bus, clocks 40 G Ch 0 40 G Ch 1	1,12 10 2,04 26 1 1,25 1,25
PLL, CLKBuff, 10G Pll AD	3,6 19,2
Front END TOTAL DIGIT IC TOTAL ANALOG IC TOTAL int 5V supply	10,6 46,9 59,4 21,3
TOTAL Supply	**112**
Assumed efficiency	
Digital DC-DC efficiency: **Analog efficiency (8%):** **Input DC-DC eff:**	**94%** **86,48%** **95%**

Table 3 Power budget measured according to operative configurations and functional conditions.

Test phase	Power (W)	Active part
Power ON	3,99	Management
Digital supply ON (FPGA not programmed)	6,00	Only digital side powered ON, FPGA not programmed, PLL off
Digital supply ON (FPGA programmed)	18,89	Only digital side powered ON, FPGA programmed, PLL off
All supply ON	17,90	All supply active, FPGA not programmed
All ON, FPGA programmed	32,29	FPGA programmed
Acquisition	64,91	32 channel active at 800 Ms/sec

Measured power is greatly dependent on both board and ambient temperature. Proper air flow shall be provided and maximum board and component temperature is monitored. The power budget is compliant to the value requested for LFAA, and with the minimum power consumption allowed by the adopted technology. In Table 3 is reported the power consumption according to the operational mode and the functionality of the board.

5. CONCLUSION

The Italian Tile Processing Module (ITPM) is the digital processor adopted by SKA LFAA consortium as reference design for future production and deployment of the Low Frequency SKA telescope. After seven years of development which has led to different phases of board definition process and a number of prototyped boards, a final version ITPM 1.6 has been released.

The overall ITPM system was schematically presented, going into detail to describe the various parts that compose it. Also the operational parameters, as well RF and power consumption performance, were reported proving their compliance with the requirements defined for the aperture array instrumentation and reported in the references..

The ITPM board and its components, along with its sub-rack system, are in an engineering process aimed at SKA volume optimized mass production.

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