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The VIS detector system of SOXS

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ABSTRACT

SOXS will be a unique spectroscopic facility for the ESO NTT telescope able to cover the optical and NIR bands thanks to two different arms: the UV-VIS (350-850 nm), and the NIR (800-1800 nm). In this article, we describe the design of the visible camera cryostat and the architecture of the acquisition system. The UV-VIS detector system is based on a e2v CCD 44-82, a custom detector head coupled with the ESO continuous flow cryostats (CFC) cooling system and the NGC CCD controller developed by ESO. This paper outlines the status of the system and describes the design of the different parts that made up the UV-VIS arm and is accompanied by a series of contributions describing the SOXS design solutions (Ref. 1–12).

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Keywords: spectrograph, VIS, detector

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1. THE DETECTOR SYSTEM

The UV-VIS CCD Detector System for SOXS is designed to reach a wavelength response from 350 to 850 nm and consists of the following sub-systems:

1. e2v CCD44-82 2K x 4K CCD
2. CFC cooling system
3. detector head
4. CCD controller unit and power supply to operate the CCD detector head, with cable set to connect them
5. shutter
6. commercial shutter control unit with cable set
7. temperature controller with cable set

1.1 VIS Detector

The detector chosen for the SOXS UV-VIS arm is an e2v CCD44-82. This detector is a high performance, back illuminated CCD with a 15.0 μm square pixel and an image area of 30.7x61.4 mm and is characterized by a high Quantum Efficiency (QE). In figure 1 is shown the QE of this detector for different coatings. This detector technology was chosen for the following reasons:

1. devices manufactured with this technology meet or exceed the requirements
2. INAF has experience with devices with this technology and it is considered to be of low risk

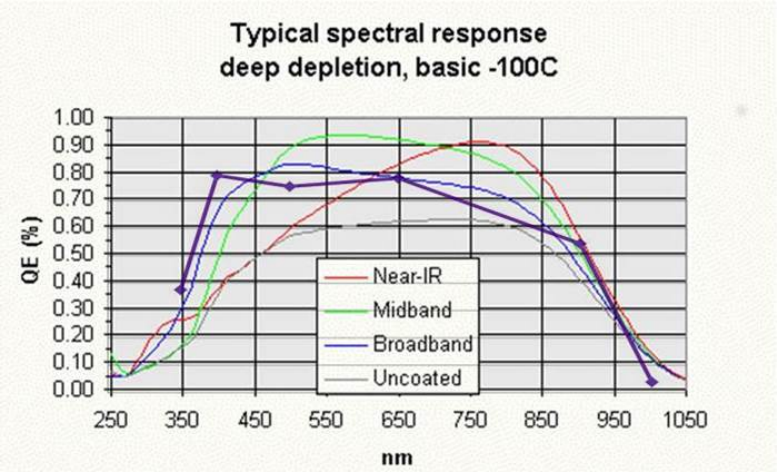

Figure 1. QE vs. wavelength for different coatings as provided by the manufacturer. The selected CCD is the midband, the purple points are our specific CCD QE data, taken from the e2v technical note

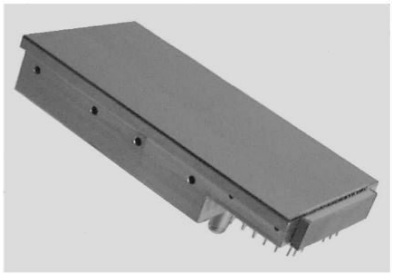

Figure 2. CCD44-82 back-illuminated CCD sensor

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Table 1. CCD main characteristics.

Detector	CCD44-82
Chip type	Thinned back illuminated
Pixel size	15 μm
Area (pixels)	2048 x 4096
Area (mm)	30.7 x 61.4
QE at 500 nm	90%
Coating	yes
Flatness	Better than 20 μm peak to valley
Peak signal	200 ke-/pixel
CTE Serial OSL	99.9993%
CTE Serial OSR	99.9999%
CTE Parallel	99.9998%

1.2 The camera housing

The detector head and wiring are based on the heritage of existing instruments at ESO. The head is coupled with a Continuous Flow Cryostat (CFC) cooling system , successfully adopted in several ESO projects. The UV-VIS camera is made up by the ESO CFC cooling system coupled through a bellows with the custom detector head that allows its placement into the UV-VIS arm of the spectrograph figure 3. Due to the reduced space available in the spectrograph, the front part of the camera, where the light will be incoming, has a special rectangular design called 'nose'.

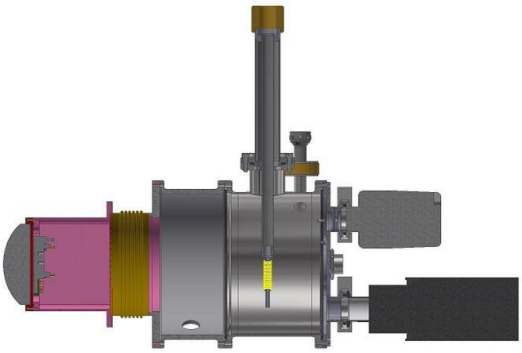

Figure 3. Drawing of the VIS detector system

1.3 Detector head and wiring

The detector wiring, i.e. the baseplate and flex circuits, will provide the components to safely mount the CCD and to conduct signals from the CCDs to the external wall of the cryostat. It also provides the mounting and wiring for the temperature sensors and heater that stabilize the detector temperature and monitor cryostat performance. The detector wiring will place minimal heat load on the cooling system. It should not introduce noticeable crosstalk or readout noise, and it should also be flexible enough to accommodate shrinkage during cooling down. It should not add appreciably to the outgassing and should use as much as possible previously tested cryogenic compatible materials and components. In the design and choice of fabrication materials and techniques for the detector head wiring, the following rules have been followed:

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- the preamplifiers are directly attached to the cryostat or very close to it
- the clocks-filters and wave-shaping (passive components) are placed in a shielded box attached to the cryostat
- clock, bias, output, and temperature signal groups are kept separate, with ground shields in between
- the thermal load of wiring on cryogenic cooling is kept as low as possible

1.4 CCD controller unit

The detector controller provides the biases and the correct sequences of clocks and analog video processing to drive and acquire the images of the CCDs. The dead time is defined as the interval between the end of one exposure (closed shutter) to the start of the next one (open shutter) and it obviously includes the read time and also other software overheads, e.g. for data storage and shutter control. The CCD controller will be the NGC (New General detector Controller) system. This controller, designed by ESO to replace the former FIERA and IRACE devices, is a single multipurpose controller able to manage both CCDs and IR arrays.The NGC is the current controller for ESO instrumentation and it will be adopted in SOXS project as well to comply with ESO standards and to reduce any compatibility failure with ESO hardware and software systems. The NGC is based on newest hardware standard (FPGA), it has the same hardware core for both optical and IR controllers and, in addition, is full compatible with ESO software and it includes all the good features of previous systems.

The NGC consists of five major components:

- Data Acquisition Computer with integrated PCI interface (DAQC)
- Detector Front-End (DFE)
- Detector Cryostat Cables (DCC)
- Detector Front-end Power Supply (DFPS)
- Detector Preamplifier (DPA)

The main NGC features are:

- high speed link
- the core element on each board is a Xilinx FPGA
- digital parts and the sequencer are implemented in the FPGA
- compact system
- full compatibility with ESO software standard

The controller has to be located near the detector, because the maximum cable length must be 2 m.

The control system is composed by:

1. LLCU, which is a Linux machine (DELL or an industrial PC)
2. PCI-Express card
3. front-end box (preamplifier)
4. power supply, including the cable to the NGC
5. two NGC modules for operations with CCD detectors
6. fiber interfaces, including fiber cable
7. CCD temperature control
8. shutter driver

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Figure 4. The NGC water-cooled housing



Figure 5. The NGC Two-Slot system housing

The NGC system has three possible housings: compact, fan-less and water-cooling. The housing is selected according to the setup where the controller is located. In SOXS we need to locate the controller close to the instrument because the cable between the cryostat and the device must be shorter than 2 m. Therefore, we selected the water-cooled housing to prevent any thermal dissipation into the telescope Nasmyth room.

The power supply for the NGC device is a 19-inch 3HE rack-mountable unit, which may be at a distance from the detector Front End (DFE) of up to 12 meters (see figure 9).

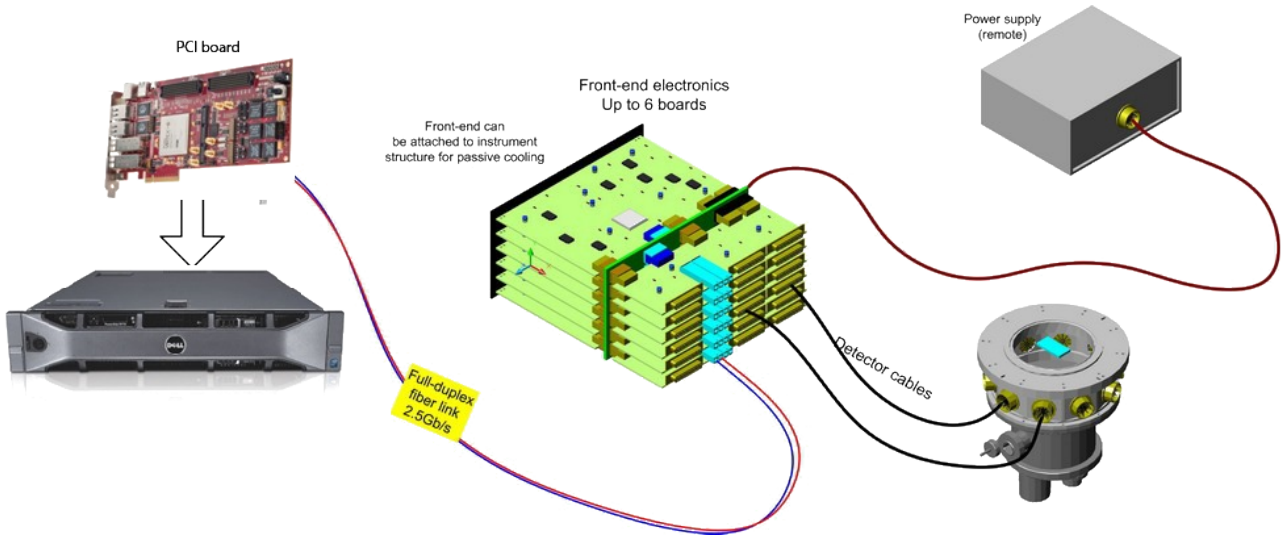

Figure 6. The ESO New Generation Controller functional diagram.

1.4.1 PCI interface Board (DAQC)

An ESO custom-made PCI64 board (figure 7) with a fiber-optic connection to the Front End is installed in the Data Acquisition Computer (DACQ). The maximum theoretical bandwidth per interface is 256MB/s, which matches the 2.5 GBit/s fiber transmission rate. The bandwidth for actual data transmission is about 20% lower.

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Figure 7. The PCIe interface board.

1.4.2 Detector front-end (DFE)

The DFE has to be located close to or on the instrument (maximum detector cable length 2m; depending on the application, an extension up to 3m may be possible). The module, from which the VIS NGC DFE can be built, is one Basic Board that contains four video channels and clock/bias generation. In order to prevent damage from overheating, all housings should be equipped with a thermal sensor that can shut off the power to the NGC box.

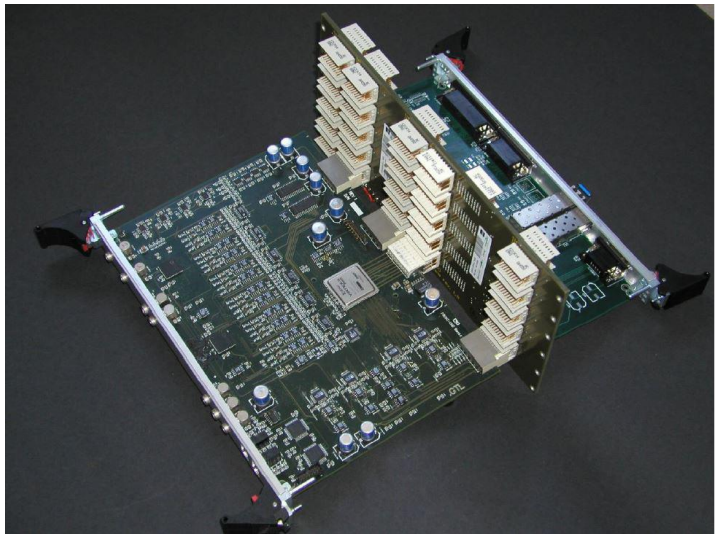

Figure 8. NGC system with Basic Board, Backplane and Transition Board (VIS arm).

1.4.3 Detector Cryostat Cables (DCC)

The Detector Cryostat Cable is the connection between the DFE and the VIS camera (figure 6). It contains the clock and bias lines and the video signals. The maximum length depends on application (2-3 m).

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1.4.4 Detector Front-end Power Supply (DFPS)

The power supply for the DFE is a 19-inch 3HE rack-mountable unit which may be at a distance from the DFE of up to 12 meters.

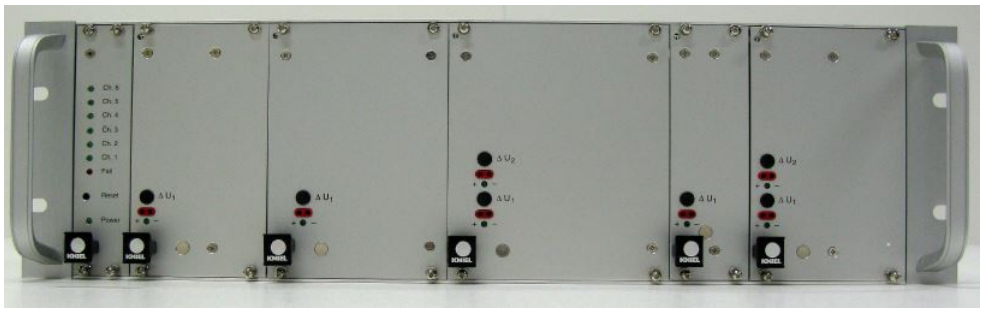

Figure 9. Power supply (front view).

1.4.5 Detector Preamplifier (DPA)

The CCD preamplifier is placed between the cryostat and the DFE. The location of the Detector Preamplifier is application dependent; in the SOXS case of an optical detector the preamplifier is located outside the cryostat. It features 4 video channels with 16 software-selectable gains and 8 software-selectable bandwidths per channel. Its outer dimensions are 100 x 120 x 40 mm^3. The preamp is show in figure 10.



Figure 10. Detector Preamplifier (DPA).

1.5 Shutter control

The shutter is driven by the NGC through its own commercial controller; it is upstream from the detector unit, at the entrance slit of the spectrograph (figure 11), which allows us to use a small shutter aperture. The selected model is an Uniblitz ES6B with its VED24 controller. (figure 12).

Features:

- 6 mm aperture
- bi-stable operation
- extremely low-profile form-factor
- RoHS compliant
- transfer time on opening: 1.9 milliseconds
- total opening time: 3.7 milliseconds
- can be configured for the VED24 shutter driver

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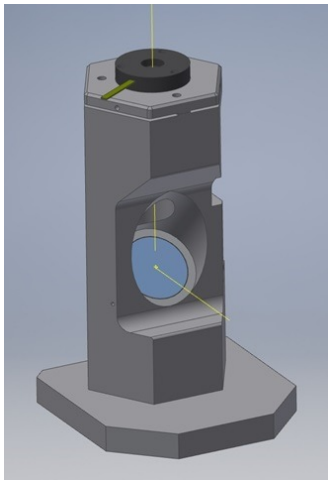

Figure 11. The entrance slit of the spectrograph and the UV-VIS shutter.



Figure 12. Shutter Uniblitz ES6B and controller VED24

1.6 Temperature controller

For the CCD temperature control two options can be take into account:

- The CCD controller integrated control
- A commercial temperature controller (i.e. Lakeshore 336.)

The characteristics of the Lakeshore 336 are summarized in the following list:

- operates down to 300 mK with appropriate NTC RTD sensors.
- four sensor inputs and four independent control outputs
- two PID control loops: 100 W and 50 W into a 50 Ω or 25 Ω load
- auto-tuning automatically determines PID parameters
- automatically switch sensor inputs using zones to allow continuous measurement and control from 300 mK to 1505 K
- custom display set-up allows you to label each sensor input
- Ethernet, USB, and IEEE-488 interfaces
- supports diode, RTD, and thermocouple temperature sensors
- sensor excitation current reversal eliminates thermal EMF errors for resistance sensors
- ±10 V analog voltage output, alarms, and relays

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Figure 13. Temperature controller Lakeshore 336.

2. CONCLUSIONS

The VIS-UV detector system is part of the VIS arm of the SOXS spectrograph that will be installed at the ESO NTT telescope located at La Silla observatory. The project is going to conclude the final design phase in 2018. Afterward, the plan is to integrate the instrument in Italy and then have the first light within 2020.

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